Proposal for DUNE FEMB QC Test

Lingyun Ke

Date 06/28/2024

@BrookhavenLab

Content

- **1. QC Test Setup Hardware**
- 2. Test Procedure with CTS
- 3. Software Operation

QC Test Setup Hardware

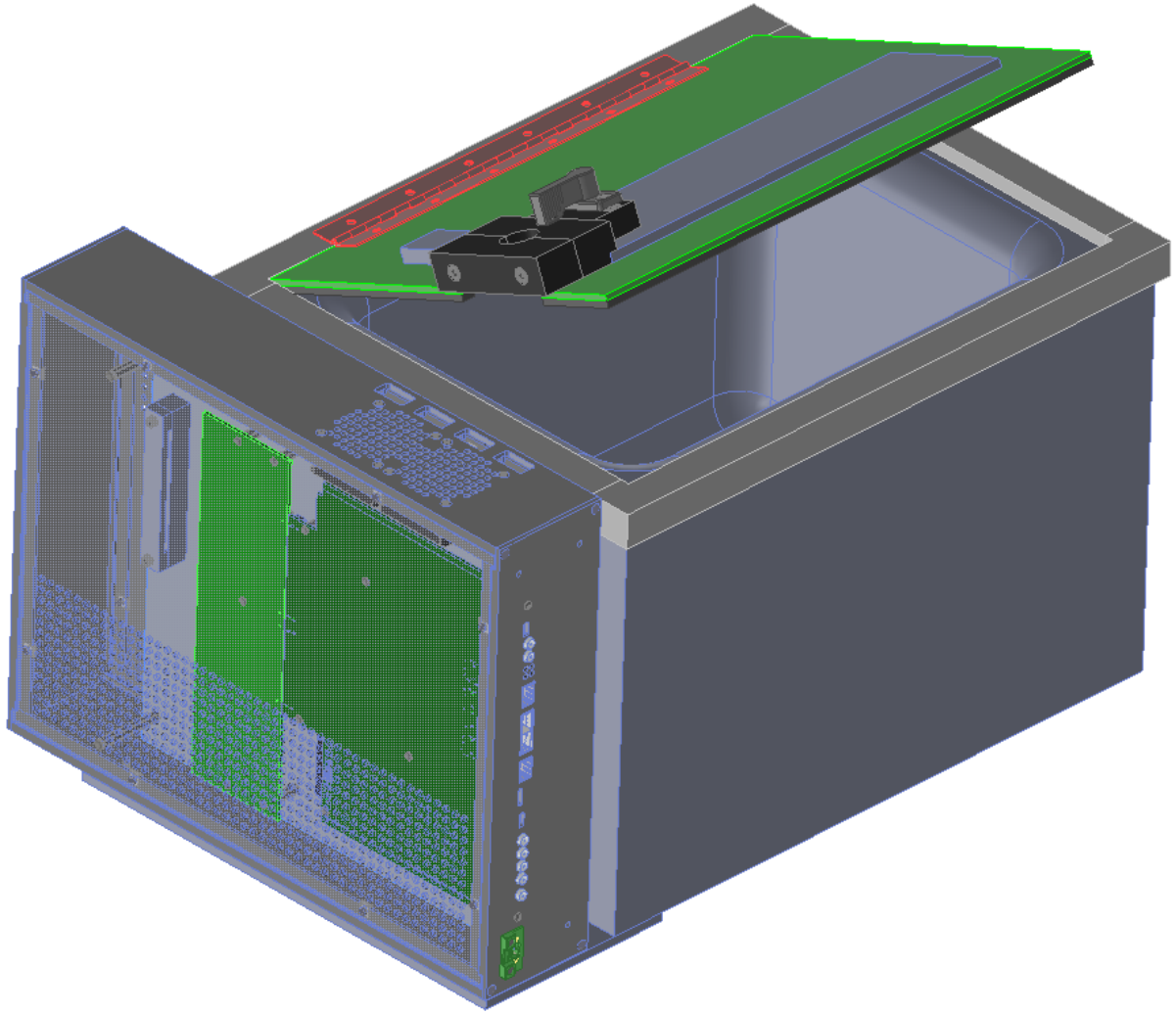
QC activities will be monitored and led by the **TPC electronics consortium**
The **same hardware setup** CTS and the same QC procedure will be distributed to all test sites.

The Hardware Setup contains:

Item	Provider
Repurposed Cryogenic Test Setup (CTS)	**MSU / BNL**
Warm Interface Board Box (WIB box)	**BNL**
Blue Plate (contain 4 * FEMB)	**BNL**
Fiber Converter	**BNL**
ESD monitor	**Test Sites**
12V / 6A DC Power Supply	**Test Sites**
Windows PC	**Test Sites**

QC Test Setup Hardware

3D module for the CTS Cold box with WIB box



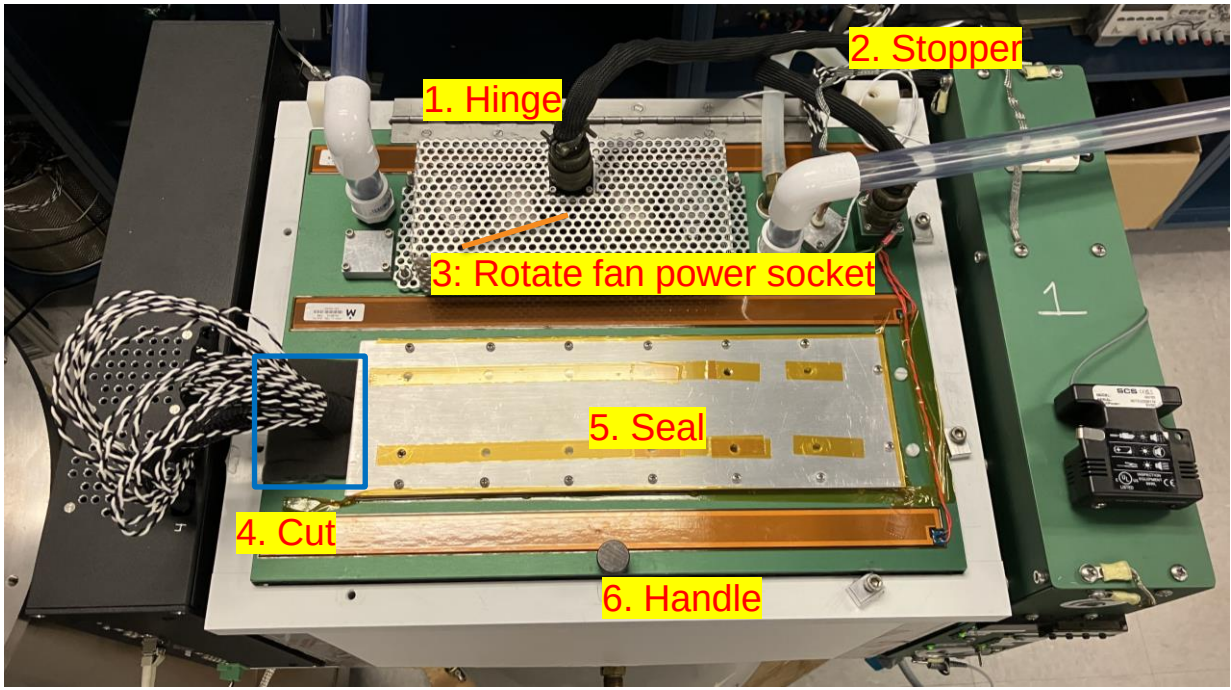
CTS cover is modified to be openable

Changes on CTS

CTS cover is modified to be openable

Prototyping

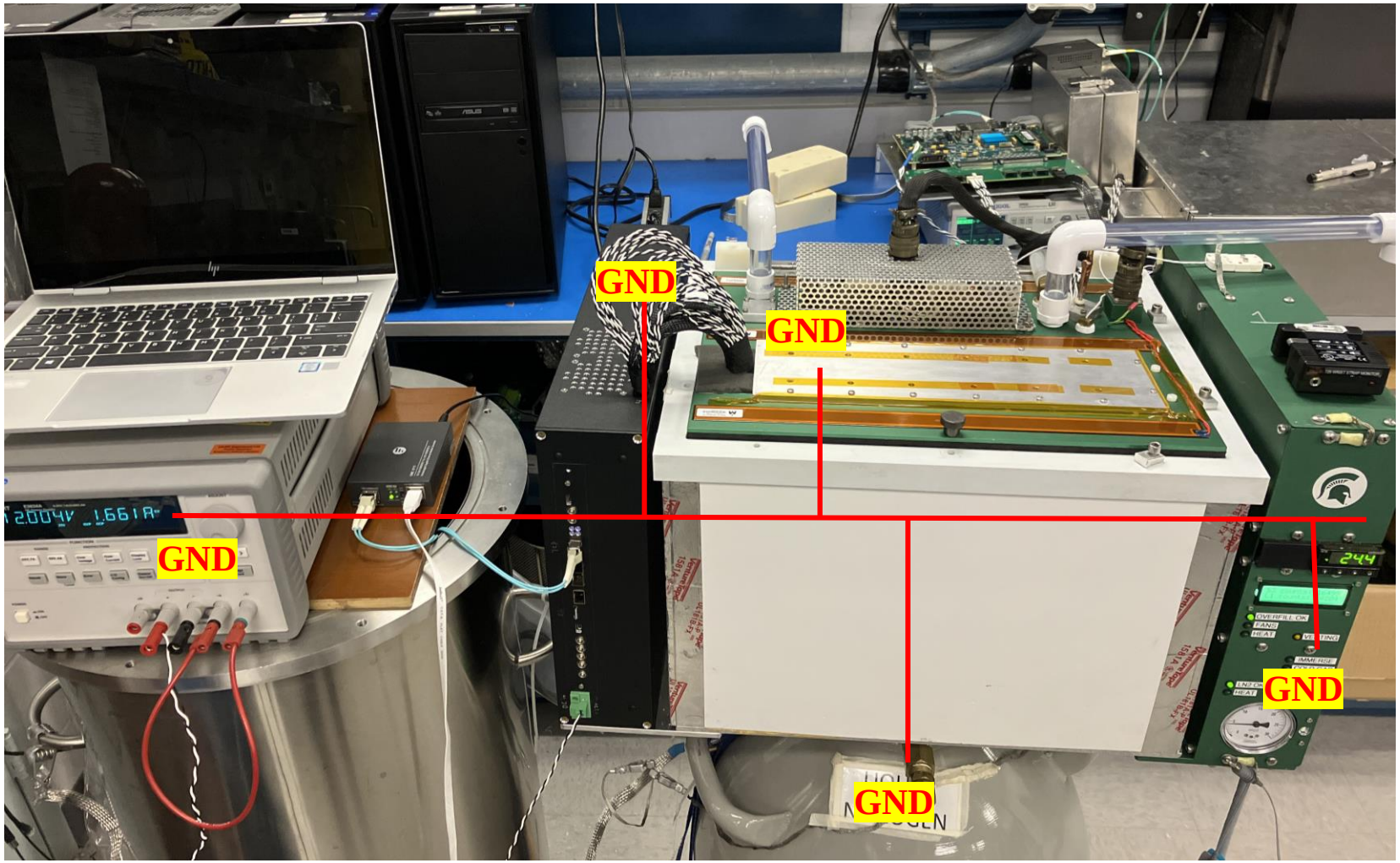
Item
1: Hinge
2: Stopper
3: Rotate fan power socket
4: New cut for cables (stopper/feedthrough to be added to prevent venting)
5: Seal the original cut
6. Handle to lift up cover



Note: All test sites can send the cover to BNL for modification. BNL will provide drawing and instruction for installing the setup.

Grounding

Cold chamber, WIB box, CTS controller are grounded.
It basically follows the ProtoDUNE grounding and isolation rules



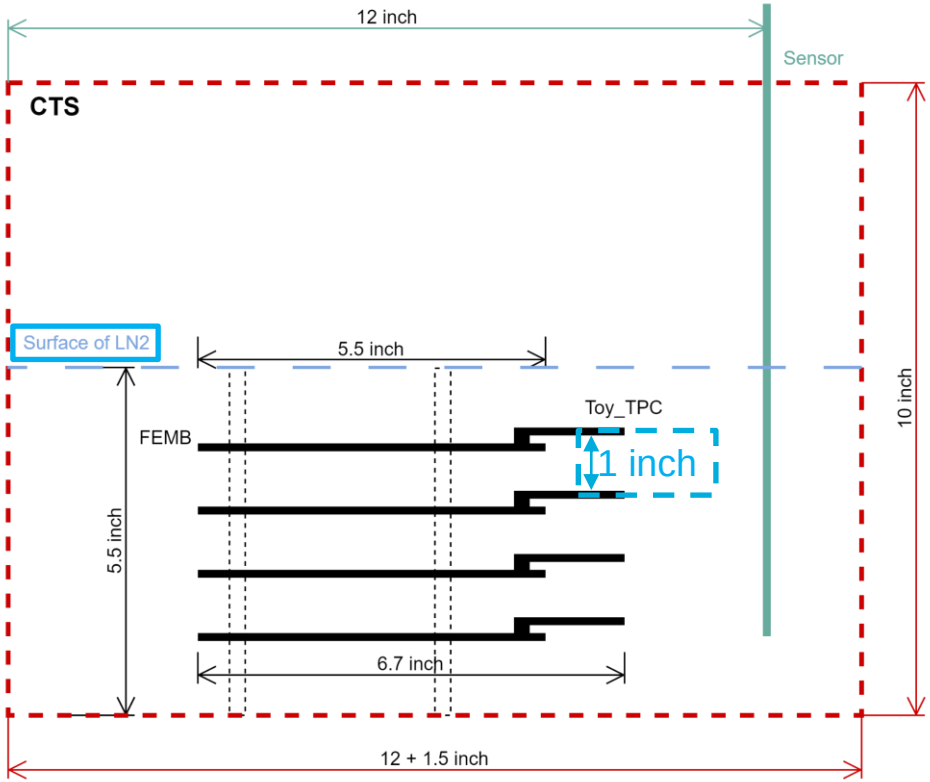
WIB Box


Power Cables
Data Cables
Adapter Board
WIB Board
Fan

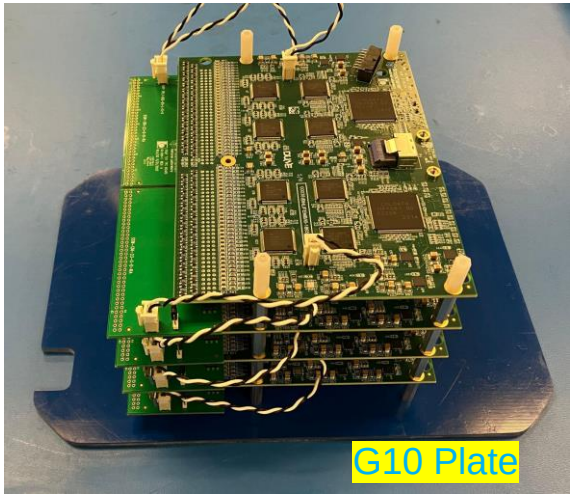

Slot #1
Slot #2
Slot #3
Slot #4
Cable Cage

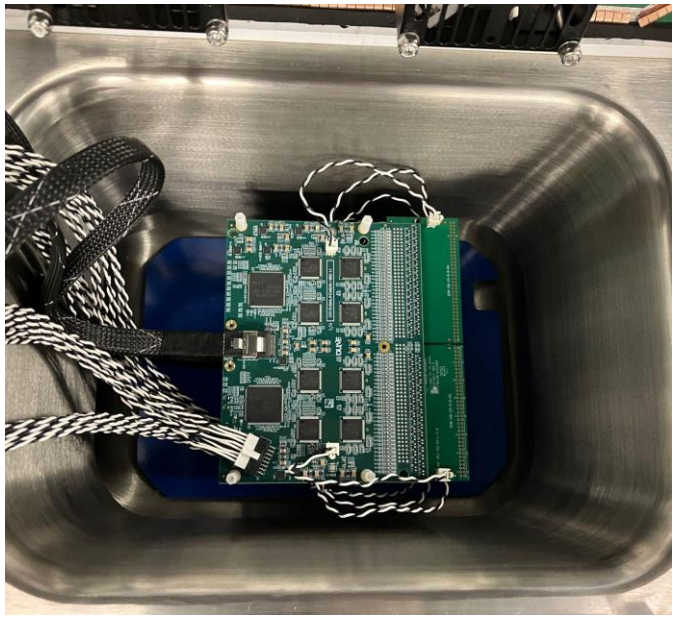
Propose to QC test on FEMB board ONLY

The Blue Plate can hold 4 FEMBs in CTS for QC test



CTS chamber provides 5.5 inches deep LN2





The return path (grounding) of FEMBs connects to WIB box via cold cables.

Brookhaven National Laboratory

Why QC test on FEMB board ONLY is preferred

- **The main purpose of cold test is to screen out boards with defective semicondutor components**
  - LArASIC, ColdADC, COLDATA, LDO, Analog switch, protection diode
  - Poor soldering can be recognized via thermal expansion
  - Passive components (resistor, capacitor, connector) **unlikely** fail at cold

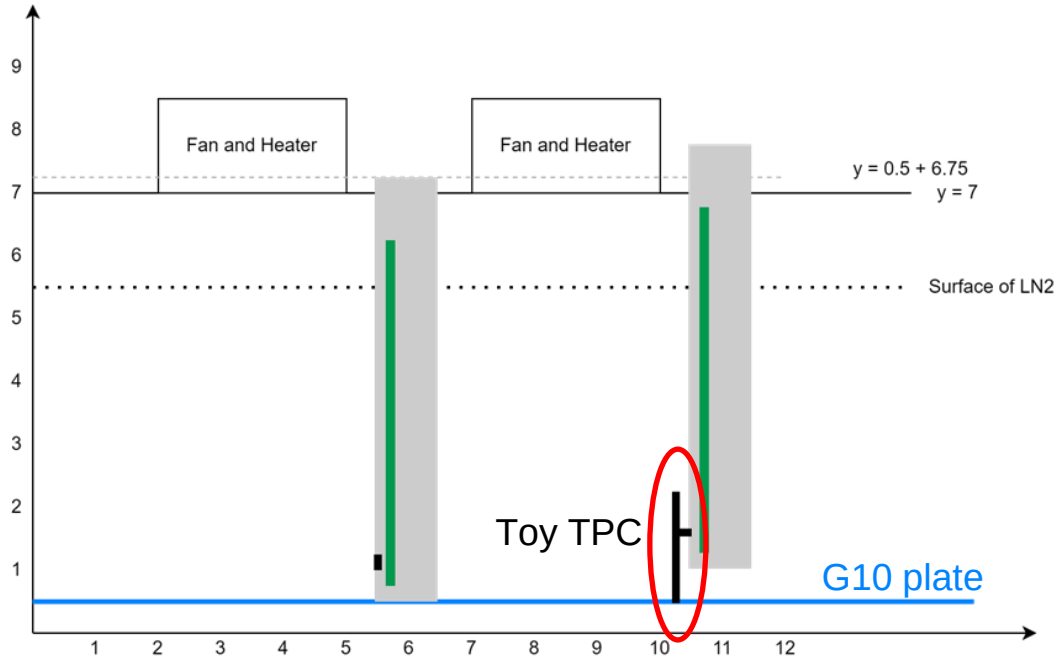
- **Yield of FEMB is not high yet**
  - FEMB-VD-1J: The post-assembly yield is **21**/25 = 84%
  - FEMB-VD-1J: **17 of 25** passed warm & cold QC in the first run. **Yield = 68%**
  - CE box assembly should ONLY be done by qualified technicians
    - Yield < 90% will require much extra effort

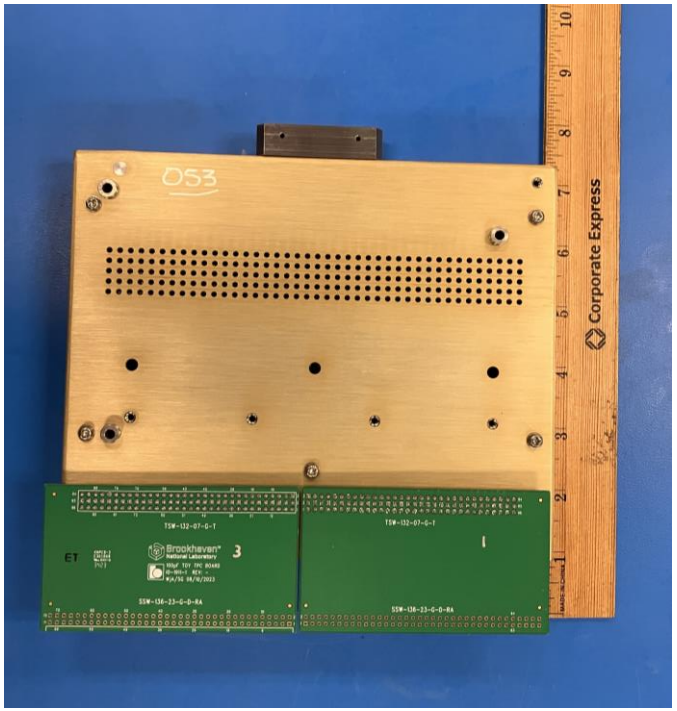
- **Install / Uninstall cold cables inside CE box is more difficult**

- **Limited space of CTS chamber**
  - Not realistic to hold up to 4 CE boxes
  - Stack-up CE boxes inside CTS chamber is difficult
    - To achieve uniform result, **position of each FEMB/CE box must be determined**
      - Hard to hold CE boxes in place

If QC test applied to VD CE box assembly

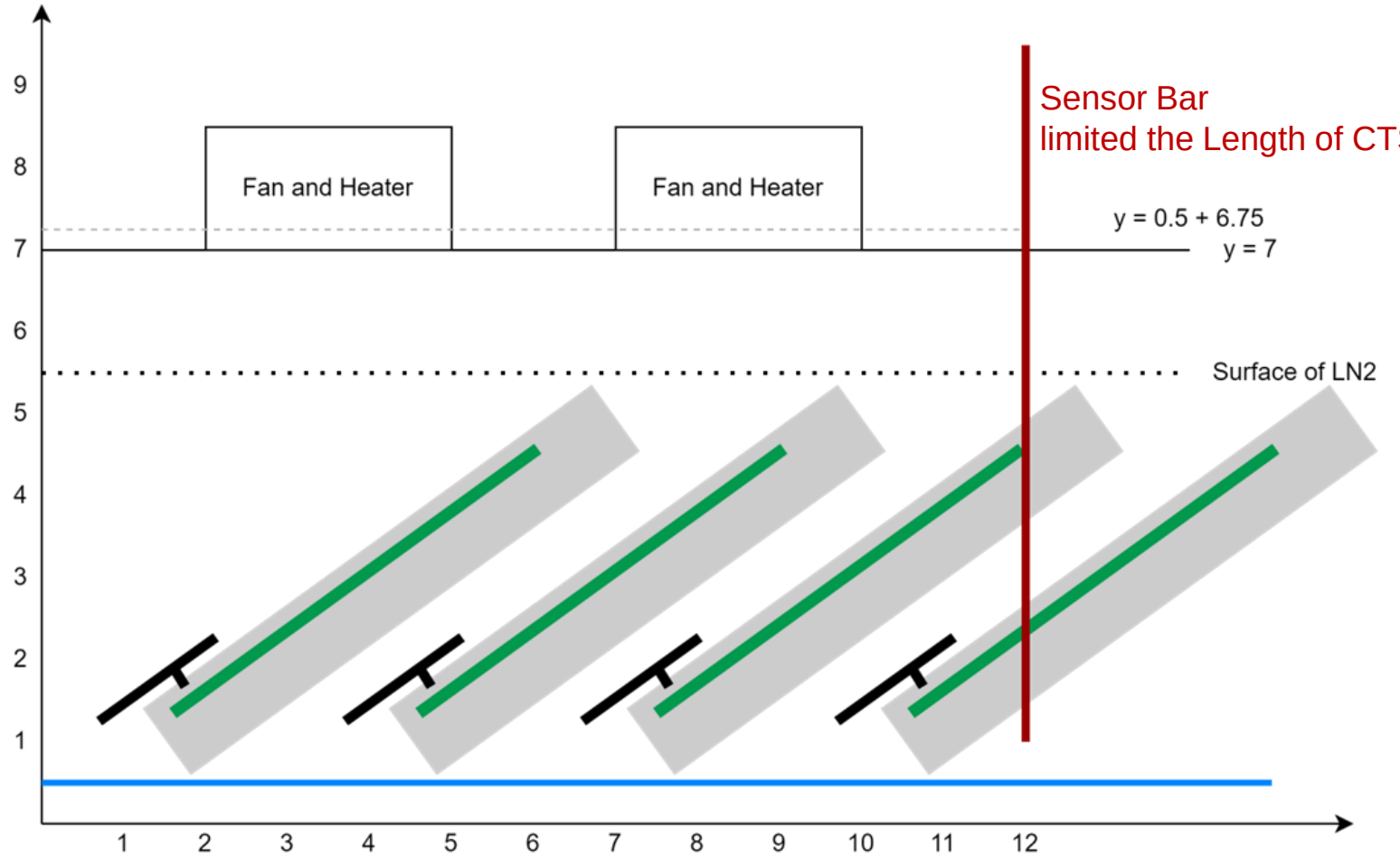
- VD CE Box can only be positioned tilted to be submerged in the LN2.
- HD CE box with CR-RC adapter board can only be placed flat to fit in CTS chamber, takes more space.





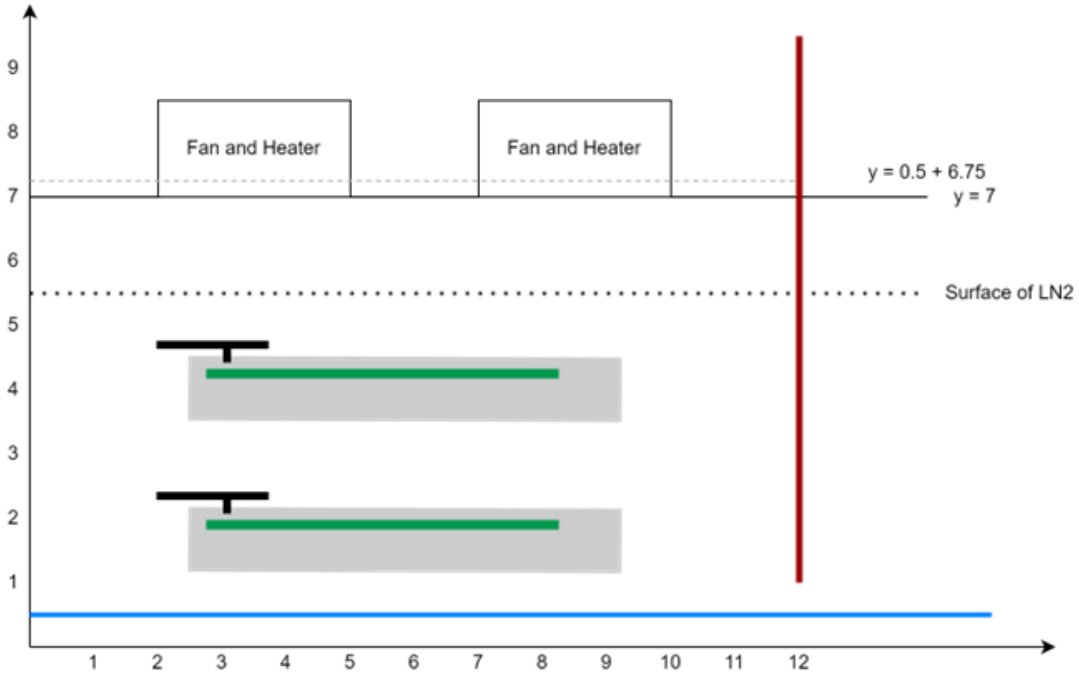
If QC test applied to VD CE box assembly

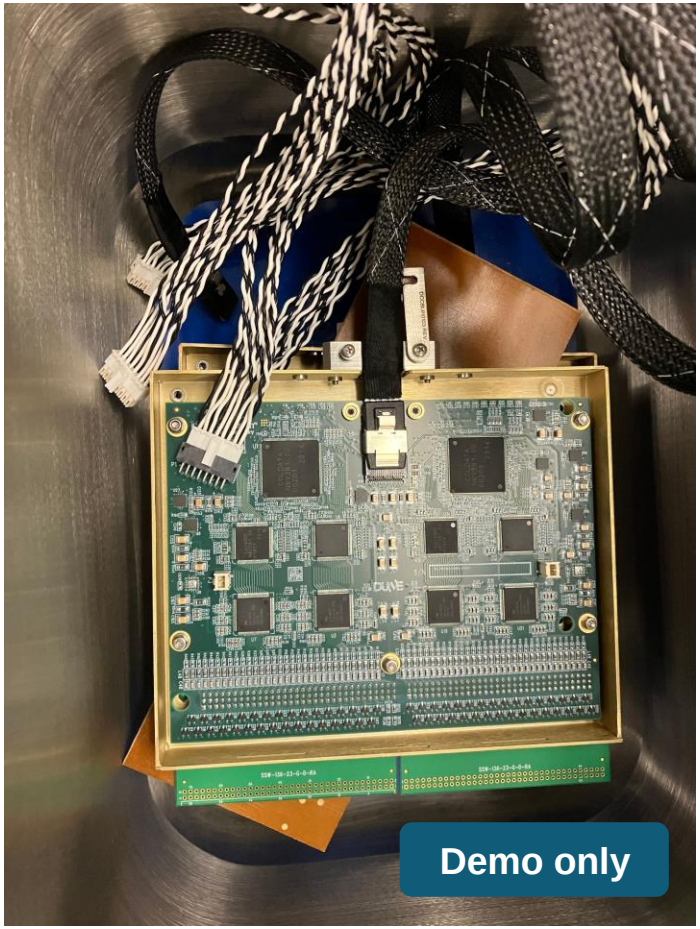
Taking support structure into account, stacking 4 VD CE boxes up is unlikely to be achievable.
The space of CTS is not enough for 4 CE boxes. Cabling is difficult as well.



If QC test applied to VD CE box assembly

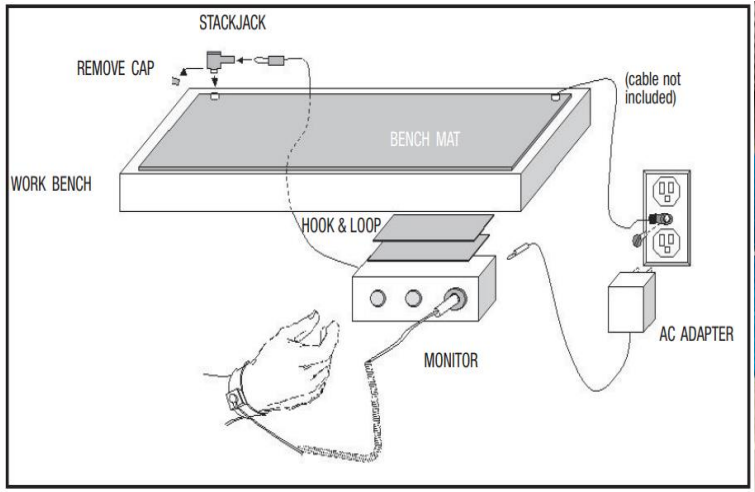
The placement of 2 VD CE boxes is acceptable.
A support structure to hold CE boxes in certain positions should be added.

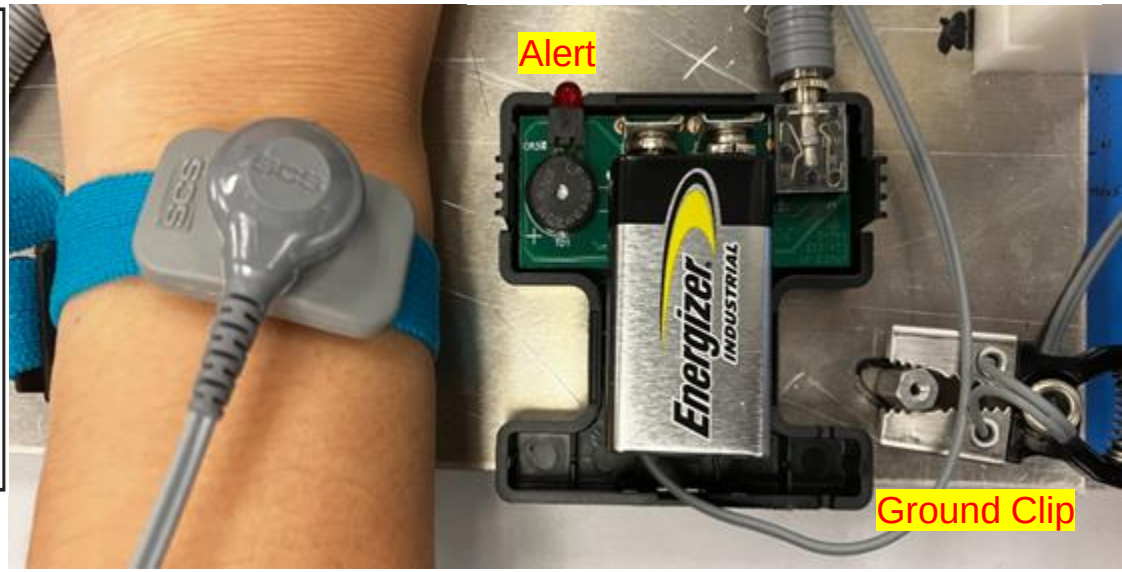




ESD Protection Consideration

An **Electrostatic Discharge** (ESD) **monitor** is deployed to assure safe handling.

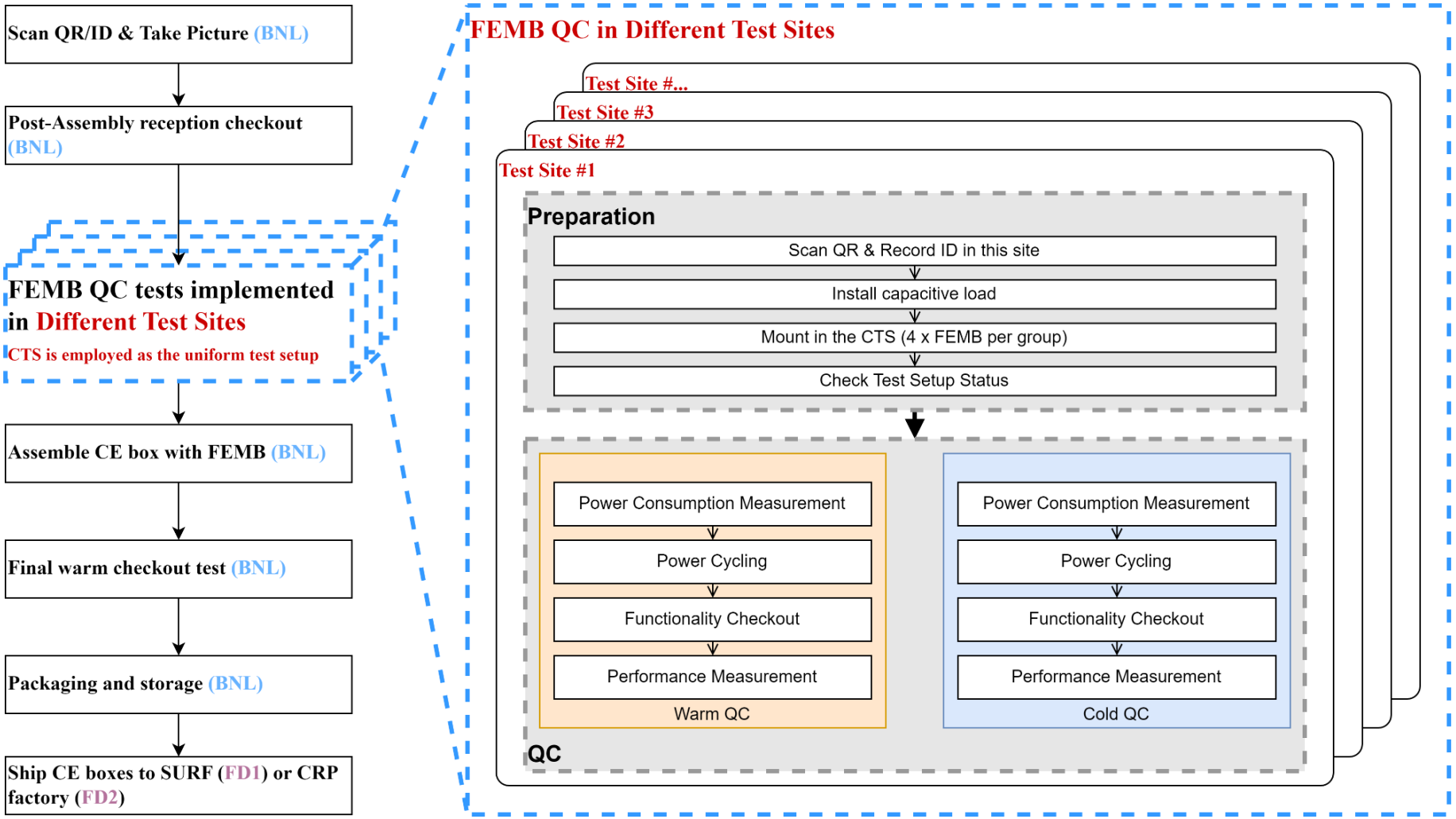




Content

- 1. QC Test Setup Hardware
- **2. Test Procedure with CTS Hardware**
- 3. Software Operation

Proposed Overall FEMB QC Procedure

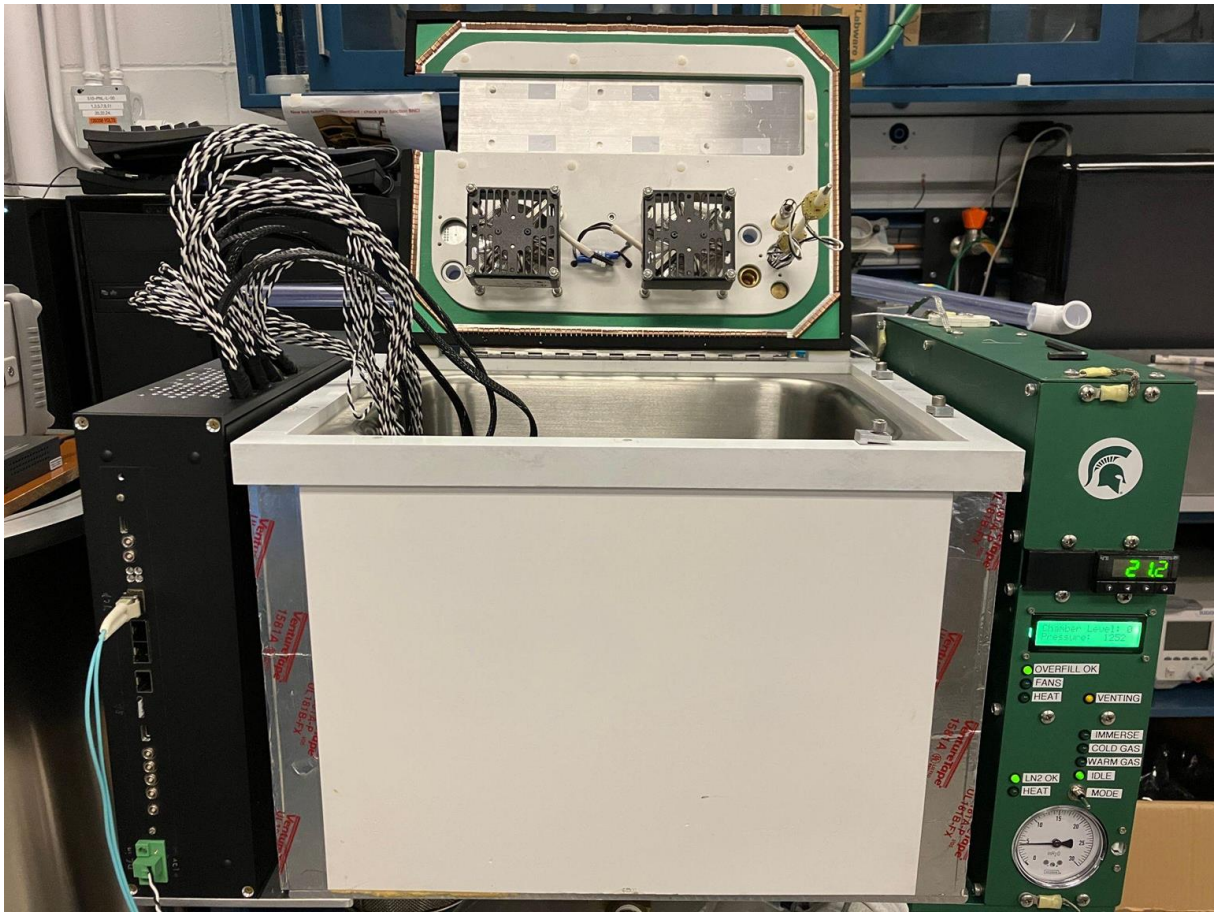


The **same hardware setup CTS** and the same QC procedure will be distributed to all test sites.

Test Procedure with CTS Hardware

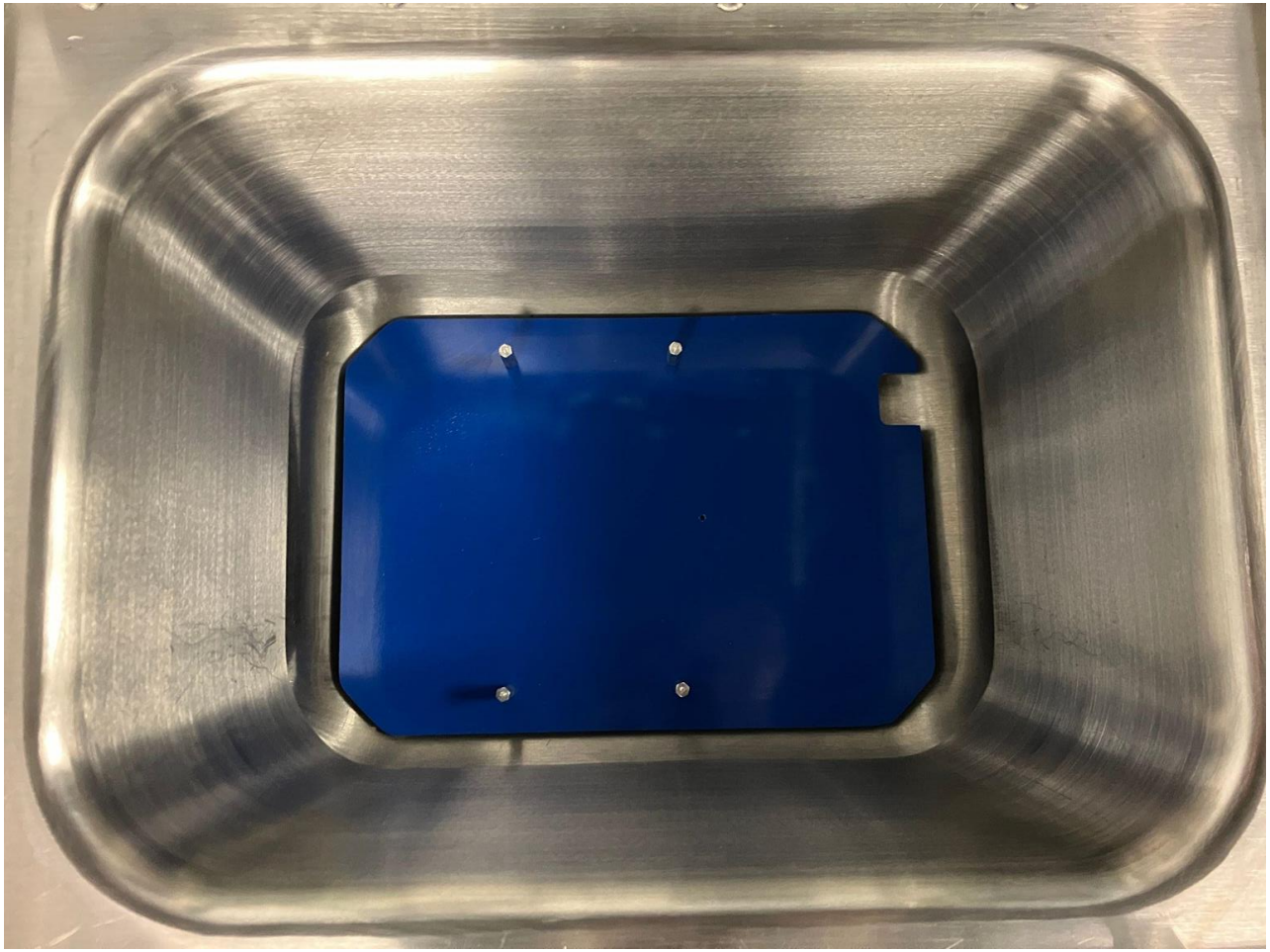
FEMB Preparation	Open cover of chamber
	Place blue plate inside chamber
	Install FEMBs
	Close Cover
Warm Test	WIB Power On
	Warm QC
	WIB Power OFF
Cold Test	LN filling
	WIB Power On
	Cold QC
	WIB Power OFF & Warm Up
Disassembly	Remove FEMBs

Visual inspection and Ground check



Test Procedure with CTS Hardware

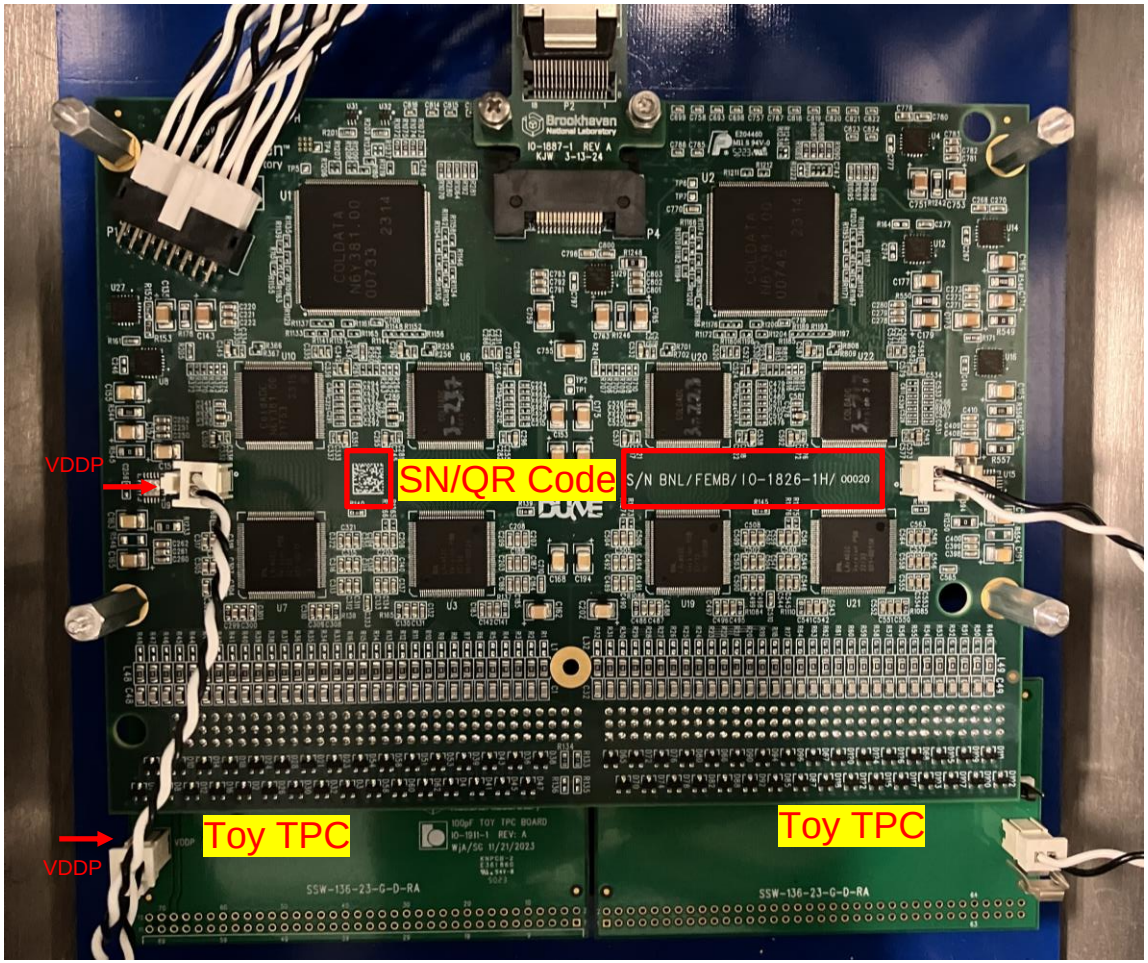
Assembly: Place blue plate inside chamber



Blue plate is made by **G10**, standoffs on it are isolated from chamber.

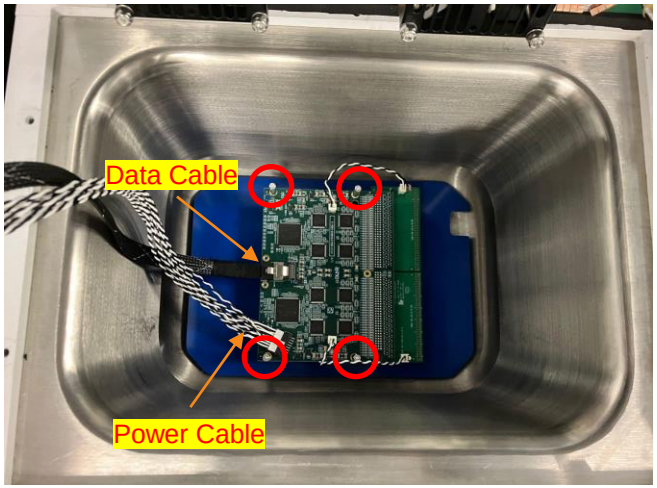
FEMB preparation

1) SN/QR reading
2) PCB-based Toy TPC

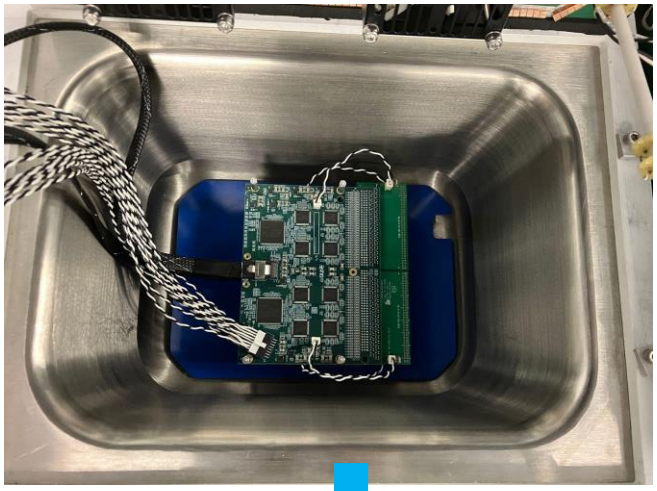


FEMB preparation

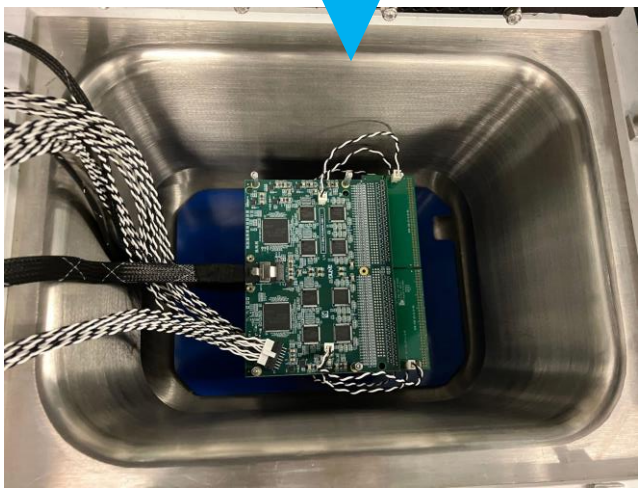
Assembly: Install & Cable 1st FEMB



Assembly: Install & Cable 2nd FEMB



Assembly: Install & Cable 3rd FEMB



Assembly: Install & Cable 4th FEMB

RT Test

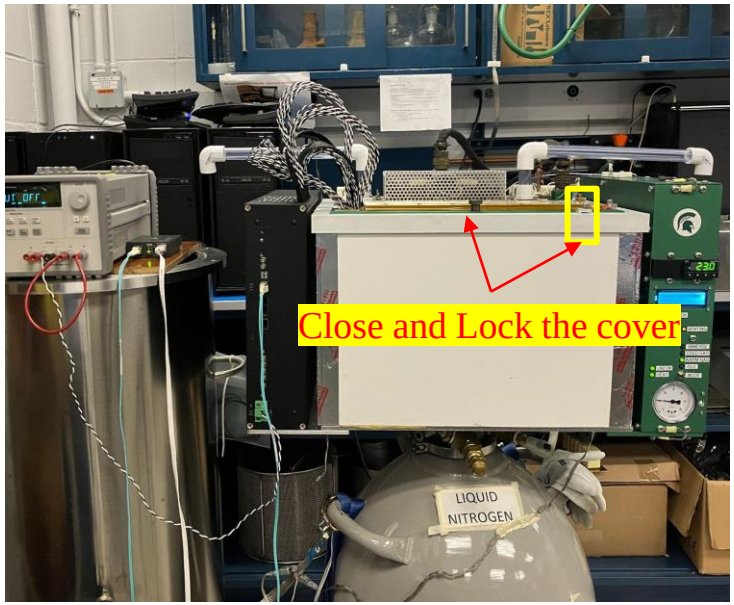
Initialization → **Checkout** → **QC** → **LN Preparation**

- Power On
- CTS → IDLE
- WIB Initialization

- Power Check
- Continuity Check

- Power meas & cycling
- Pulse response
- Monitoring
- Noise Measurement
- Calibration
- ….

- WIB Power Off
- Fill LN2




```
================================================================================
+++++++                GENERAL REPORT for FEMB BOARDS TESTING
+++++++
================================================================================


01 Initial Information
Operaton: lke
env: RT
Toy_TPC: 150 pF
Note: com
FEMB ID: {'femb0': 'G38', 'femb1': 'G10', 'femb2': 'G39', 'femb3': 'G12'}
date: 10_12_2023_19_48_53
/n
FEMB ID 38      PASS    ALL ASSEMBLY CHECKOUT
FEMB ID 10      PASS    ALL ASSEMBLY CHECKOUT
FEMB ID 39      PASS    ALL ASSEMBLY CHECKOUT
FEMB ID 12      PASS    ALL ASSEMBLY CHECKOUT
```

LN2 Test

Cool Down

Initialization → **Checkout** → **QC** → **Warm Up**

The same procedure as the RT Test

- **CTS Cool Down**

IDLE → Warm gas
Warm gas → Cold gas (5min)
Cold gas → Immerse
Ready → Level 3

- **CTS Warm Up**

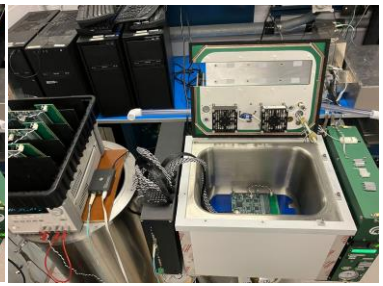
WIB Power Off
Immerse → Warm gas
Ready → Temperature > 30 °C

```
==========================================================================================
+++++++                  GENERAL REPORT for FEMB BOARDS TESTING                  +++++++
+++++++                                                                          +++++++
==========================================================================================


01 Initial Information
Operator: lke
env: LN
Toy_TPC: 150 pF
Note: com
FEMB ID: {'femb0': 'G38', 'femb1': 'G10', 'femb2': 'G39', 'femb3': 'G12'}
date: 10_12_2023_20_09_12
/n
FEMB ID 38      PASS    ALL ASSEMBLY CHECKOUT
FEMB ID 10      PASS    ALL ASSEMBLY CHECKOUT
FEMB ID 39      PASS    ALL ASSEMBLY CHECKOUT
FEMB ID 12      PASS    ALL ASSEMBLY CHECKOUT
```

FEMB Disassembly




Open Cover

Remove FEMBs (Cold cables) one by one and put them into an ESD-safe Tray

(-> check if FEMBs are completely dry)

Remove Toy TPCs

- Put the tray in dryer for one hour (optional)
- Each FEMB is enclosed into a ESD bag and foam box for storage and shipping

Checkout & QC Test Summary of 25 FEMB-VD(1J)

- Post-assembly Checkout (**21**/25 = 84%)

FEMB	Failure Modes	Test Environment	Description	Status
#56	Assembly	RT	A poorly soldered P4 data connector	Repaired
#12	Assembly	RT	Shorts were observed on LArASIC	Repaired
#61	LArASIC	RT	CH-115 ESD damage	Repaired
#43	LArASIC	RT	LArASIC U17 SPI SDO can not send signal	Repaired

- Initial QC results shown in the table below
  - Current Yield: **17/25 = 68%**
  - **22/25 = 88%** if issued FE chips are screened out during ASIC QC

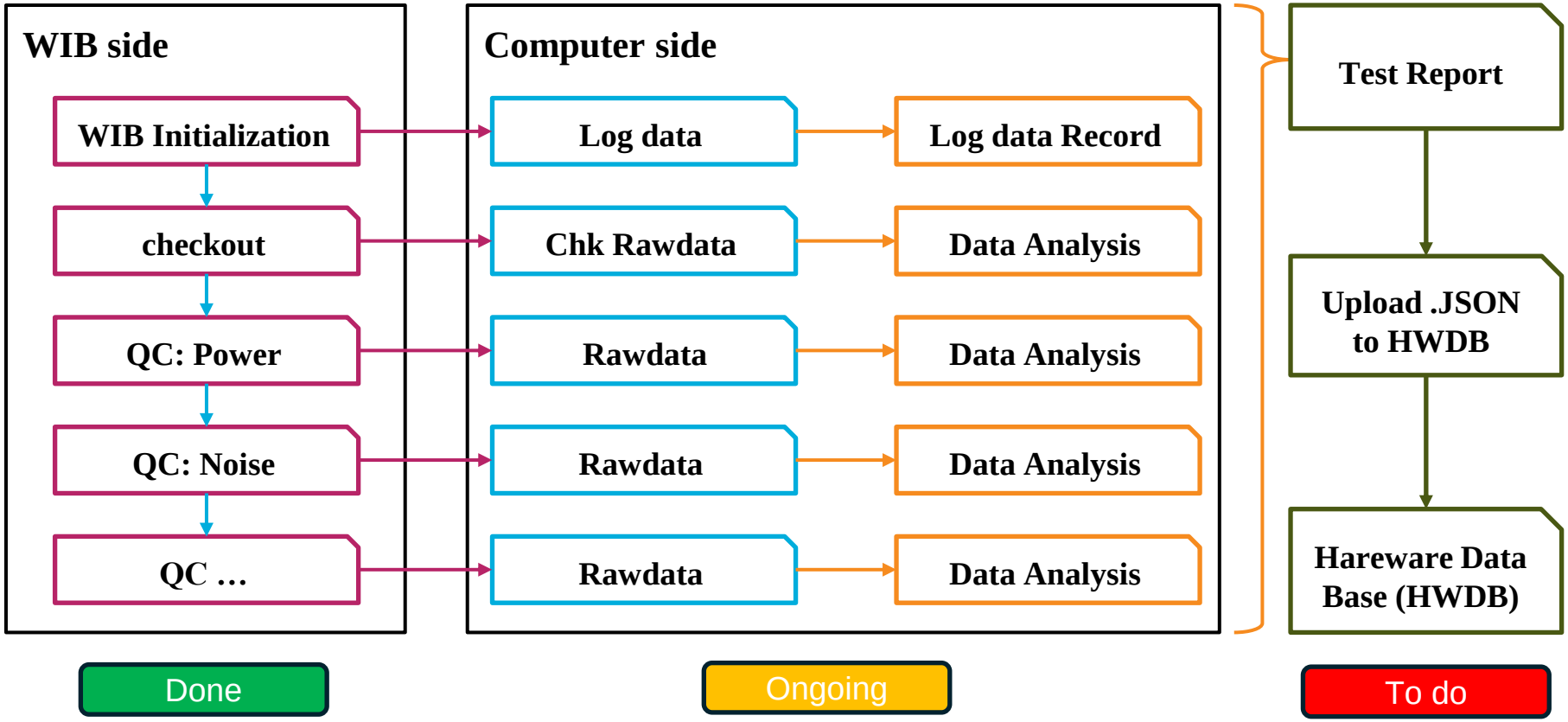
#03	ColdADC	LN2	When temperature lower than 173 K, register values of ColdADC chip#7 after POR are not default	To be repaired
#S12	Regulator LArASIC	LN2	1. U12 (LDO) output voltage lower than set value at cold 2. One of FE channel observed non-linearity issue at 4.7 mV/fC	Repaired
#36	LArASIC	LN2	One of FE channel observed non-linearity issue at 4.7 mV/fC	Repaired
#53, #11, #38, #61, #01	LArASIC	RT	One of FE channel observed non-linearity issue at 4.7 mV/fC (To be screened out during FE QC in future)	Repaired

Content

- 1. QC Test Setup Hardware
- 2. Test Procedure with CTS Hardware
- **3. Software Operation**

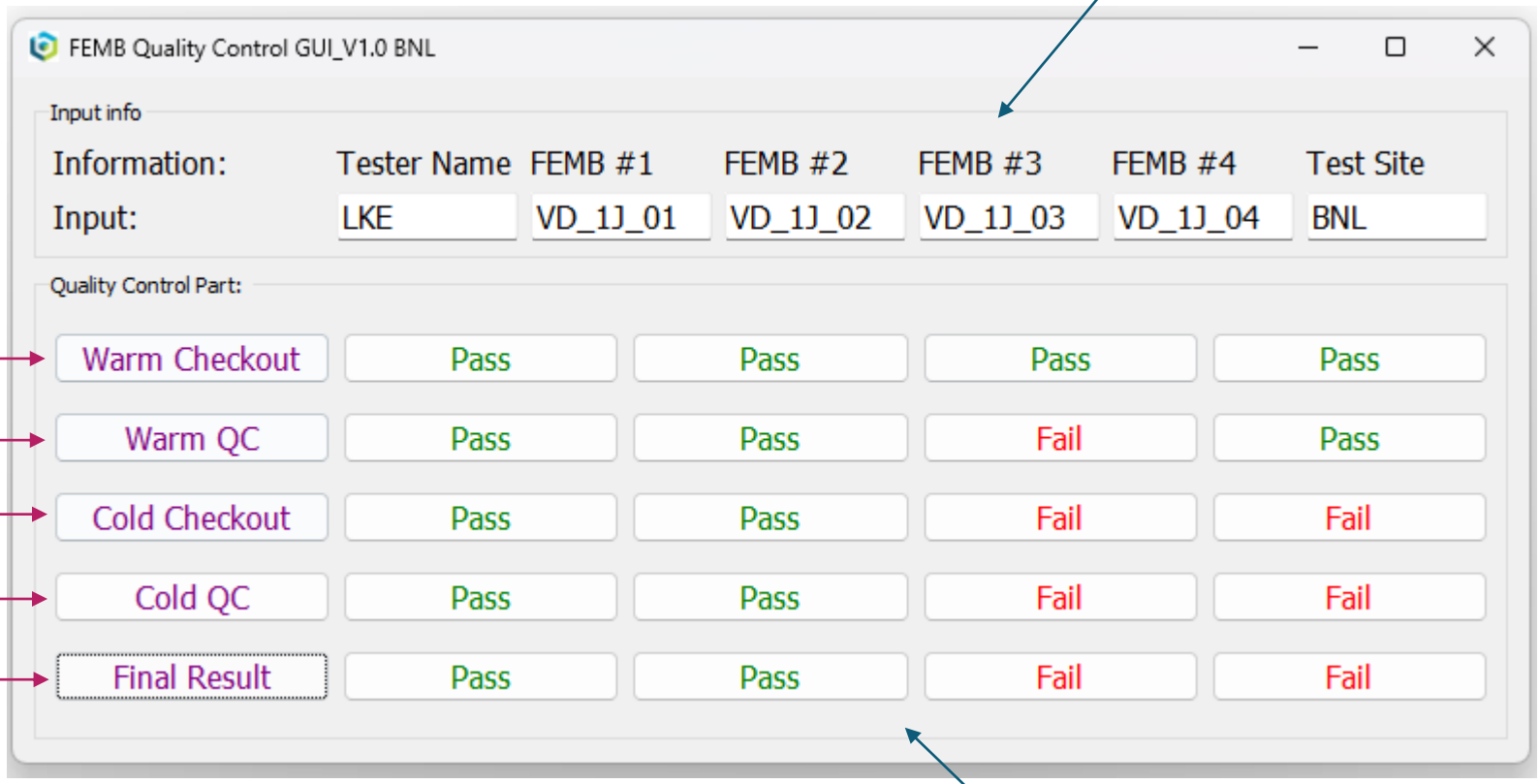
FEMB QC Test and Analysis Procedure

Current Procedure: data analysis is offline
Under-developing: data acquisition and analysis will be performed at the same time



User Interface

The software test scripts have been verified by QC tests.
Currently, command-based user interface is available.
Graphic User Interface (GUI) is going to be developed.



Summary

- The **updated CTS** can serve as a controllable testing environment for FEMB QC tests.
  - QC with CE box is possible but not recommended due to limited chamber space and yield of FEMB
- The **test procedure** has been well defined and **test script** has been developed.
  - Human intervene is minimized
  - A GUI to be developped to display QC status in real-time
- The time for one QC test cycle of 4 FEMBs is **2~3 hours**.
- Documentation (User Manual) is ongoing

Item	Time (s)
initial CTS and install FEMB in CTS box	600
Warm QC	1400
Fill LN2	1800
LN2 QC	1400
Warm up	2400

Plan for BNL Visit

- Proposed FEMB QC test sites
  - University of Cincinnati: Alex (CTS onsite)
    - Bring the CTS cover to BNL for modification
  - LSU: Hanyu (Transfer CTS from Martin)
    - Bring the CTS cover to BNL for modification
  - Iowa State: (Need a CTS)
    - BNL can spare one to Iowa State
- Training for FEMB QC at BNL
  - Week of 07/22, 07/29
  - Please submit BNL registration ASAP.

Thank you

Main Non-linearity Issue Explain

For the normal channel, each pulse's peak value corresponds to a DAC output that forms a straight line, demonstrating good linearity.
For the issue channel: The linearity is poor, illustrated by the red line.