LGADs for RDC3

Dr. Simone M. Mazza

(SCIPP, UC Santa Cruz)

On behalf of the LGAD collaboration

CPAD meeting July 2024

Pushing the time resolution limit with innovative LGAD design in combination with fast-timing readout and infrastructure

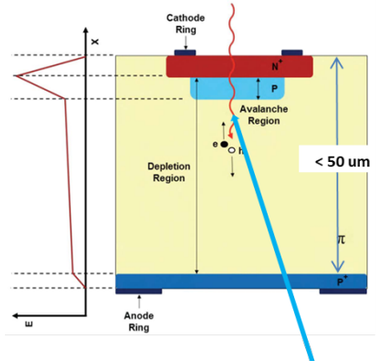
Institutions:

M. Artuso - Syracuse University
M. Benoit - Oak Ridge National Laboratory
G. Giacomini - Brookhaven National Laboratory
P. Gutierrez - University of Oklahoma
W. Li - Rice University
M. Marjanovic - University of Oklahoma
S. Mazza* - University of California Santa Cruz
S. Seidel - University of New Mexico

* Contact person: simazza@ ucsc.edu

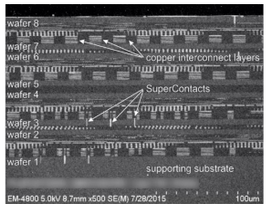
Institutions

- **UCSC**: Extensive silicon sensor and fast-timing readout characterization expertise. Sensor TCAD simulation
- **BNL**: Extensive silicon sensor fabrication expertise
- **ORNL**: Silicon sensor simulation, integration, assembly, and characterization expertise
- **OU**: Silicon sensor expertise, LGAD characterization
- **Syracuse University**: Silicon simulation (TCAD), characterization and performance study with picosecond timing electronics
- **Rice University**: LGADs sensor TCAD simulation and characterization
- **UNM**: LGAD characterization and radiation damage effects expertise

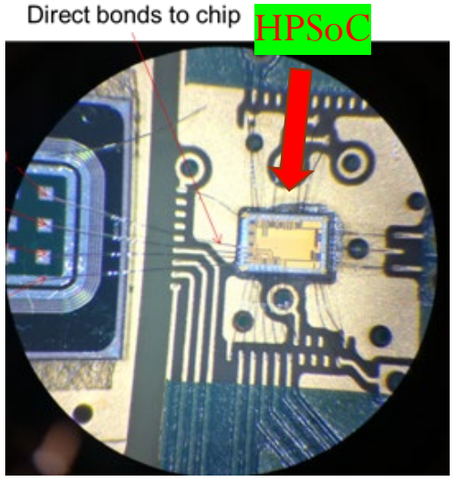


Sensor
- Characterization
- Fill factor
- Fast timing
- Radiation hardness

Integration
- Bump bonding
- Wire bonding
- Advanced integration



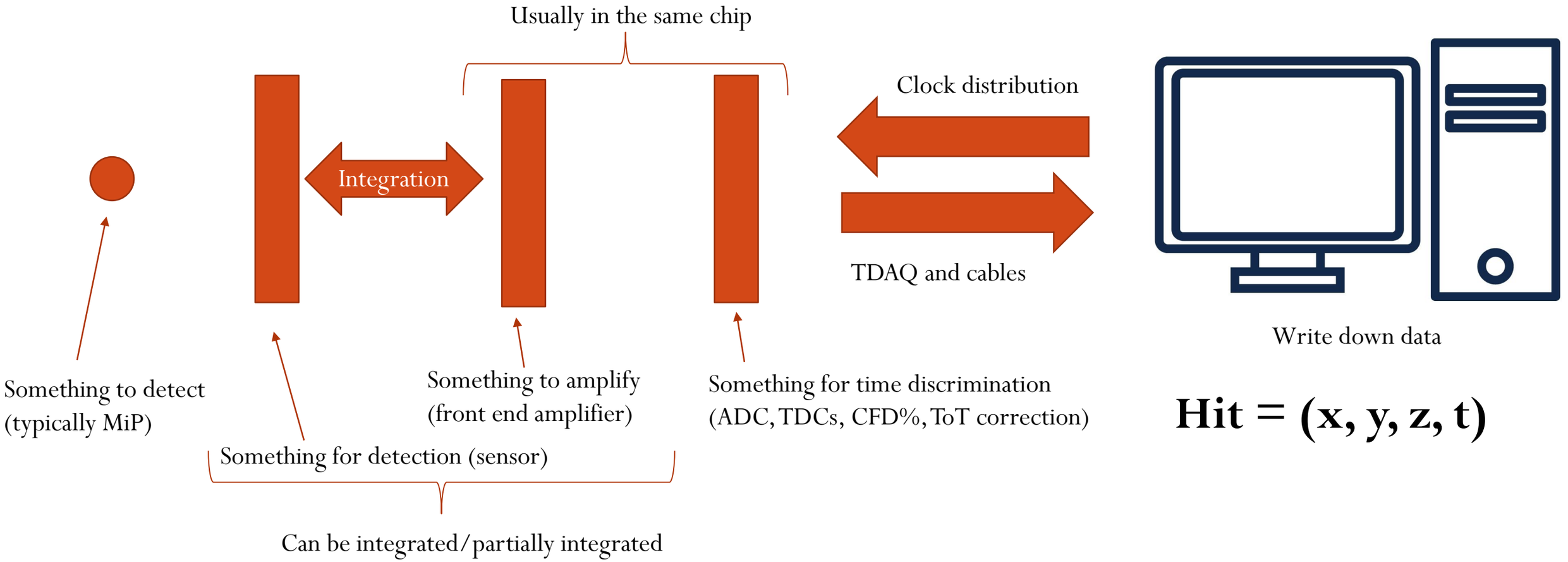
Readout chip
- Fast amplification
- Digitization
- Reconstruction
- Power requirements



The questions we seek to answer are:

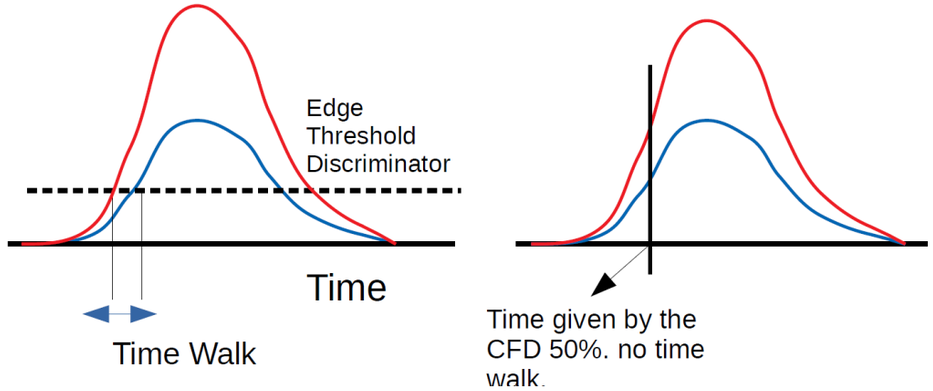
What is the achievable limit of time resolution, and what's the limiting factor? How thin can the device be without excess material (minimal material budget)?

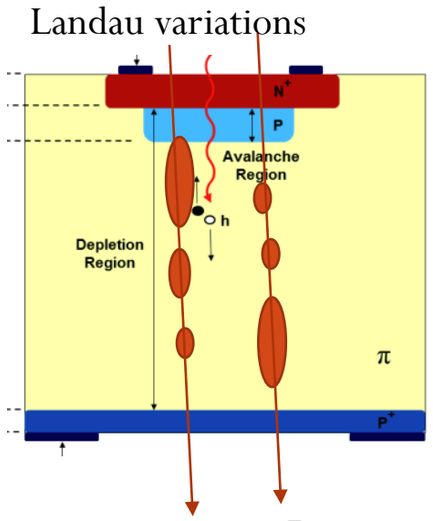
Another important goal of this collaboration is identifying 4D/5D tracking applications outside NP and HEP and the application of the LGAD technology to calorimetry by measuring the hit energy.

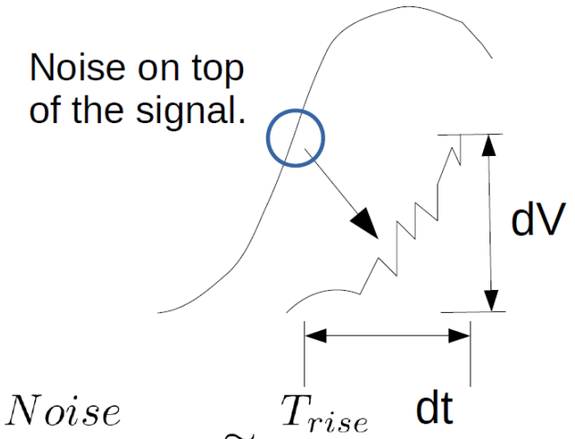


Hit = (x, y, z, t)

Time resolution







$$\sigma_{Jitter} = \frac{Noise}{dV/dt[CFD\%]} \approx \frac{T_{rise}}{SNR}$$

Sensor time resolution main terms

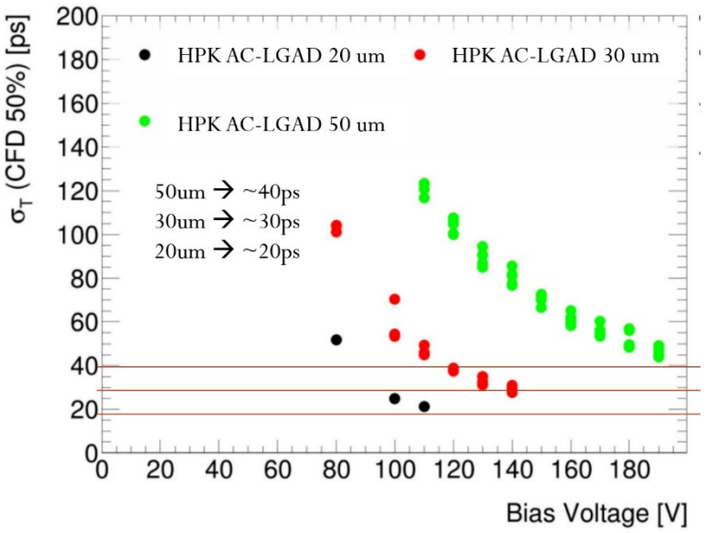
$$\sigma^2_{timing} = \sigma^2_{time\ walk} + \sigma^2_{Landau\ noise} + \sigma^2_{Jitter} + \sigma^2_{TDC}$$

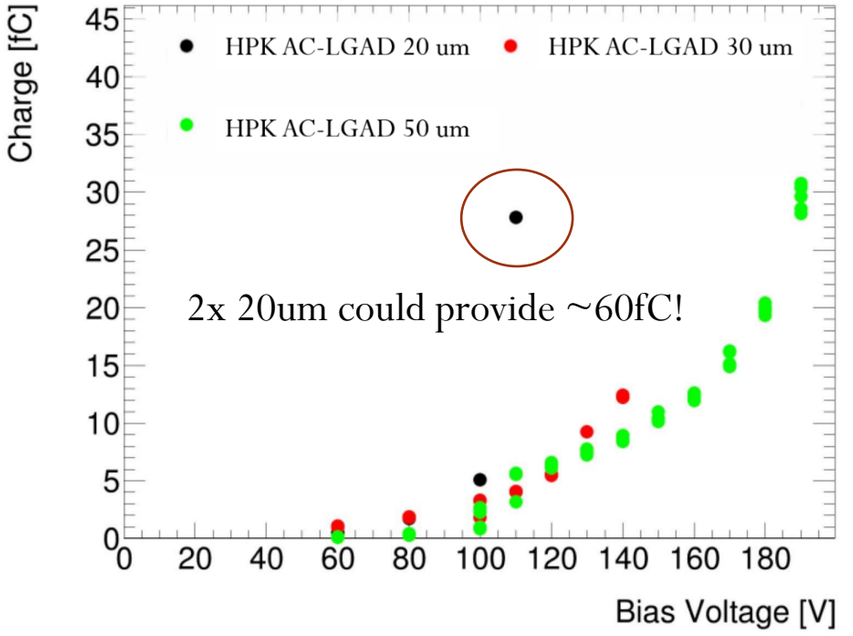
- **Time walk**:
  - Minimized by correcting the time of arrival using pulse width or pulse height (e.g., use 50% of the pulse as ToF)
- **Jitter**: from electronics
  - Proportional to $1/\frac{dV}{dt}$
  - Reduced by increasing S/N ratio with gain
- **TDC term**: from digitization clock (electronics)
- **Landau term**: proportional to silicon sensor thickness
  - Reduced for thinner sensors
  - Dominant term at high gain
- Why better timing?
  - Improve pileup rejection
  - Increase limit of ToF PID

Pushing the time resolution limit – sensor

- **Thinner detectors with high S/N maximize time resolution**
  - However, 20um LGADs are fragile and struggle to get to the required S/N unless very close to the breakdown
- In general LGADs also have limited gain, at high voltages gain suppression kicks in

- Solution: fabricate a thicker device that behaves as a thinner sensor
  - **Multi-gap LGAD**, inspired by multi-gap RPC
  - (A Rice U. and UCSC idea)
- **Proof-of-concept ongoing!**

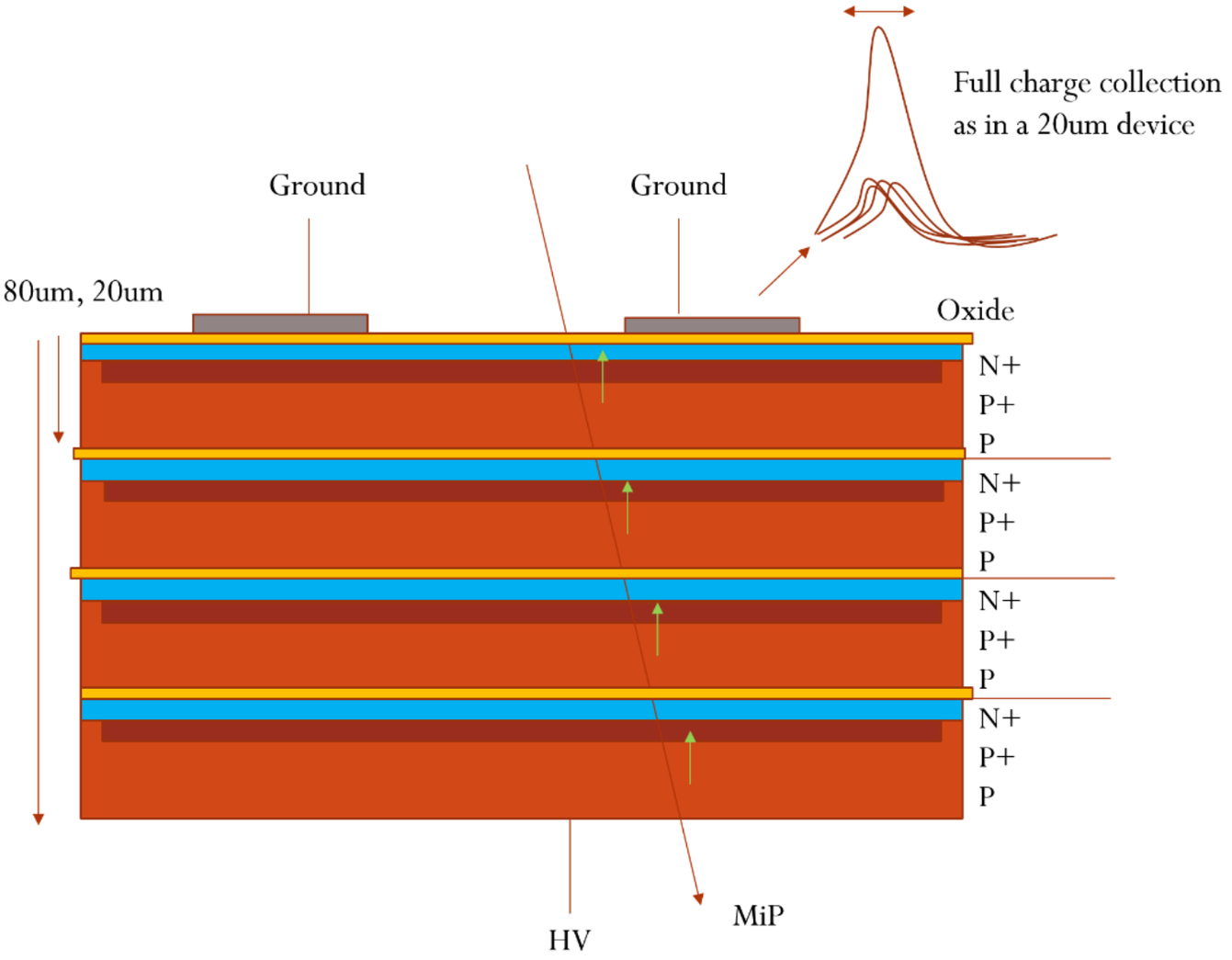




Multi-gap LGAD

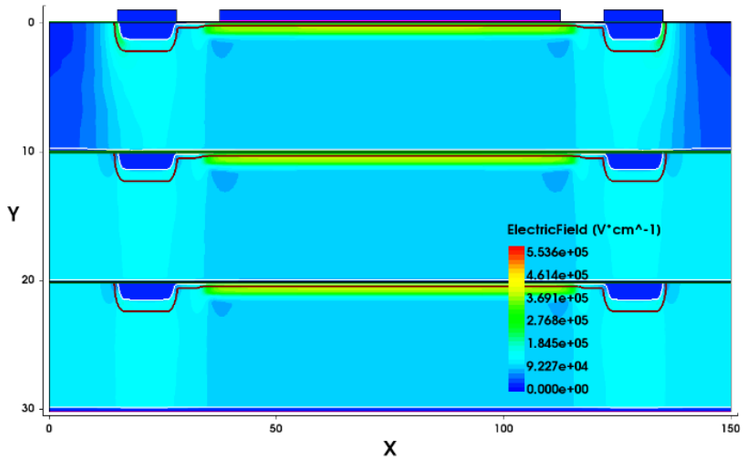
- Multi-gap LGAD is composed by several thin layers
  - Charge is induced on top via AC-coupling
  - Oxide layer in-between layers
  - N+, P+ have be resistive to make it work

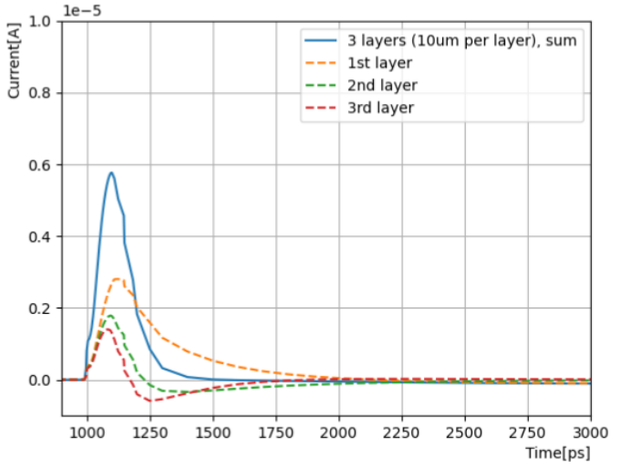
- Charge collection and multiplication parallelization
  - Faster rise time and charge collection
  - Charge is multiplied by the number of layers. In the example, if 20um sensor has gain of 10x, the total gain is 40x.
  - Charge is also higher than a single layer of 80um because there's less gain suppression (base charge is lower)
- High risk/reward device!



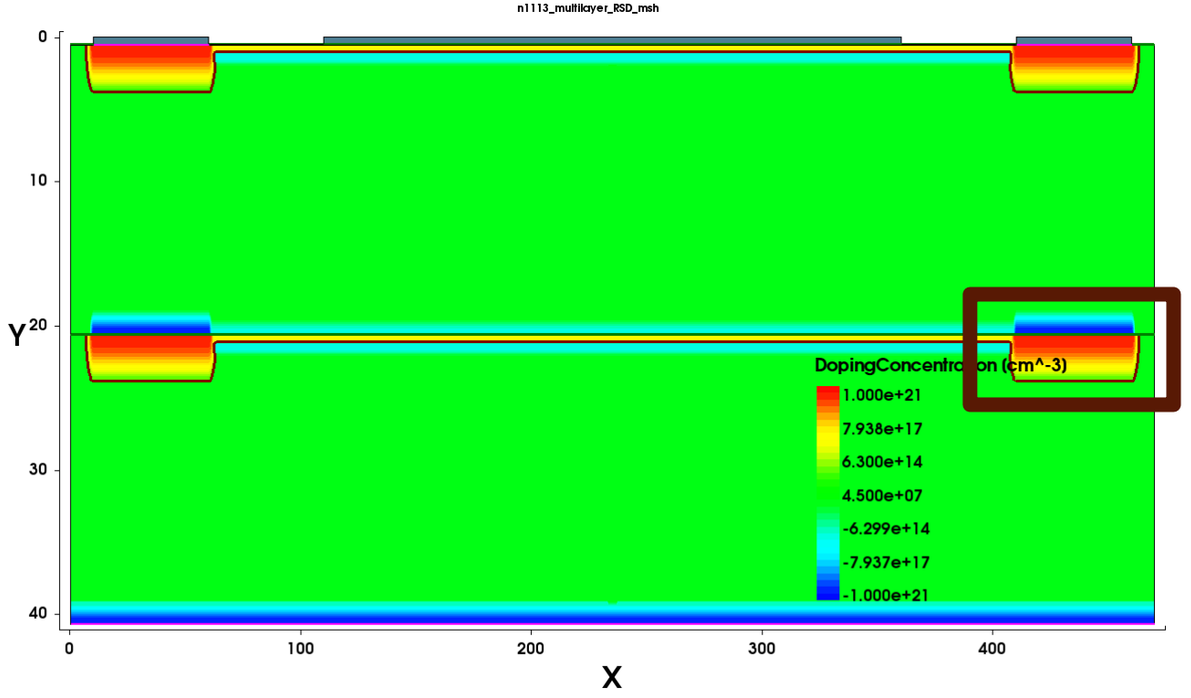
Preliminary TCAD simulations

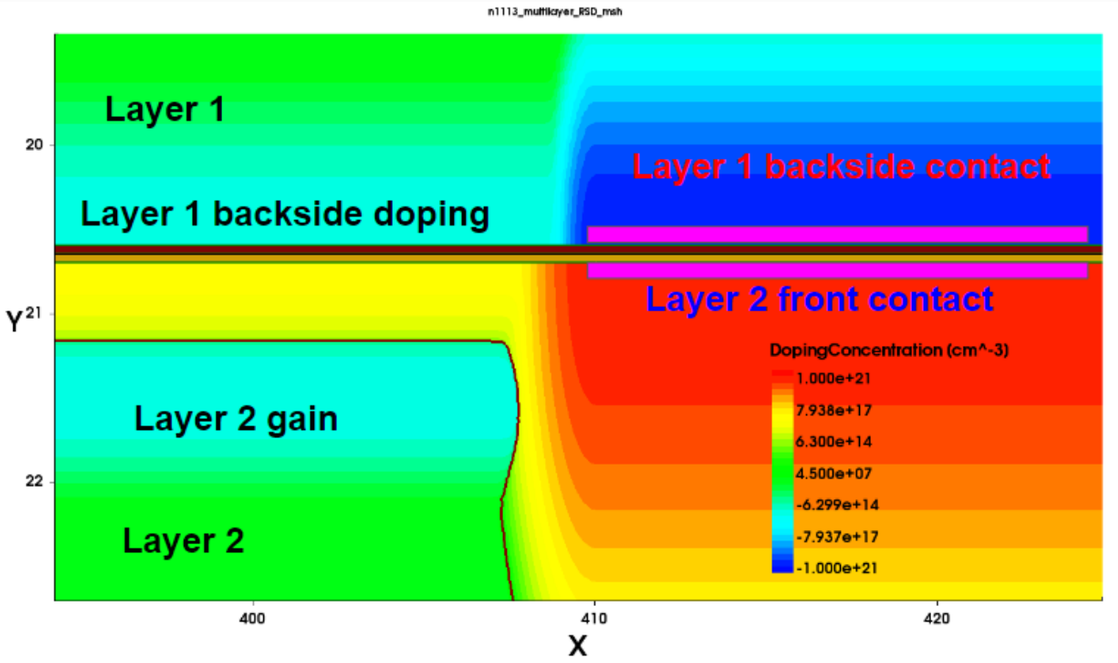
- The idea has been tested with TCAD simulations and there are promising results
  - 3x 10um layers, showing good signal induction on the top
- Current R&D path: finalize TCAD simulation and organize a first prototype production
  - Currently simulating the effects of the doping in the several layers on signal transfer to the surface
- We reached out to two industry partners expert in 3D integration that can produce such a device, production expense is compatible with year 2 and 3 of the funding cycle
  - Layers are produced with series of w2w bonding (low temp) and thinning
- w2w low temperature bonding was proved to be an effective way to produce LGAD devices
  - First DJ-LGAD prototype produced with w2w (https://indico.cern.ch/event/1132520/contributions/5140036/)
  - Advanced 3D integration is, in general, a very important topic to pursue for our community!

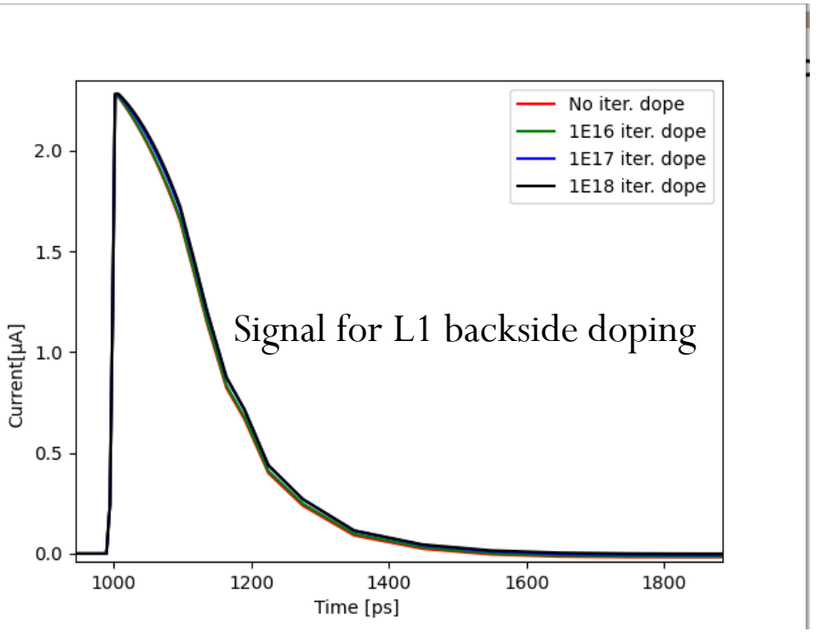




2x 20um device

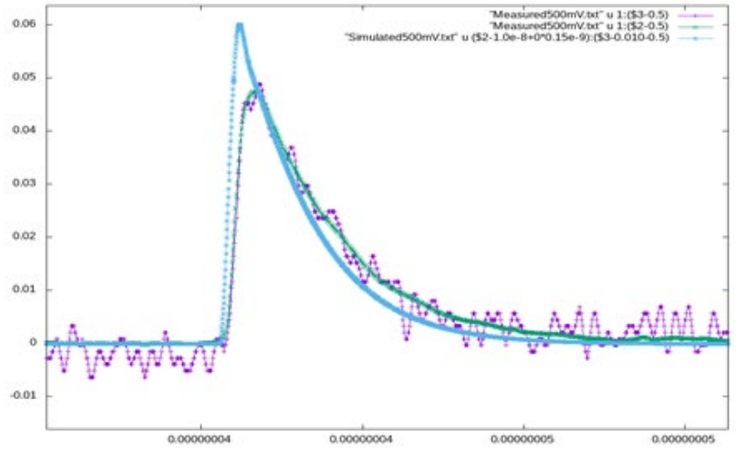


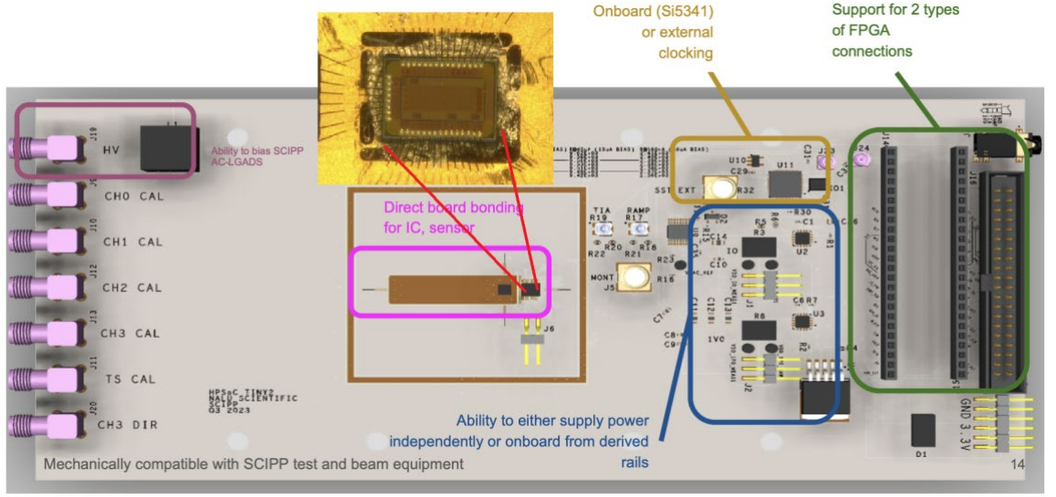




Pushing the time resolution limit – electronics

- The path to 10 ps time resolution is even harder for a 'large channel count' integrated electronics
  - Low power full waveform digitization might be a viable solution
- NALU scientific is collaborating with UCSC (HP-SOC) and Syracuse for the development of frontend chips for fast timing using full digitization
  - UCSC also developing a SiGe IC with industry and FAST3 chip with INFN Torino
- Effort funded separately but with great synergy

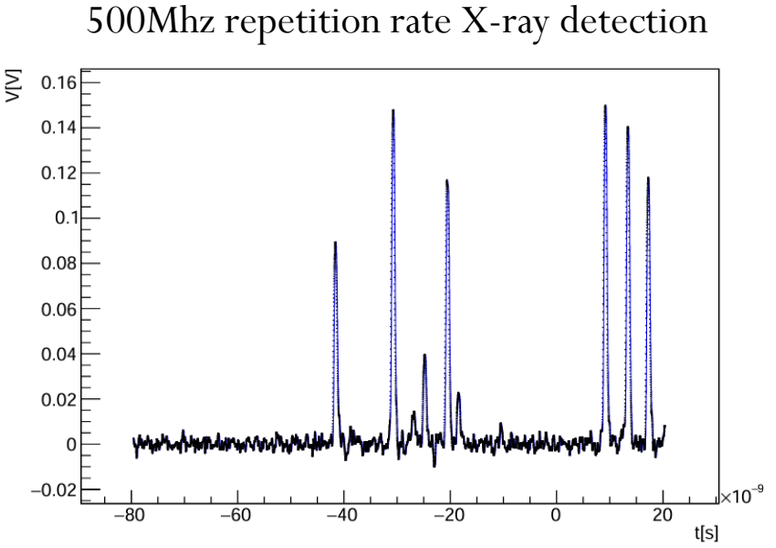


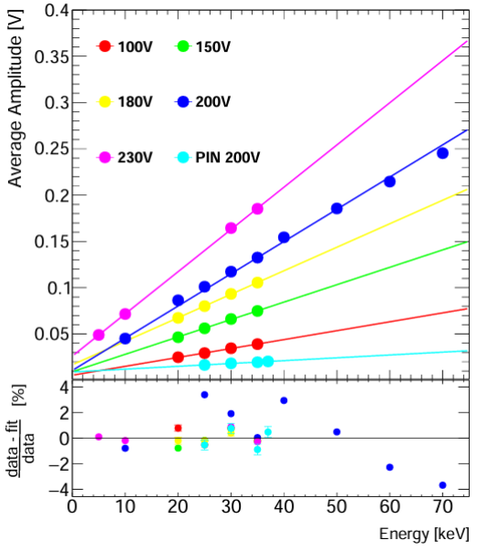


Timing applications in other fields

- LGAD technology can be applied to HEP, NP, space…
- X-ray physics is also a very interesting field
  - LGAD are thin (good for repetition rate), with gain (can detector low energy X-rays, even sub-KeV)
- Multi-gap LGAD allows for the fast repetition rate detection of low energy X-ray while maintaining a high rate of detection

- Same w2w bond technique for sensor development can be used to produce devices used for UV/IR photon detection
  - APD/LGAD featuring highly engineered deep junctions, compatible with black silicon on the entrance window for 100% QE for photon detection from UV to near IR (RDC2)
  - Investigation of Epitaxial growth for production as well





https://iopscience.iop.org/article/10.1088/1748-0221/18/10/P10006

R&D Plan and funding

- The R&R plan is to start the first with studying the feasibility of a multi-gap LGAD design using TCAD simulation
  - The support needed for engineering time is well within the budget constrains (~100k$)
- At the same time, investigate the general use of w2w bonding for LGAD fabrication, budget can't cover a production yet but can support feasibility studies
- At the same time, minor support for ongoing fast chip development independently funded
- **Deliverable**: multi-gap and engineered deep junction LGADs designs investigation using TCAD simulation
- **Deliverable**: continue investigation of timing chips

- Second and successive year: increase over 200k$ for the fabrication of a prototype multi-layer device
  - Ideally one sensor or one chip production per year after year 1, and then characterization activities are performed year-round
  - A new sensor or chip technology typically requires 2-3 years for a first working demonstrator; therefore, it fits well in the 3/4-year timeline of the funding call
- **Deliverable**: multi-gap and engineered deep junction LGAD prototypes
- **Deliverable**: sensor + readout system with improved time resolution
- **Deliverable**: expand applications of LGADs outside NP and HEP

RDC involved

- **RDC3**: Solid state detector development (multi-layer LGADs)
- **RDC11**: Pushing the limits of time resolution
- **RDC4**: Readout electronics and integration (low power, good timing)
- **RDC9**: moderate spatial resolution/high time resolution LGADs for calorimeter and time of flight applications
- **RDC2**: photon physics (X-ray detection)

Backup

4D/5D technology for future trackers – why LGADs?

SCIPP
SANTA CRUZ INSTITUTE FOR PARTICLE PHYSICS
UC SANTA CRUZ

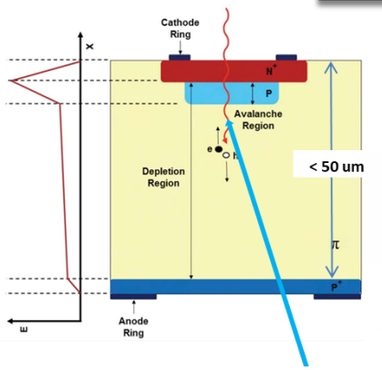
Need very small pixels: (e.g. 50k pixels/cm^2)

Thin sensors are required for very good time resolution
Thin sensors need gain!

- **Basic research need (BRN) requirements for future trackers**
- Spatial resolution ~ 5 um
- **<u>Temporal resolution ~ 10 ps</u>**
- Very low material budget (sensor + elect. < 100 mm of silicon)
- Very low power consumption (air cooling < 0.2 W/cm2)

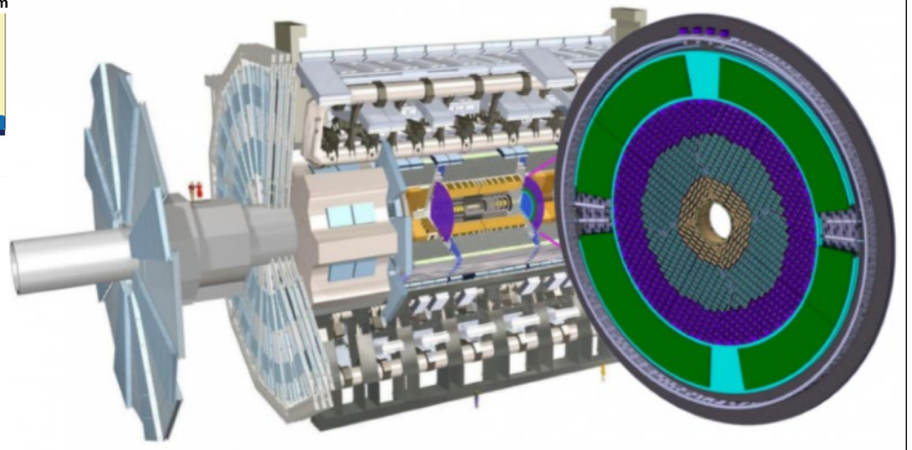
Good temporal resolution requires a lot of power per pixel: minimize # of channels!

- Low-Gain avalanche detectors (LGADs)
  - Example of blue-sky R&D within RD50, AIDA, supported by the US DoE (US-Japan)
- First prototype in 2012, now produced by >10 companies/labs
  - In 2019/2020 ATLAS and CMS submitted TDRs for large-scale timing upgrades to suppress backgrounds using LGADs with area of ~10 m^2
- Issues: granularity (almost solved), radiation hardness (good up to several 1E15Neq), power dissipation (issue for electronics), **time resolution limit at 20ps**



LGAD, Silicon sensor with thin gain layer to boost S/N

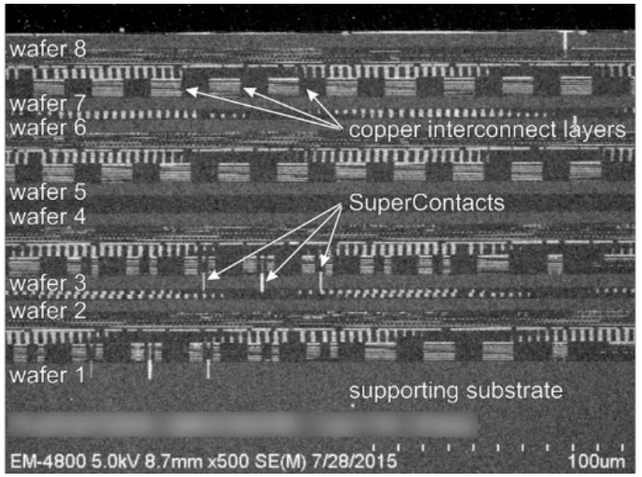
<u>ATLAS HGTD</u> <u>CMS ETL</u>



Snowmass papers: <u>4D tracking paper</u>, <u>CMOS</u>, <u>Electronics</u>, <u>SiC</u>, <u>3D integr.</u>

Pushing the time resolution limit – integration

- **3D integration** technology in industry currently allows tight packaging of sensor and chip
  - Improves sensor to chip connections in many ways
  - Additional aid to reach the goal of 4D tracking
  - https://arxiv.org/abs/2203.06093
- Not currently available in HEP, we need a community effort to make it available
  - Currently pursued by few groups together with small companies through DoE SBIRs



- **Very fine pitch** bonding (down to ~3 μm)
- **Better connection:**
  - Connections are shorter and faster than in circuit boards with long traces
  - Shorter connections also have reduced dissipated power
- **Better performance**: reduced input capacitance and lower noise
- **Integration of heterogeneous materials or different wafer technologies**
- **Reduction of single layer thickness**, after integration all supports can be removed
- See white paper https://arxiv.org/abs/2203.06093