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Functional Requirement Specification
LLRF Functional Requirements Specification (FRS)
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IIFC Approvals

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Table of Contents

1. INTRODUCTION

The Low Level Radio Frequency (LLRF) system is responsible for controlling the amplitude and phase of the RF fields in each cavity of the accelerator, providing a frequency reference for timing systems, and for providing frequency references to instrumentation systems. Additionally the LLRF system is responsible for providing resonance control of RF cavities. The PIP-II accelerator is divided into 3 frequency sections: 162.5 MHz, used by the warm cavities and the eight SRF Half Wave Resonantors; 325 MHz, used by the SRF Spoke Resonantors; and 650 MHz SRF elliptical cavities that comprise the rest of the accelerator. Most cavities will require the option of running the RF in either continuous wave (CW) or pulsed mode. The LLRF system will also provide a beam synchronous reference to the Chopper Program Waveform Generator (CPWG), which is also responsible for synchronizing linac beam with the Booster RF system and is covered in a separate FRS.

2. LLRF SYSTEM SCOPE

- Provide distributed phase-locked reference signals at 1300 MHz (for instrumentation), 650 MHz, 325 MHz, and 162.5 MHz.
- Provide amplitude and phase control of the RF field in the 162.5/325/650 MHz cavities
- Provide resonance control for the 162.5/325/650 MHz cavities
- Provide RF synchronous clocks to the global accelerator timing system
- Provide the RF signals of cavity probe and reflected power to the Station RF Protection Interlock (RFPI)system
- Provide RF status to the Machine Protection System (MPS)
- Provide scalar and waveform data to the control system
- Provide circular buffered data for beam loss or other machine fault diagnostics
- Provide operation in both continuous and pulsed mode

3. KEY ASSUMPTIONS, INTERFACES, AND CONSTRAINTS

3.1 Assumptions:

Accelerator Control System Core Services

- Alarms: The ability to view and display alarms available is required. An alarm server that interprets RF system alarm information in the context of operating mode is required to produce meaningful RF alarms.
- Data Archiving: Data archive capabilities similar to what is in existence (EPICS collaboration) now are required to support fault analysis, component lifespan analysis, overall system performance, and system interoperability studies (e.g., interactions between RF system and energy locks). Waveform archiving to provide a time history of waveform data (history buffers) collected by the low level RF system is required.
- Data Save and Restore: Data associated with a machine configuration must be saved and available for restore to the front-end computer in order to reestablish the RF parameters for a particular accelerator operations configuration (e.g. 60 MeV beam operations and the various beam currents).
- The ability to periodically save and restore RF control parameters must be available either automatically or on-demand in order to recover the RF system after a front-end computer reboot or LLRF system reset.
- RF High-Level Functionality Applications: Applications that consider the behavior of all of the cavities as a system or its interaction with other systems such as the following notable examples are required.
  - An application similar to Krest (CEBAF), which is a beam based tool that ensures the cavities are operated on crest (beam phase is the same as the cavity phase) by performing cavity-by-cavity and zone-by-zone phasing is required. In the case of the PIP-II LINAC the program will need to be able to set the cavities at the appropriate phase off of crest to meet the beam dynamics needs.
  - Applications similar to LEMi (LINAC Energy Management for the Injector) and LEM are required to set up the optics lattice and to distribute desired energy gain across a LINAC segment taking into

account operational drive highs limitations, cryogenic heat load considerations, fast and slow energy lock cavity headroom requirements, cavity trip rate models, cavity operational state, etc.

– RF performance analysis tools similar to the RF Fault Counter, Cavity Status/History, RF Analyzing Tool (RAT), and gradient calibration are required to maintain and improve operability of the RF system. These tools shall have access to and respond to the LLRF lost gradient and lock flags as necessary.

3.2 Interfaces:

- Detailed interface descriptions will be provided in the technical requirements specification for each module
- Forward power, reflected power, phase reference and cavity probe signals are provided from the beamline enclosure
- 1GB Ethernet line to the controls network
- Connection to the precision global timing clock (synchronized to the 162.5 MHz RF)
- Connection to the MPS system
- The global timing and MPS system will provide event signals to the LLRF system
- A beam synchronous and RF synchronous start trigger for pulsed mode operation. (divided down from 162.5 MHz)
- LLRF provides a drive signal to the high level RF system through a fast RF switch controlled by LLRF and an external switch controlled by the RF protection system
- Connection cables to the resonance control tuner in the cryo-modules
- A control system interface
- Beam loading information from the CPWG
- Local RF monitor calibration panel as well as Piezo amplifier monitors

3.3 Constraints:

- Cost, time, and space constraints will be addressed in the technical requirements specification for each module

4. REQUIREMENTS

4.1 Cavity Amplitude and Phase Control

The primary responsibilities of the RF system are to first provide a global frequency and phase reference for cavity control, and to frequency translate between RF and IF where signal processing/control takes place. The RF system must be highly linear, stable, and must support a large dynamic range with a low noise floor. Precision monitoring is critical for calibration and diagnostics.

The Digital IF Processor digitizes the IF signal provided by the RF system and applies FPGA-implemented digital signal processing and control algorithms to regulate the cavity field. The digital output from the IF processor drives digital to analog converters to produce the IF output signal, which is returned to the RF section. The resonance control system is comprised of the stepper motor driver, the Piezo amplifier driver, and a digital FPGA card. The resonance control chassis drives the cavity tuner. The cavity tuner combines the motion of a stepper motor and Piezo actuators, which perturb the cavity geometry in order to maintain the cavity resonance frequency within the specified tolerances.

In general, a Self-Excited Loop (SEL) and a Generator Driven Resonator (GDR) mode shall be available. The current digital IF processor system uses active feedback and feed forward control which shall be used as a basis

for the PIP-II design. Future control schemes involving beam-based feedback and other forms of control may be implemented in the LLRF on-board controller.

A simulator-on-chip shall be available for diagnostic purposes. It is still in review whether this will be on the same controller or implemented as an additional, plug-in module.

- The system shall provide diagnostic tests for the control loops to confirm correct operation
- In the case of a fault, the control system shall be able to handle a shutdown without damaging the machine or the LLRF system
- The cavity control system shall be able to keep phase and amplitude regulation down to 0.01 deg and 0.01% respectively with beam-based feedback after an initial settling time of 20 microseconds.

4.1.1 Additional MO, LO, and PRL, System Requirements:

The PIP-II RF Distribution System shall implement all the requirements outlined in this document.

- A programmable divider ratio output from the 162.5 MHz source shall be provided to the Accelerator global timing system. Three spare divider channels shall be available for future expansion.
- Each 162.5 MHz, 325MHz, and 650MHz phase reference signals delivered to the LLRF system should not drift from each other by more than 0.1 degrees per day with a maximum of 1 degree integrated seasonal drift.

4.1.2 LLRF Control System Interface

The distributed control system software running on the front-end computers shall serve a supervisory role in the system acting as a window into the LLRF control system. Requirements for the LLRF control system interface are listed below.

- The LLRF system shall interface with the global control system used in the rest of the accelerator.
- The LLRF system shall be capable of interfacing with multiple control systems, such as ACNET, EPICS, and Labview.
- The LLRF system shall be capable of providing forward power, reverse power, and cavity gradient waveform history, pre and post trigger, with a 1μs or better resolution, upon receiving a fault trigger request from the clock/event system. This requires a circular buffer implemented in the LLRF controller.
- Debug software should be available for board verification and testing.
- It shall be possible to control/drive the stepper motor and piezoelectric cavity resonant frequency tuners through the accelerator control system or directly by the LLRF system. It shall also be possible to drive the Piezo amplifiers from analog inputs to the amplifiers.
- The LLRF system shall provide meaningful RF alarm flags to the global control system. The flags shall include, but are not limited to, forward power fault, cavity gradient fault, and power sum fault.
- The LLRF system shall be capable of retrieving setting history from the global control system upon power failure or system reboot.

4.1.3 LLRF Interface to RF Protection Interlock System

The LLRF output is controlled by the RF Protection Interlock (RFPI) system which turns off a GaS switch during fast trips. *The RF Protection Interlock (RFPI) System shall interface with the Low Level RF system using a number of co-axial cables.*

- The LLRF system shall provide a ready signal to RFPI system. The RFPI system shell provide a permit signal to LLRF system allowing LLRF to operate normally after the receipt of ready signal.
- The RFPI system shall turn off the GaS switch in event of trip condition. The same signal shall be provided to the LLRF system for information.

4.2 Resonance control:

The system shall provide compensation for Lorentz force detuning using a piezoelectric tuner (PZT) for pulsed operation. Each SRF cavity will contain several electromechanical tuners. Coarse tuning is accomplished using a stepper motor while fine control and control requiring fast response is accomplished using two piezoelectric actuators. The piezoelectric actuators are mechanically in series with the stepper motor. The Resonance Control Chassis (RCC) is capable of managing four SRF cavities comprised of four stepper motors and eight Piezo stacks. The main components are: one four-channel Stepper Motor Driver, four two-channel Piezo Amplifiers, and one FPGA based controller card.

- The CW Resonance Control shall auto-track and compensate for drifts in the cavity resonant frequency by purposefully deforming the cavity's mechanical structure.
- Mechanical and piezoelectric tuners will be used to maintain cavity frequency to within 1-2 Hz for the mechanical tuner and within 1 Hz for the piezoelectric tuner.
- It shall be possible to turn off auto-track mode to allow manual tuner adjustments. When auto-track is reengaged, it shall resume resonance tracking from the present tuner positions.
- During initial turn on the cavity will be driven in a self excited loop with amplitude regulation requirements relaxed to 5 %. There is no phase regulation requirement imposed.
- The LLRF control system shall configure and drive the tuners. The LLRF control system shall allow for manual control of the tuners through the accelerator global control system. The LLRF control system shall provide periodic updates of the tuner position, limit switch status, direction, etc. to the accelerator's global control system.
- There shall be supervisory control over the Piezo drive amplifier and stepper motors.

4.2.1: Stepper Motor Driver

Course tuning of the cavity is accomplished using a stepper motor control system. The stepper motor control system is comprised of stepper motor control board and control software. This specification defines the technical design and fabrication requirements for the stepper motor driver and control.

- The stepper motor control system shall drive the stepper motor based on the commands issued to it from the LLRF controller. The driver shall be capable of selecting the driver current, hold current, current cut back in idle mode, selectable micro-step size, inhibit mode etc..
- The stepper motor control system shall also read the status of limit switches with isolated signals. These limit switches shall prevent the stepper motor from driving any farther than the physical limits set on the tuner, thus preventing any damage that may be caused to the cavity or the tuner.
- A stepper motor thermocouple shall be incorporated into the stepper motor control system and shall provide monitor and interlock signals to the RFPI chassis.
- The stepper motor controller shall be able to relax compression on the cavities for system warm up and shall be capable of moving the cavity tuners to this safe state in the event of an unscheduled warm up or power outage.
- The stepper motor control system shall be capable of operating the stepper motors with and without holding current.

4.2.2 Piezo Driver Amplifier Module:

The Piezo Driver amplifier is part of the Resonance Control system within the Low Level RF system. The Piezoelectric-based resonance control system complements the wide tuning range of the stepper motor with low noise actuator that has a much narrower tuning range. The Piezo amplifier is driven by a feedback control loop capable of providing a ~120 Volt differential potential across the Piezo stack, and the required current to provide a large signal bandwidth while maintaining fidelity and noise performance similar to professional audio systems. The design requirements are itemized below.

- The Piezo driver amplifier module shall provide two channels of Piezo control signals.

- The Piezo driver amplifier module shall produce a maximum differential voltage range of 120V, with a maximum of ±50V to ground for each leg of the Piezo drive.
- The current of each amplifier leg and the differential output voltage shall be monitored by 16-bit ADCs and read back to the FPGA board.
- The Piezo driver amplifier module shall provide front panel output monitors to allow for system transfer function and noise measurements with traditional rack and stack equipment.
- The Piezo drive amplifier module shall be low noise drive to avoid excitation of high Q mechanical modes
- The Piezo drive amplifier module shall include current limiting to avoid mechanical damage or generate additional cryogenic heat load.
- The Piezo drive amplifier module shall have differential drive to reduce ground noise excitation of the piezoelectric tuner and to reduce voltage to ground.
- The Piezo drive amplifier module shall have isolators on all digital signals to reduce ground loops and provide input isolation.
- The Piezo drive amplifier module shall have two amplifiers per cavity to provide redundancy in case of amplifier or transducer failure.
- The Piezo drive amplifier module shall include output enable and over current protection
- The Piezo drive amplifier module shall include design ruggedness and high reliability
- It is possible for broadband noise from the controller and amplifier to excite mechanical modes in the cavity. For this reason, the SNR for the amplifier shall be a minimum of 115 dB (0.1 Hz to 1 kHz), with the most attention placed on noise near the cavity resonant frequencies.

5: PERSONAL SAFETY REQUIREMENTS

Electrical Safety - All modules will be closed so that there is no exposure to shock hazards. Output connectors will not have exposed contacts. LOTO procedures will be followed for any connect/disconnect of cables.

6: EQUIPMENT PROTECTION REQUIREMENTS

Machine Protection – The LLRF control system will be interfaced with the MPS and accelerator control system to allow for proper sequencing in the case of a fault. Proper sequencing scripts and system handling will be developed through discussion between LLRF, RF, Controls, and Operations. This interface will be provided through an SFP fiber connection using 8b/10b.