Fermilab | U.S. DEPARTMENT OF ENERGY | Office of Science

PIP-II LLRF Station

Philip Varghese

PIP-II LLRF Final Design Review

July 17, 2024

A Partnership of:
- US/DOE
- India/DAE
- Italy/INFN
- UK/UKRI-STFC
- France/CEA, CNRS/IN2P3
- Poland/WUST

OUTLINE

- Introduction
- LLRF System Architecture
- LLRF Stations Configuration for PIP-II
- Technical Requirements and Documentation
- Preliminary Design
- PIP2IT and STC Performance/Results
- Process to Final Design
- QA/QC Plan
- Summary

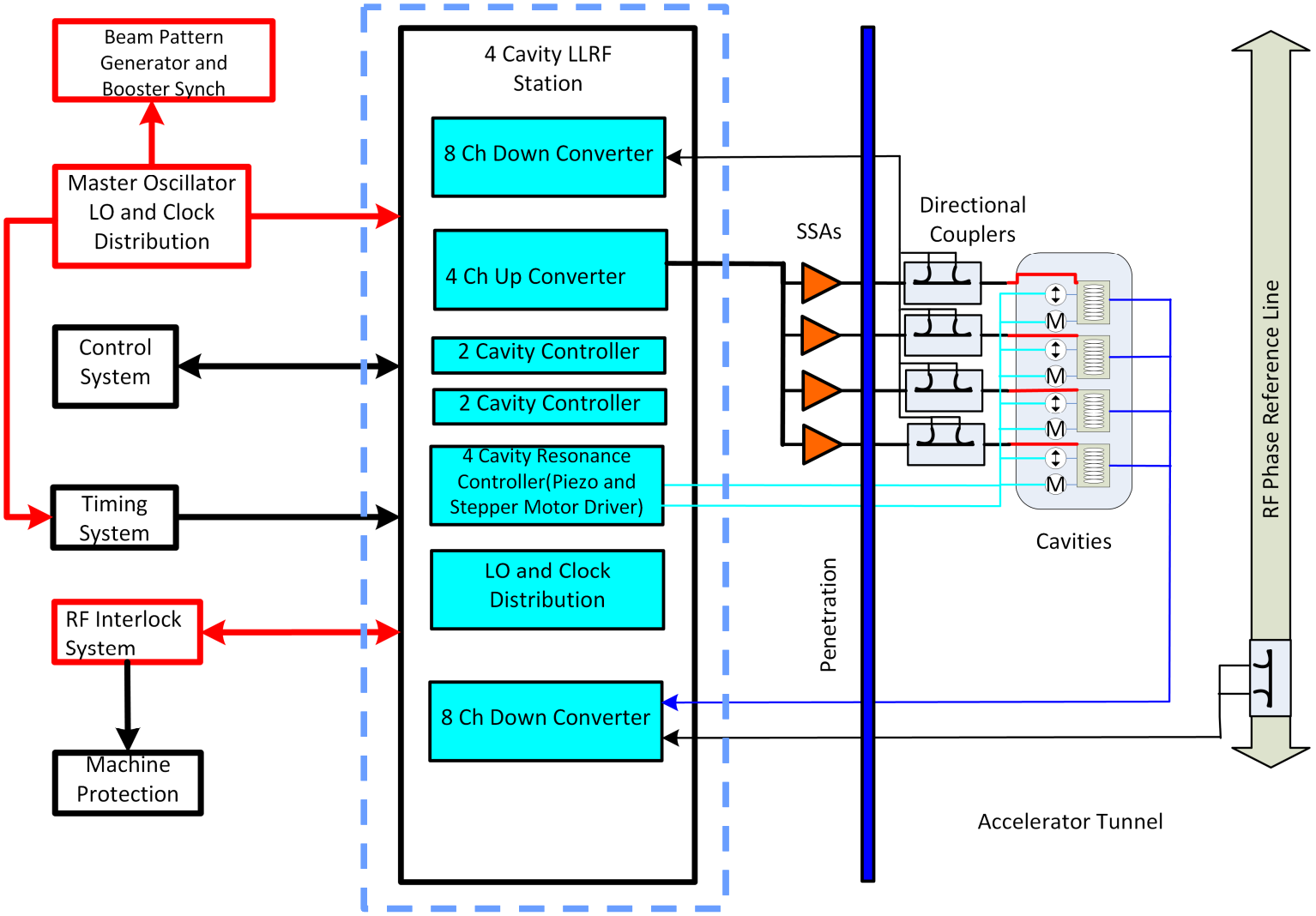
Introduction

- **Philip Varghese**
  - L3 Manager for LLRF and RFPI
  - Ph.D. Electrical Engineering
  - 30+ Years Experience, 22 Years in FNAL LLRF Group
  - >7 years of direct involvement with PIP-II

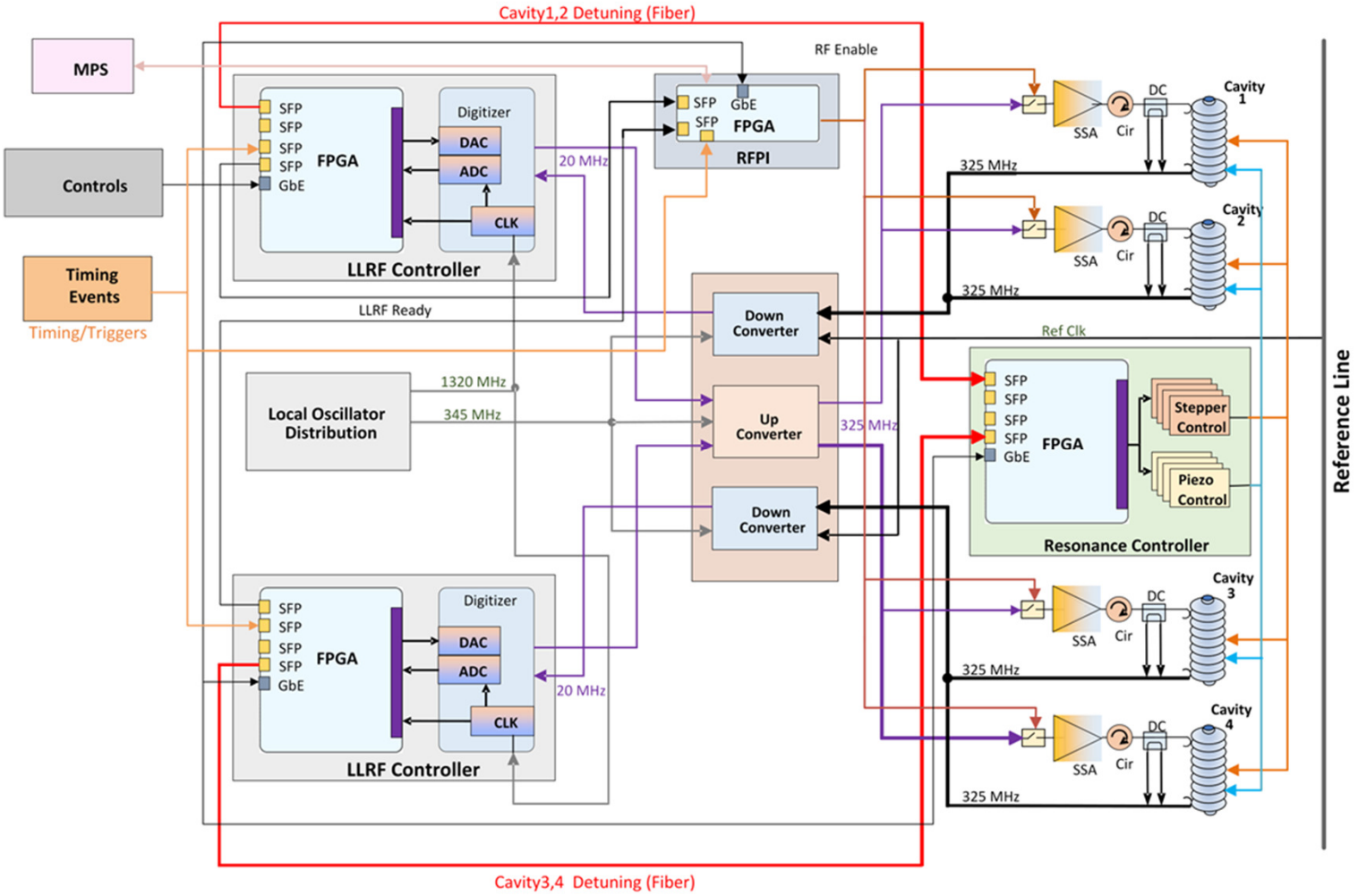
- Relevant Experience
  - Principal Engineer, LLRF Group Leader
  - Lead Engineer: PIP-II IT LLRF System design/testing
  - Lead Engineer: Design of 3 generations of FPGA based LLRF Hardware for SRF cavity control
  - Resonance control studies on LCLS-II cavities
  - FAST/IOTA cryomodule LLRF system design/commissioning
  - Experience working with various collaboration teams for PIP-II and LCLS-II Projects
  - Extensive experience developing various LLRF systems for normal and superconducting cavities

- Previous Relevant Experience
  - 12 years, Embedded Systems, Industrial Controls, Automotive Electronics

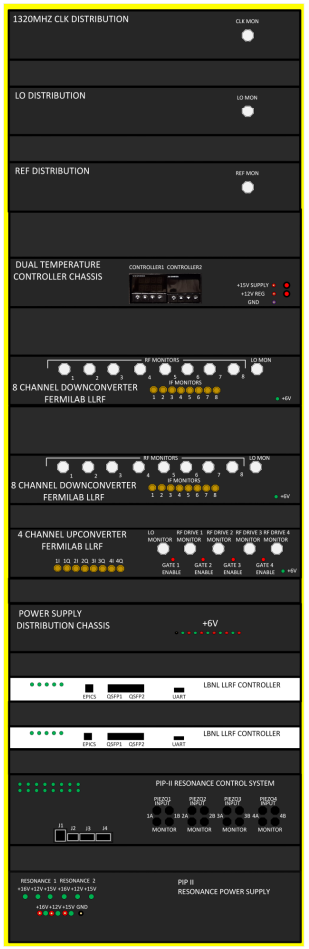
PIP2 4-Cavity RF Station



PIP2 4-Cavity RF Station



4-cavity LLRF Station Rack – Components 1



1320 MHz Clock Distribution

LO Distribution

Reference Distribution

Dual Temperature Controller

8-Channel Downconverter

8-Channel Downconverter

4-Channel Upconverter

UC/DC Power Supply

LLRF Controller

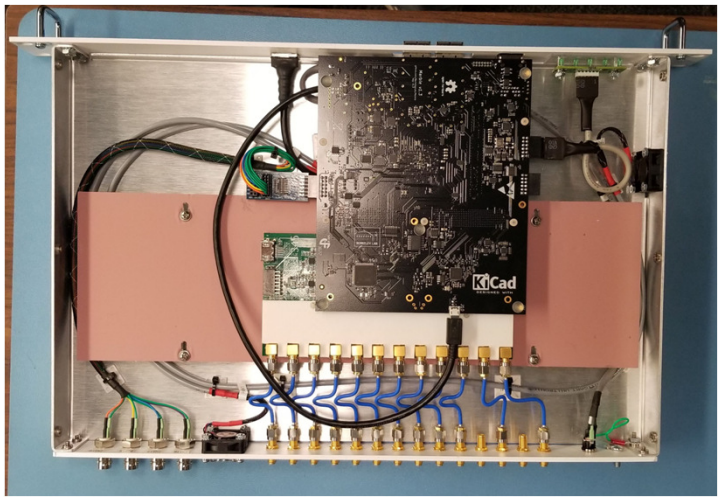
LLRF Controller

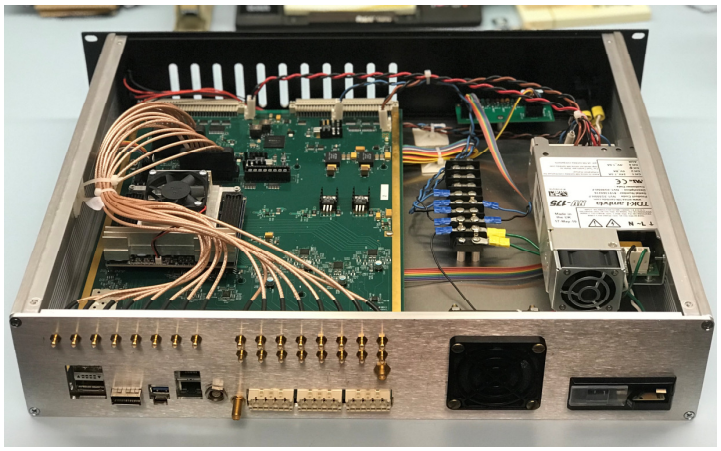
Resonance Controller

RCC Power Supply

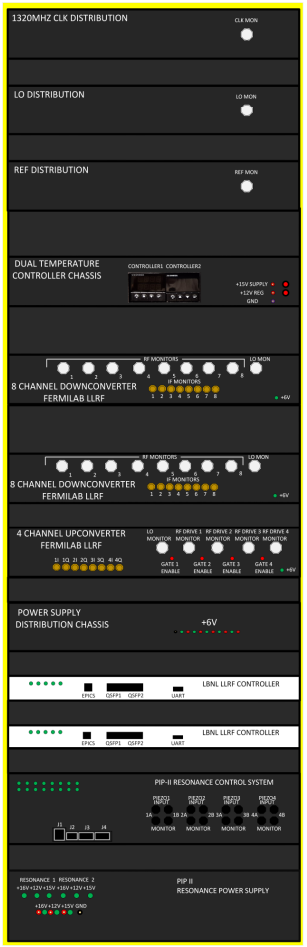
LBL-Marble RFS
Xilinx – Kintex

FNAL- LLRF Controller
Intel – Arria10 SOC





4-cavity LLRF Station Rack – Components 2



1320 MHz Clock Distribution

LO Distribution

Reference Distribution

Dual Temperature Controller

8-Channel Downconverter

8-Channel Downconverter

4-Channel Upconverter

UC/DC Power Supply

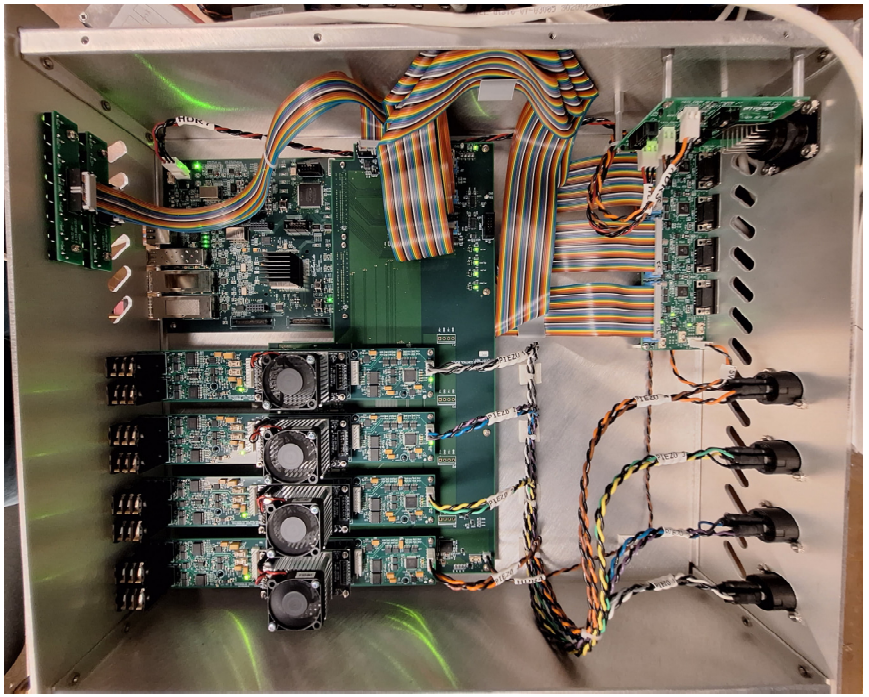
LLRF Controller

LLRF Controller

Resonance Controller

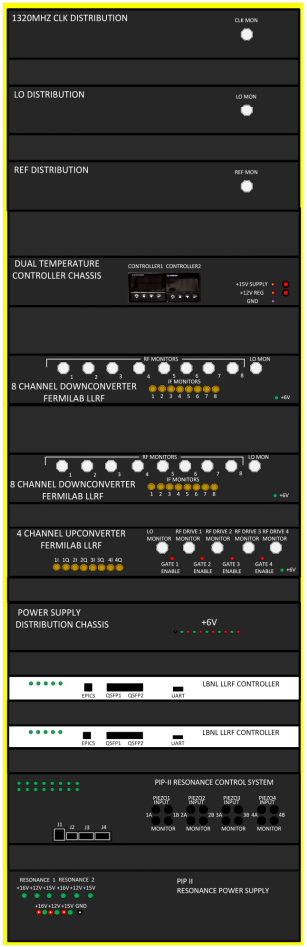
RCC Power Supply

JLAB/FNAL
Resonance Controller
(Marble FPGA)
Xilinx – Kintex



RCC Covered in James's talk

4-cavity LLRF Station Rack – Components 3



1320 MHz Clock Distribution

LO Distribution

Reference Distribution

Dual Temperature Controller

8-Channel Downconverter

8-Channel Downconverter

4-Channel Upconverter

UC/DC Power Supply

LLRF Controller

LLRF Controller

Resonance Controller

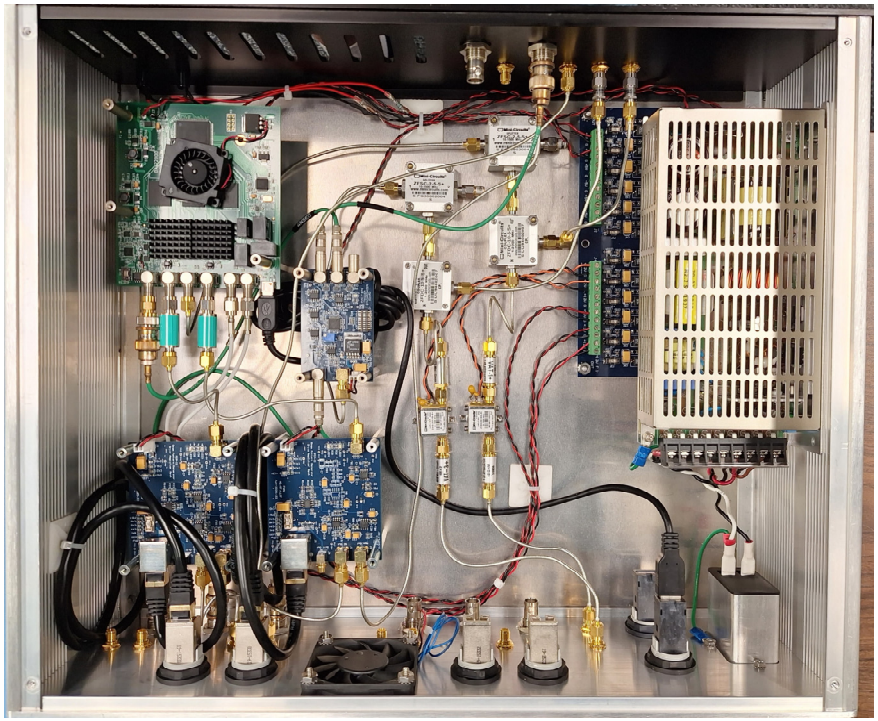
RCC Power Supply

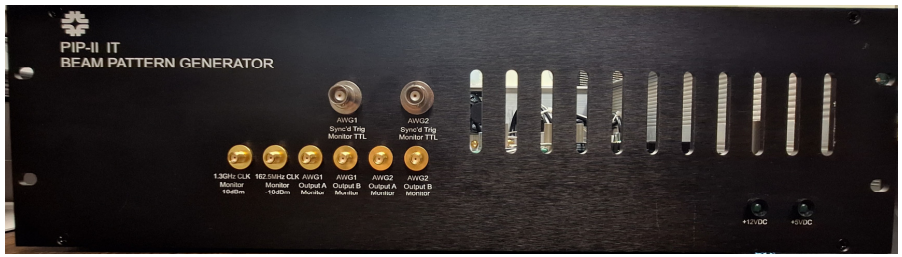
4-channel Upconverter

8-channel Upconverter

Covered in Ahmed's talk

Beam Pattern Generator Prototype





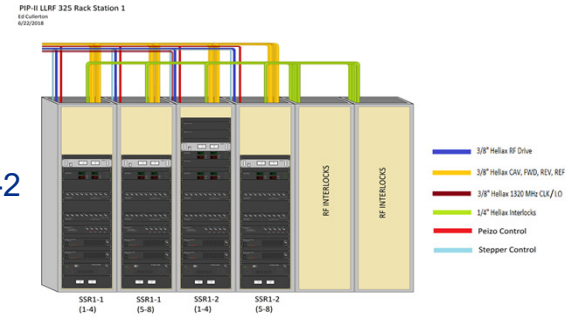
- BPG Upgrade project is underway
- Obsolete AWG hardware replaced with an Arria10 SOM and COTS DAC Board
- FDR in mid 2025

PIP-II Linac - LLRF Station Allocation

CM type	Cavities per CM	Number of CMs	CM configuration+	CM length (m)	Q_0 at 2K (10^{10})	Surface resistance, (nΩ)	Loaded Q^{Δ} (10^6)
HWR	8	1	8×(sc)	5.93	0.5	9.6 (2.75‡)	2.32
SSR1	8	2	4×(csc)	5.53	0.6	14 (10‡)	3.02
SSR2	5	7	sccsccsc	6.3*	0.8	14.4	5.05
LB650	4	9	cccc	5.52*	2.15	9.0	10.36
HB650	6	4	cccccc	9.92*	3	8.7	9.92

	Station 1	Station 2	Station 3	Station 4	Station 5	Station 6	Station 7	Station 8	Station 9	Station 10	Station 11	Total
	RFQ, B1-4	HWR	SSR1-1,2	SSR2-1,2,3	SSR2-4,5	SSR2-6,7	LB650-1,2,3	LB650-4,5,6	LB650-7,8,9	HB650-1,2	HB650-3,4	
Number of cavities	6	8	16	15	10	10	12	12	12	12	12	125
RF Freq (MHz)	162.5	162.5	325	325	325	325	650	650	650	650	650	

S3 – SSR1-1,SSR1-2



S4-S11 – SSR2 (7), LB650 (9), HB650 (4)

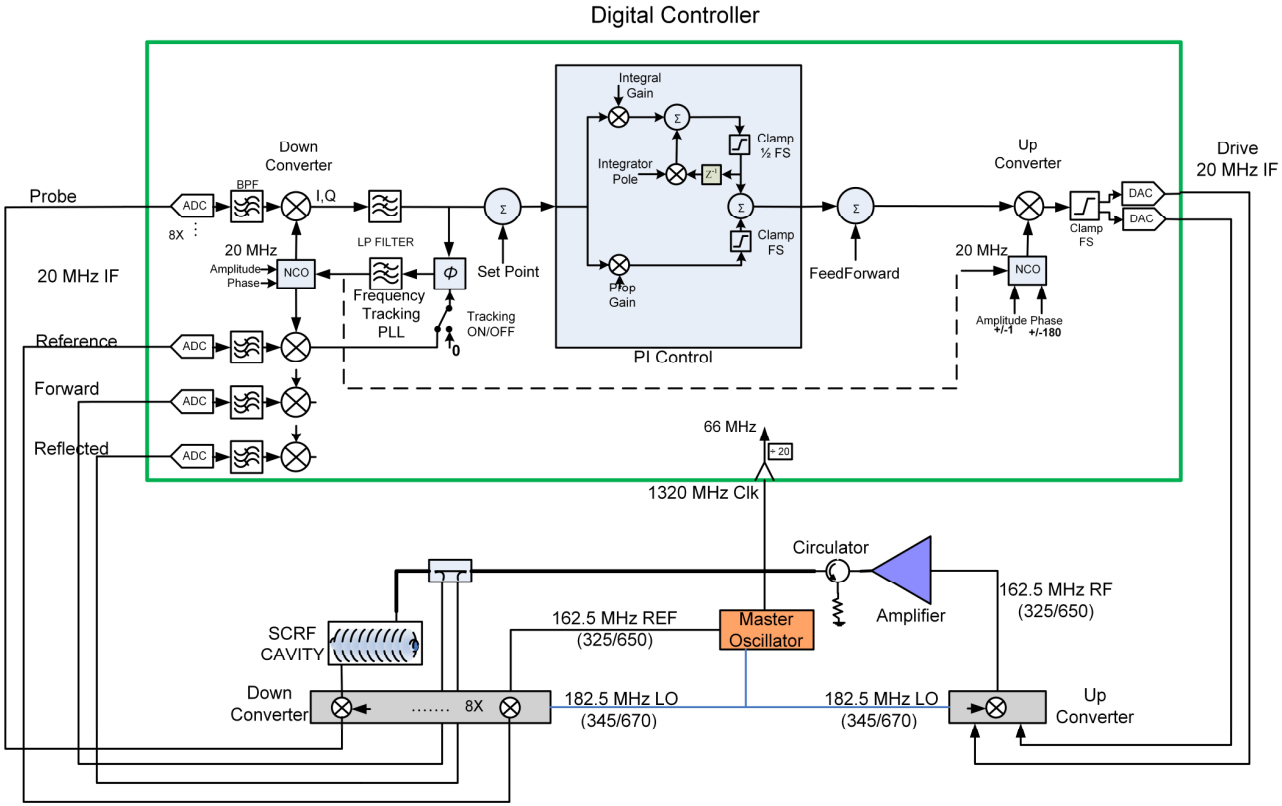
LLRF Station Requirements

- RF amplitude and phase control for 12-16 cavities per station
- Downconvert Cavity Probe,Forward and Reflected signals to 20 MHz IF
- Upconvert 20 MHz IF outputs to RF drive for SSA's
- Resonance Control for superconducting cavities
- Reference, LO and Clock distribution
- Power supplies, Temperature controllers for various chassis

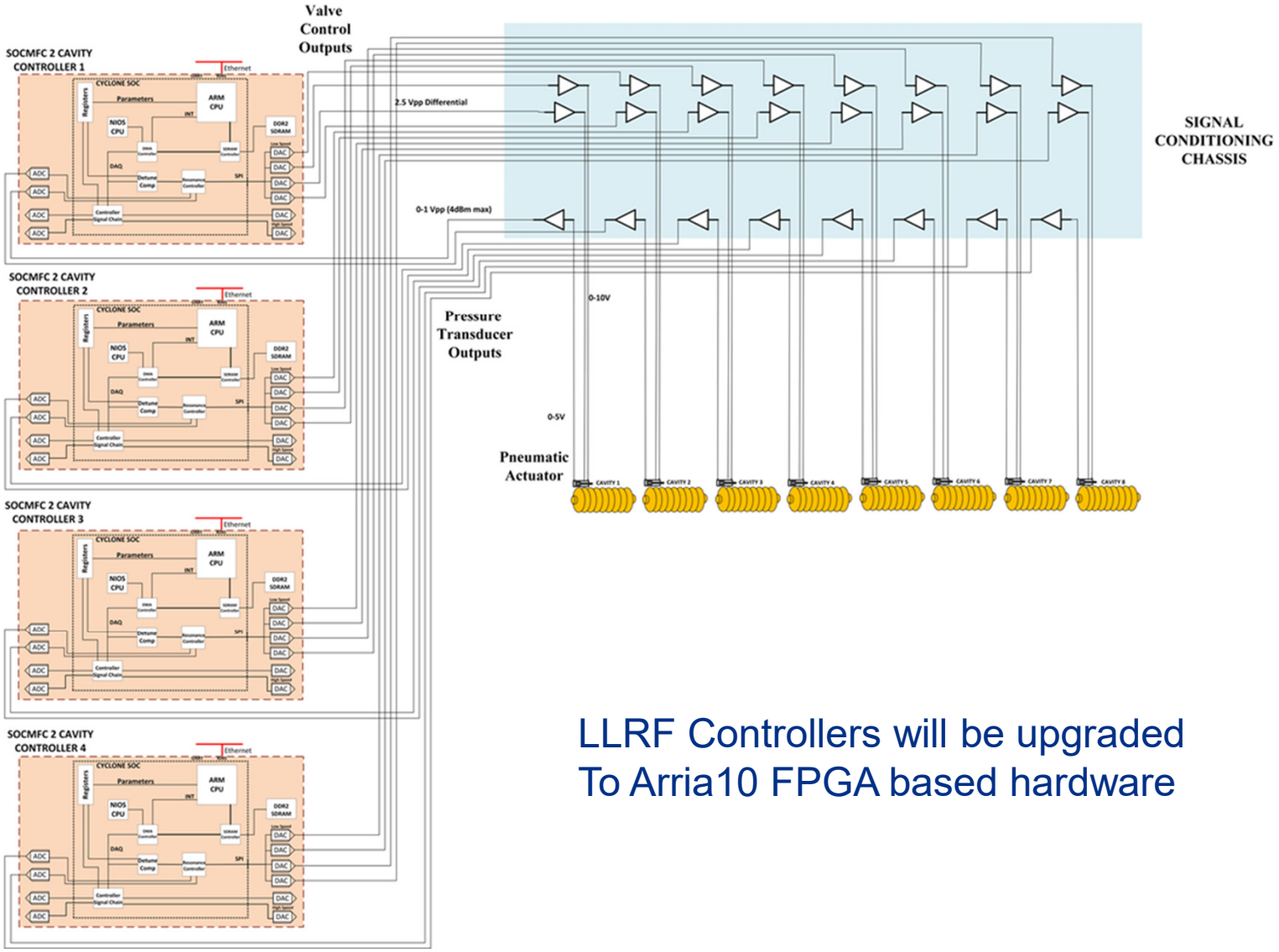
[1]	ED0011278	Technical Requirements Specification -FPGA Board
[2]	ED0011279	Technical Requirements Specification – ADC DAC Mezzanine Board
[3]	ED0005054	Technical Requirements Specification – Controller Chassis
[4]	ED0005782	Technical Requirements Specification – Resonance Control Chassis
[5]	ED0005166	Technical Requirements Specification – 8-Channel Downconverter
[6]	ED0005163	Technical Requirements Specification – 4-Channel Upconverter

LLRF Controller Design

- Tested during PIP2IT
- RFQ, B1-3, HWR and SSR1 were tested with beam
- PIP-II Amplitude, Phase regulation and Cavity Detuning specifications were met

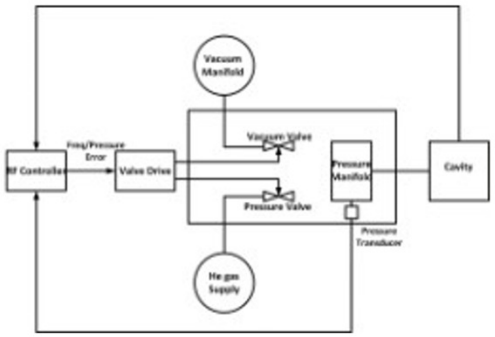


HWR Resonance Control at PIP2IT

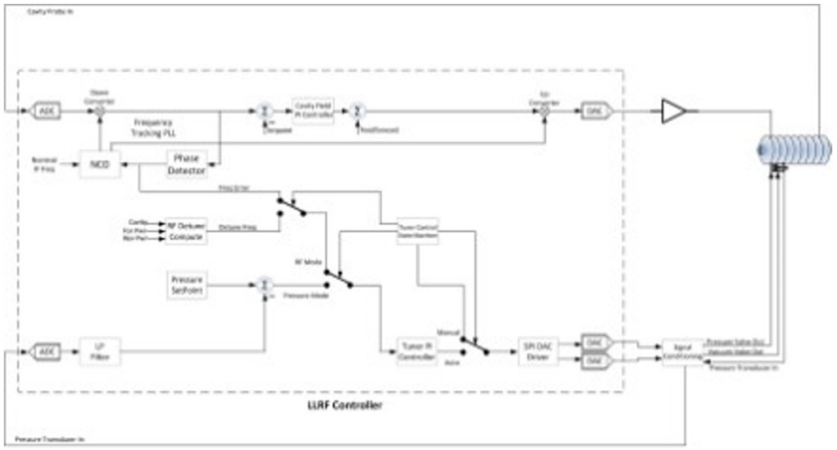


LLRF Controllers will be upgraded
To Arria10 FPGA based hardware

HWR Resonance Control Design

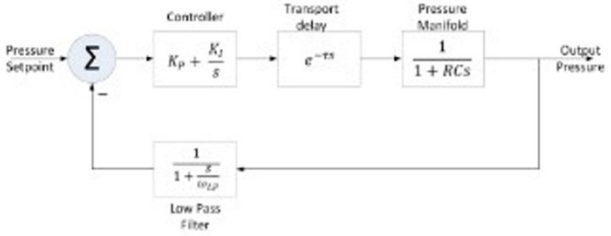


Physical Model

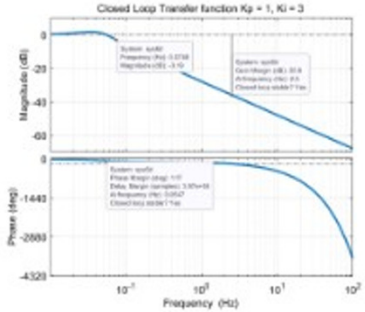


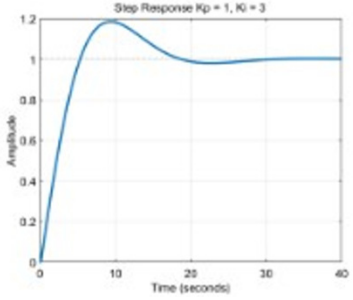
Controller Implementation

Control System Model

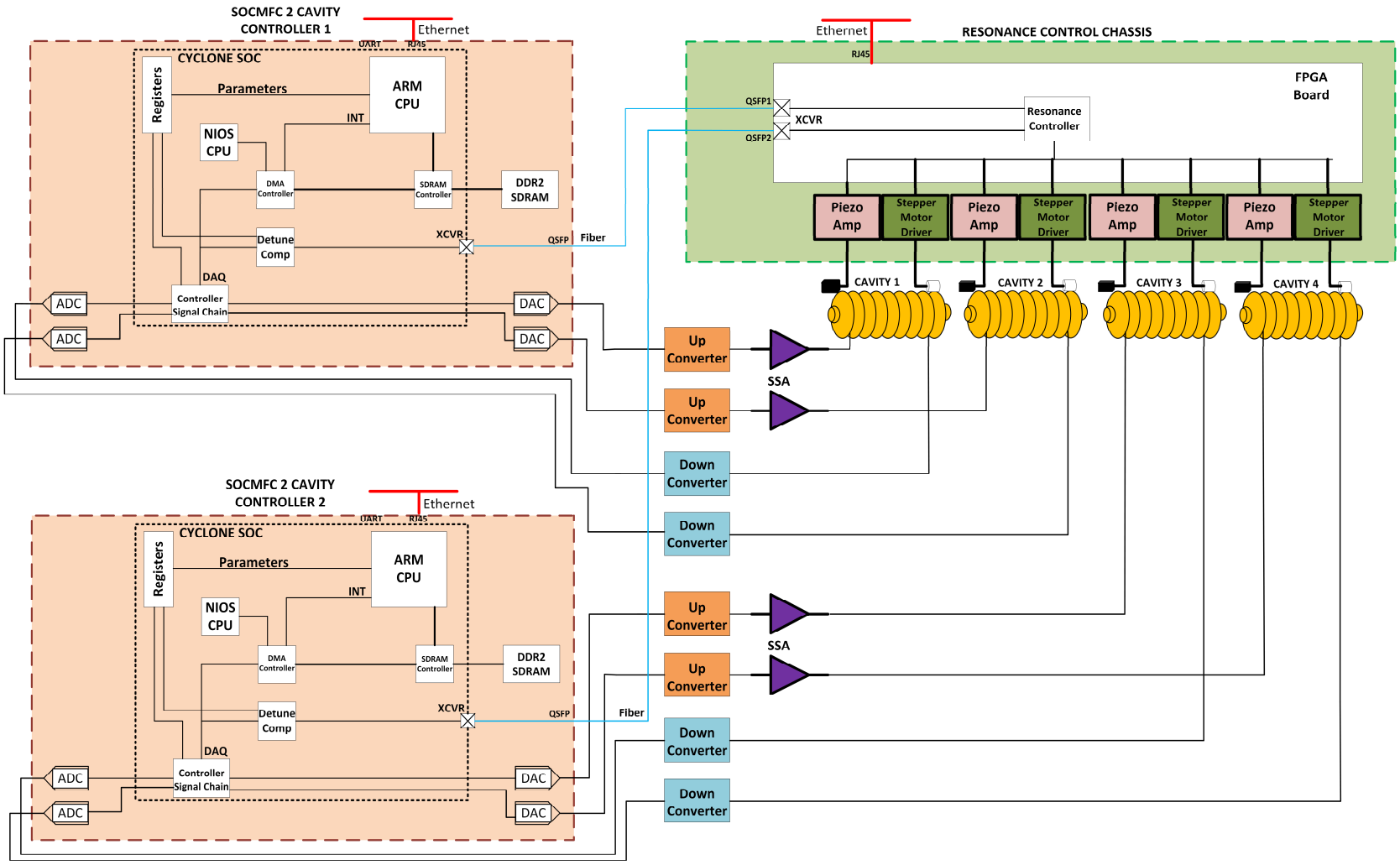


Control System Simulation



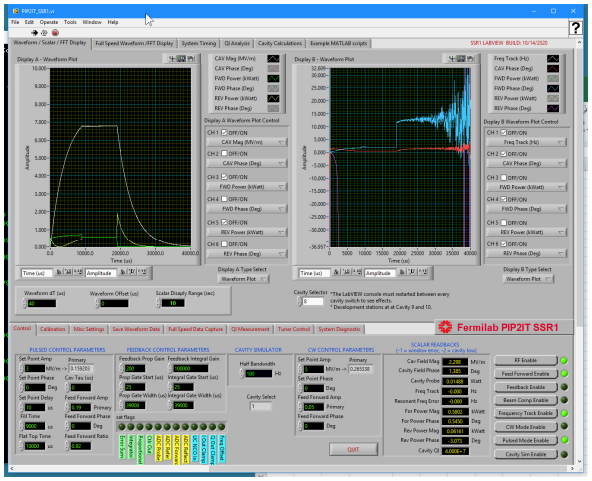


SSR1 LLRF System at PIP2IT



LLRF Controllers will be upgraded
To Arria10 FPGA based hardware

RF Detune Calibration



$$\ddot{\mathbf{V}}(t) + \frac{\omega_0}{Q_L}\dot{\mathbf{V}}(t) + \omega_0^2\mathbf{V}(t) = \frac{\omega_0 R_L}{Q_L}\dot{\mathbf{I}}(t)$$

$$\frac{d\vec{V}}{dt} = (-\omega_{1/2} + j\Delta\omega)\vec{V} + R_L\omega_{1/2}\vec{I}$$

$$\frac{d\vec{V}}{dt} = a\vec{V} + b\vec{K}_1$$

$$a = \frac{1}{\vec{M}_V} \cdot \left[\frac{d\vec{M}_V}{dt} - \beta\vec{M}_K\right]$$

- The cavity is operated in pulse mode with a cavity field ~ 1/2 FS magnitude and the cavity probe and forward waveforms are recorded.
- Numerical analysis of the acquired data provides cavity parameters such as half bandwidth and the detuning constants

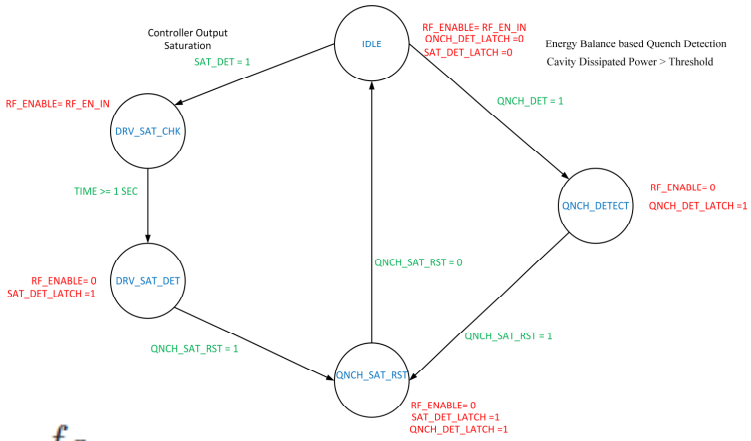
Cavity Quench Detection/ Overdrive Protection

$$P_{\text{diss}} = |\vec{K}|^2 - |\vec{R}|^2 - \frac{dU}{dt}$$

$$U = \frac{V^2}{\omega_0(R/Q)}$$

$$\frac{dU}{dt} = 2\Re\left(\vec{V}\frac{d\vec{V}}{dt}\right) \cdot \frac{1}{\omega_0(R/Q)}$$

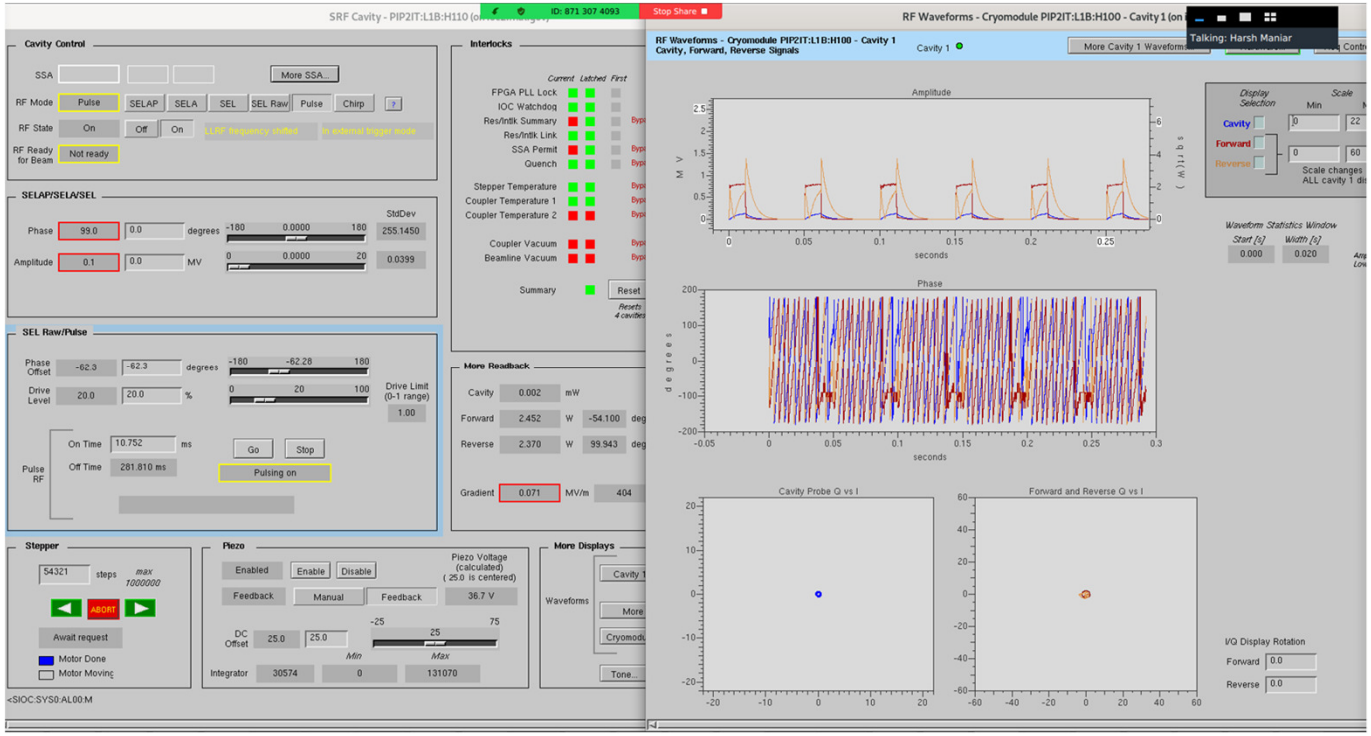
$$f_K|\vec{M}_K|^2 - f_R|\vec{M}_R|^2 - f_V 2\Re\left(\vec{M}_V \cdot \frac{d\vec{M}_V}{dt}\right) - f_Q$$



- Quench Detection is based on computing the dissipated power in the cavity. The dissipated power is compared against a threshold for quench detection
- RF overdrive is detected when the controller output saturation persists beyond a specified time (~ 1 sec)

Pulsed mode for calibration and system identification for the entire RF system (LCLS-II style EPICS screens)

- Hardware self tests and automated system ID performed at turn-on
- SSA response
- Bandwidth and Q_L
- Detune frequency
- Coupling coefficients
- Plant gain
- SEL phase offset
- Probe calibration based on emitted energy
- Circulator S_22
- Piezo transfer function and capacitance measurements
- Cavity resonance finding



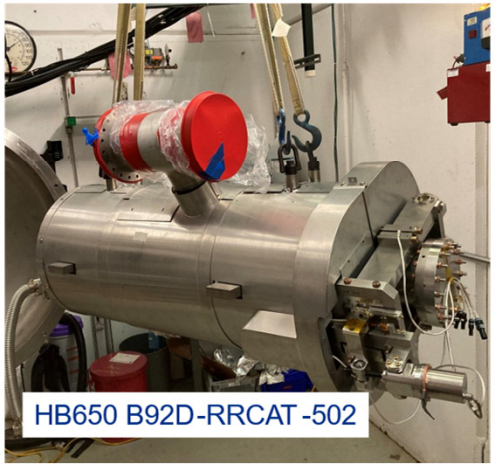
Covered in Shree's talk

HB650 and LB650 Cavity Testing at STC

- HB650, beta=0.9, **B9A-AES-001**
- January-March 2020
- STC commissioning for 650 MHz operations
- Prototype coupler/tuner validation/testing
- Prototype cavity characterization

HB650 B9A-AES-010

- HB650, beta=0.92, **B92D-RRCAT-502**
- October-November 2021
- Prototype coupler/tuner validation/testing
- Prototype cavity characterization, qualification for prototype HB650 cryomodule assembly


HB650 B92D-RRCAT-502

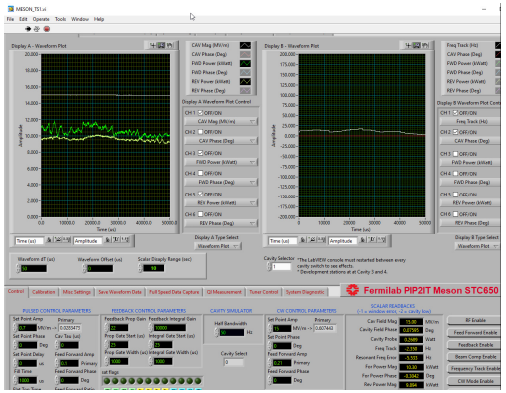
- LB650, beta=0.61, **B61-EZ-001**
- June-September 2022
- Preproduction coupler/tuner testing
- Prototype cavity characterization


LB650 B61-EZ-001

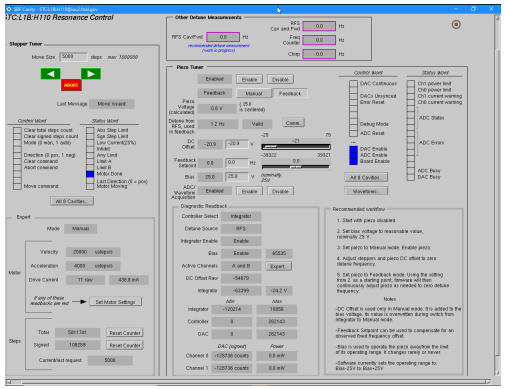

Bare HB650 Cavity


LB650 Cavity on ANL EP stand

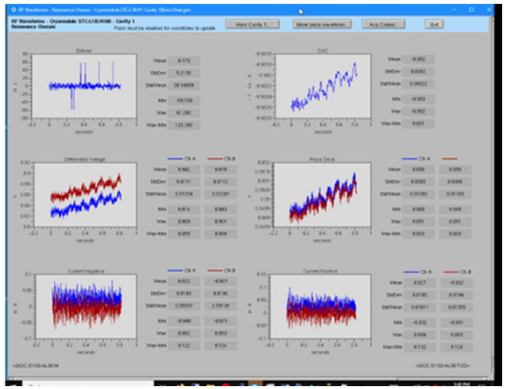
HB650 Cavity Measurements



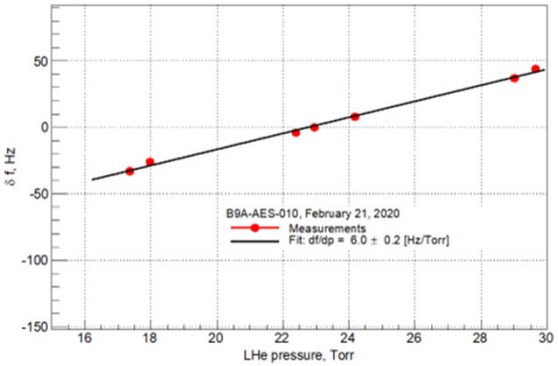
GDR Mode 15 MV/m



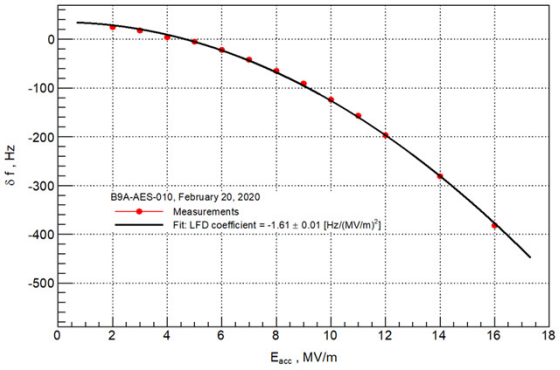
Piezo Tuner Controls



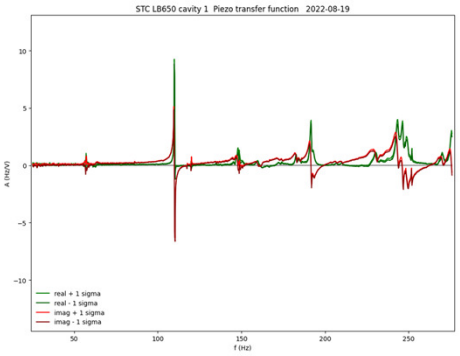
Tuner Waveforms



df/dp = 6.0 Hz/Torr



LFD Coefficient = 1.6



Piezo Transfer Function

Path to Final Design

- Options Considered for LLRF Controller
  1. Option A - FNAL Arria10 Based SOCFPGA Chassis
  2. Option B - LCLS-II design based RFS controller
  3. Port LCLS-II firmware to FNAL controller
  4. Test at STC650 and PIP-II-TI

Fermilab Arria10 SOC FPGA Board

LBNL RFS Controller (LCLS-II Based Design)

- Final Selection of LLRF Controller
  1. Marble FPGA board based RFS chassis was chosen
  2. FNAL controller firmware/software scaling to full Linac is challenging
  3. LCLS-II firmware to ported to FNAL controller does not efficiently use SOC features
  4. LCLS-II deployment of the RFS firmware/software and EPICS interface provides a straightforward path to the PIP-II design.

Quality Assurance – Test/Acceptance Plan

- A detailed test procedure will be used for each RF chassis component with acceptance criteria included to ensure any defects are identified before integration into RF station.
- The RF controller and Resonance Control Chassis will have test procedures that check all subsystems and features such as configuration, signal levels, network connectivity, digitizer noise performance etc.
- Test software and bench setups will be developed to facilitate functional and performance testing of all functional blocks and logging all test data.
- System level testing procedures will be used to test the integrated RF station components along with the EPICS user interface

Covered in Shrividhyaa's talk

Summary

- Third generation RF chassis components
- PIP2IT demonstrated LLRF systems and met PIP-II requirements
- LCLS-II is using same RF chassis components
- Goal is to use the proven LCLS-II software/firmware with EPICS user interface implemented on newer hardware
- Porting the firmware/software to newer hardware is not trivial but requires far less resources and effort than developing new software/firmware.
- Porting has been successfully demonstrated on the PIP-II RCC designed with a newer FPGA board from a different vendor (XILINX to INTEL to XILINX switch)

References

- P. Varghese et. al., 'LLRF System for the Fermilab PIP-II Superconducting LINAC', LLRF2023, Gyeongju, Republic of Korea, October 2023
- P. Varghese et. al., 'PIP-II-IT Final Report - LLRF Systems', PIP-II DocDB,#5396-v1, June 2021
- P. Varghese *et al.*, "Resonance Control System for the PIPII-IT HWR Cryomodule", IPAC21, Campinas, Brazil, May 2021, THPAB337
- P. Varghese *et al.*, " Performance of the LLRF System for the Fermilab PIP-II Injector Test", IPAC21, Campinas, Brazil, May 2021, THPAB338
- P. Varghese, 'Mu2e LLRF Controller Board Testing', Mu2e DocDB, # 30385-v2, Aug 2019

Thank You

Backup Slides