DAPHNE_V3 Status and Plans

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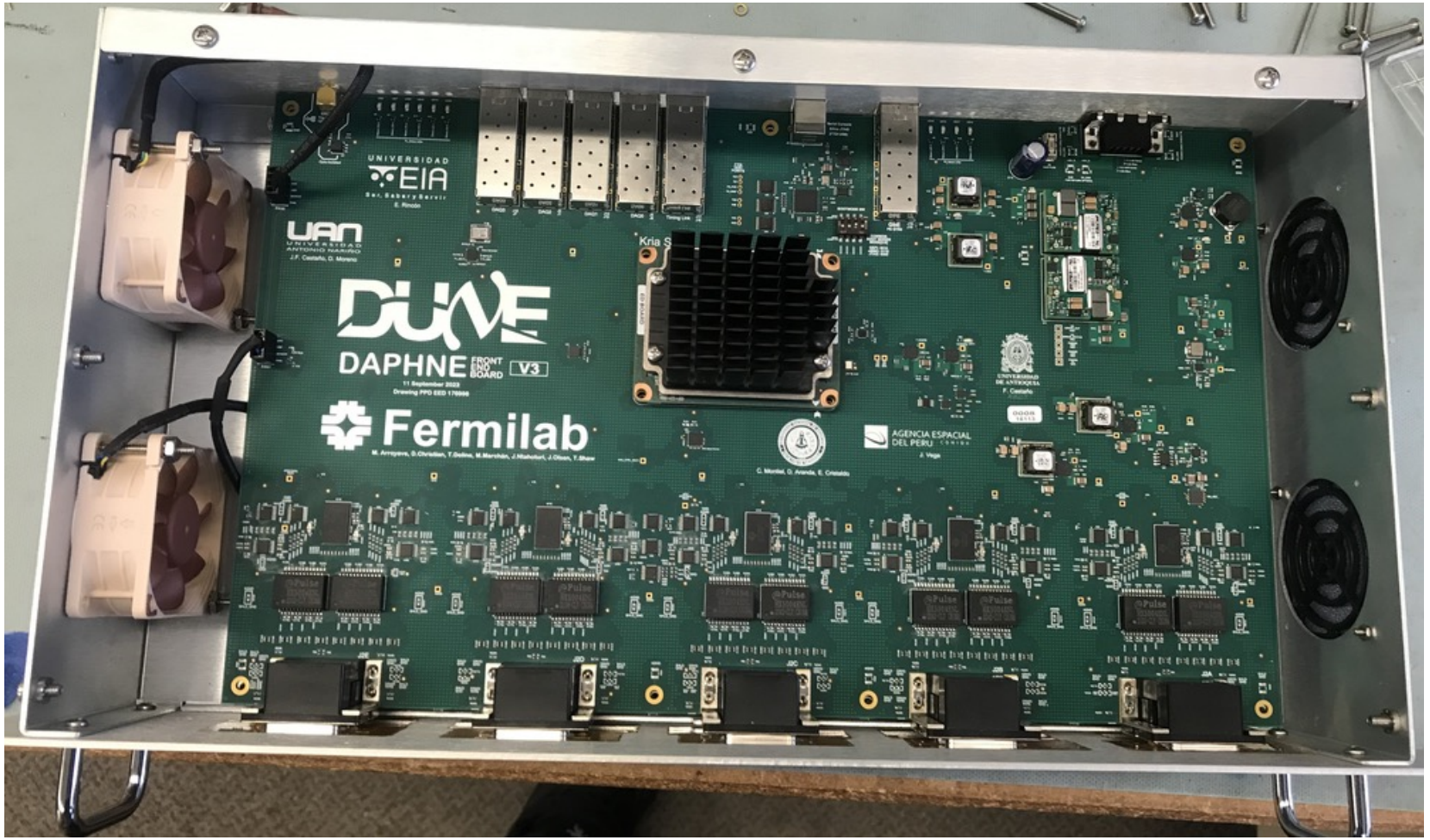
DAPHNE_V3 (40 channel version for HD)

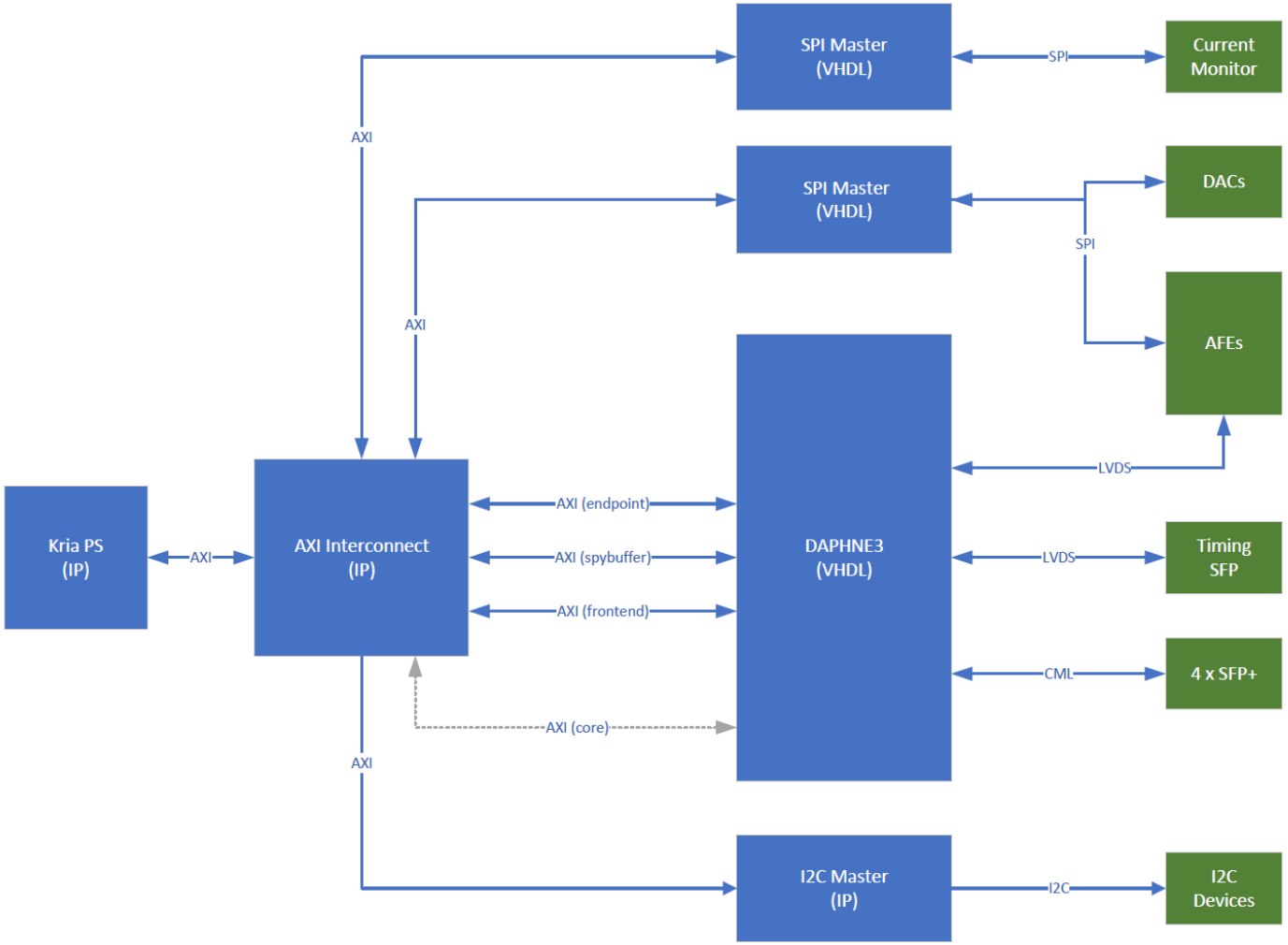
Xilinx Kria “Zynq” module enables 10 GbE output

- Multicore ARM LINUX processor
- FPGA
- “AXI” interconnect

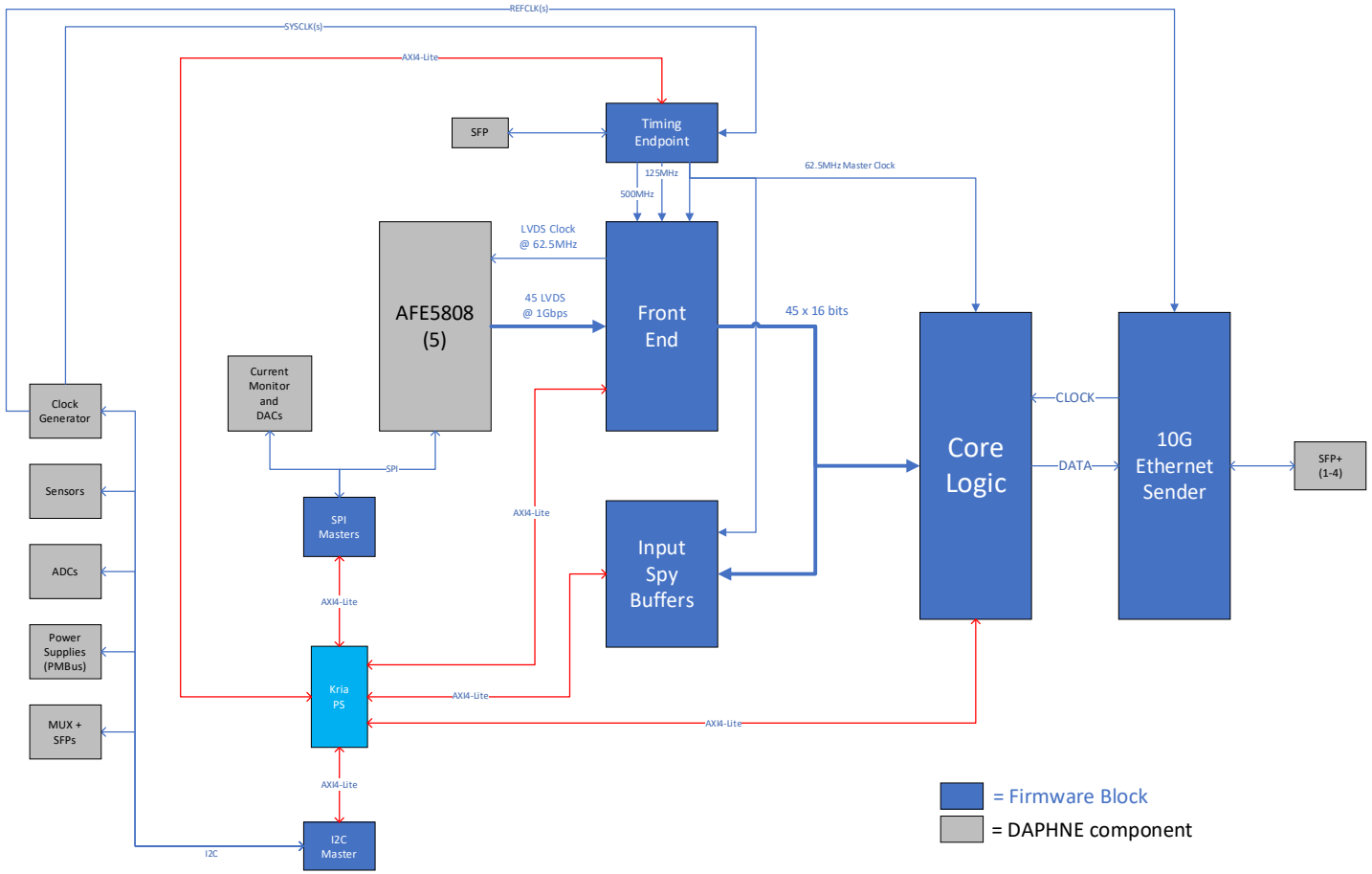
- Functions that were written in microcode for DAPHNE_V2 are now written as shell scripts or C or Python programs



(Simplified) Zync Top Level Diagram



Firmware Block Diagram



Status – the good

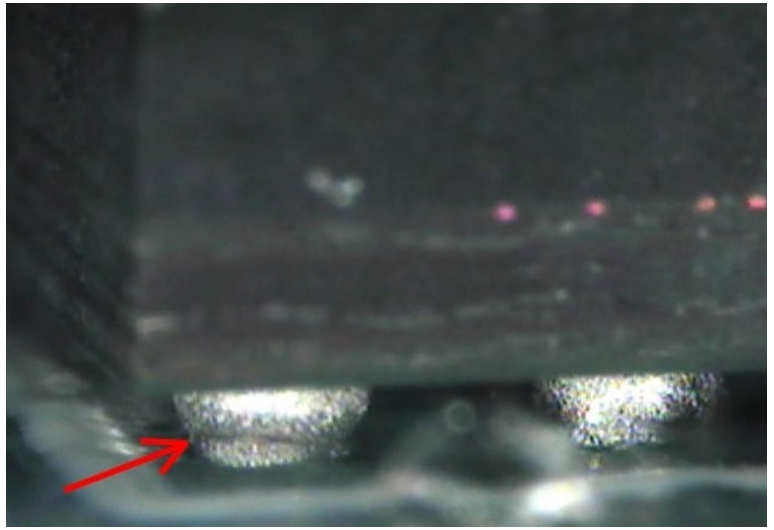
- Our procedure for compiling firmware with AXI links and timing constraints finally works reliably.
- Bias generator works.
- All DACs work.
- New current monitor (integrated mux/amp/ADC) works.
  - Kurt Francis has written the initial version of a program to measure I/V.
- All other SPI/I2C control works.
- The procedure for establishing bit and word alignment of AFE serial data input to the FPGA has been written and works.
  - This procedure relies on spy-buffer readout, so that has been tested and works.
  - AFE test modes (ramp,etc) work .
- The timing interface was tested months ago and worked.
- Minor modifications are required to reduce the usage of block RAM, but this is expected to be straightforward.
- We will implement the simple streaming sender first; this is largely unchanged from V2.
- We have a prototype 10GbE sender block (written by RAL), but need to work with the DAQ group on integration.

Status – the bad

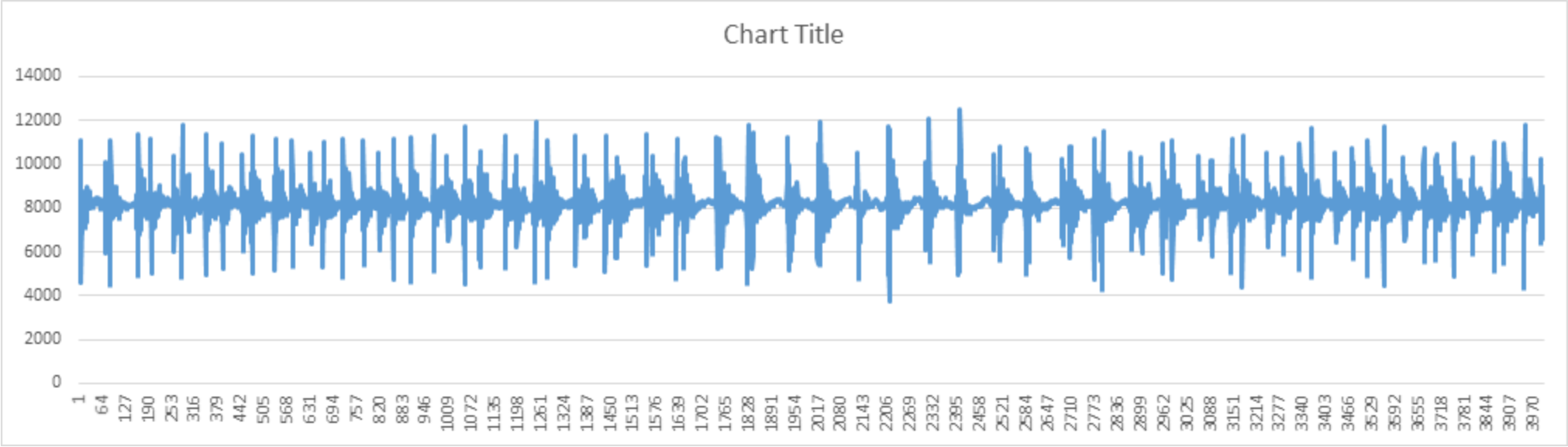
- Almost all of the boards have at least 1 AFE that does not work properly.
  - Some cannot be programmed
  - Some have one or more channels with output stuck at 0 or stuck at 1
- All channels are noisy, with or without an input signal.

AFE Problems

- The problems are different on every board, so we do not believe there is a design or artwork error.
- There were problems with the ball grid array parts when these boards were assembled.
  - The assembler called out possible “head in pillow” defects.
  - We found open circuits on a number of ground contacts on the Kria connectors.
  - The assembler reflowed all BGAs & we no longer measured opens… but we could test only a small number of the Kria connector pins and non of the AFE pins.
- Our best guess is that the AFE problems are BGA problems.
  - We are making arrangements to have the bad parts replaced on two boards.
  - This should be done next week, so in 2-3 weeks we should know whether or not this was the problem.



Noise Problems

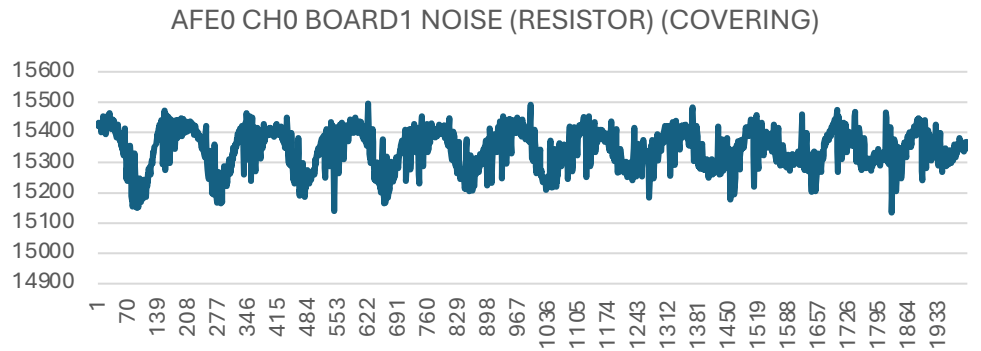


First look at a (warm) SiPM biased at 56V by DAPHNE_V3 (Kurt Francis with Jacques Ntahoturi)

Open channels look similar.

Noise Problems – Debugging

- Jacques found that the main DC/DC converters radiate quite a lot of noise.
- He built a copper box to shield the DC/DC converters and this reduced the noise significantly, but substantial noise remains.
- Shielded versions of the DC/DC converters are made, but were not available when parts were purchased for the DAPHNE_V3 prototypes. We will order shielded parts and test.
- Also, analog and digital ground are shorted and we do not yet know where the short is. This may mean that noise on digital bias voltages can inject noise through the “analog” ground. This problem is also a focus of our current efforts to understand and fix the noise problem



Plan for DAPHNE_V3 (Vertical Drift)

- We will soon start work on a 32-channel version of DAPHNE_V3 for use with vertical drift style PDS modules.
- APC has developed an optical to (single ended) electrical converter for use with DAPHNE_V2A with modifications specified by Esteban and tested first at Milano.
  - This has been used at the NP02 cold box and is being used at ICEBERG to read out cathode style PDS modules.
- APC is currently working on an 8-channel optical to (SE) electrical converter to be used with the 32-channel DAPHNE_V3.
- We have agreed to use the same D input connectors as are on the current DAPHNE_V3 at least for the first prototype.

New D Connector Pin Assignments

- Need to provide +/- 5V for the optical to electrical converters.
- Pins will be assigned so that an active differential to single ended converter can also be implemented for membrane modules.
- For membrane modules, SiPM bias voltage will be supplied through separate pins – One bias/trim pair for 4 channels.