DEEP UNDERGROUND NEUTRINO EXPERIMENT **I**nterface **C**ontrol **D**ocument	Document # **DUNE-ND-DAQ-ICD-02**	Date Effective XX Month, 20XX	Status Draft 0
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	Subsystem/Office		
Document Title **ICD Template**			

1. Change History and Approval Log

Rev	Date	Description of Changes	Group Level Approval					Chief Engr.	Project Manager
Draft 1	XX/XX/XX	Initial Draft (Uncontrolled)							

2. Table of Contents

3. Acronyms

ICD	Interface Control Document
ND	Near Detector
LAr	Liquid Argon (detector)
LArPix	Liquid Argon Pixel FEE
DAQ	Data Acquisition
FEE	Front End Electronics
TBD	To be determined
TBC	To be confirmed
CCM	Control Configuration and Monitoring

4. Reference Documents

Existing charge electronics (LArPix) documentation: data format

5. Description of Interface

This document describes the interface between the DUNE ND LAr system (charge and light systems) and the DUNE ND DAQ system. At the time of description, changes to the electronics are possible for both the charge and light system electronics.

6. Details of Interface

6.1. Physical Interfaces

6.1.1. Charge System Electronics

The interface between the LAr on-detector charge electronics and the DAQ is defined to be at the point of network switch(s) and a 100 Gbps optical fiber with redundancy. The ND LAr consortium will be responsible for the 140 1 Gb RJ45 links from the warm controller boards to the on-detector rack network switches, the number of which is TBD. The DAQ consortium will be responsible for the network switches and for the fiber to the above-ground DAQ room. The overall picture of the FEE chain is shown at the end of this section. The number of channels and boards is shown in the diagram at the end of this document.

6.1.2. Light System Electronics

The Light System electronics consist of 8400 channels readout through VME boards and consolidated by ND-LAr provided COTS units. The interface between the LAr on-detector light electronics and the DAQ will consist of optical fiber connection from the consolidation units into network switch(s), which the DAQ consortium is responsible for, with the number of connections TBD. The ND-LAr consortium is responsible for the fibers feeding into the switch, and the DAQ is responsible for the fiber to the above-ground DAQ room.

6.1.3. Timing

Timing and synchronization messages are distributed on OS2 single mode fibre. The timing system will use 1000Base-BX-20 SFP modules which transmit at 1310nm and receive on 1550nm. The TPC Electronics timing endpoints on the detector will use matching 1000Base-BX-20 SFP modules which transmit at 1550nm and receive on 1310nm.

Downlink: The timing system will normally transmit continuously. This is to allow endpoints to receive a clock even outside of a run. However, the endpoints must have the capability of recovering from an interruption in the timing data stream. The ND-LAr consortium is responsible for receiving the optical signal and distributing it to the front-end electronics. The timing endpoints will use a CDR device at the endpoints to separate clock and data signals.

Uplink: Each timing endpoint will implement the parts of the DTS (DUNE Timing System) protocol needed to respond to status requests and delay adjustment commands. If an endpoint is unable to do this then steps will be taken to ensure that the endpoint to timing system laser is disabled.

Link Speed: This is set to 62.5 MHz.

Clock Jitter: TBD

Power and Timing Card (PTC): The timing to each endpoint will be provided over a single LC fibre to the PTC. Distribution and fan-out of the timing signals from the PTC to the electronics will be the responsibility of ND-LAr.

Fiber Connection: The ND-LAr consortium is responsible for the duplex fiber that runs from the last timing system optical fanout. The ND-LAr consortium is responsible for choosing the optical connector on the transceiver on the PTC side. The transceivers on the DAQ side have an LC connector.

6.1.4. Control, Configuration, and Monitoring

The same network connections will be used for CCM as are used for data flow.

6.2. Data Formats and Protocols

6.2.1. Charge Electronics

The average data rate from the charge readout will be 30 MB/s in continuous readout operation, with a maximum of 100 MB/s, transmitted as self-triggered, zero-suppressed information. There may be a spike in rate when the electronics are starting up that goes higher. This will be accounted for in startup procedures through the CCM system of the DAQ.

The input and output data formats are described in the linked document in section 4. Any changes to the format will be discussed between the LAr group and the DAQ group and the change agreed between the consortia.

Data will be transmitted as TCP/IP.

6.2.2. Light Electronics

The average data rate from the light electronics is TBD. The full readout for a beam spill will be 33 MB, but the rate for cosmic and calibration has not yet been determined.

The data will be packetized waveforms with a 16 ns sampling rate and 2048 sample buffer depth available on-card.

Data will be transmitted over TCP/IP.

6.2.3. Timing

Timing and synchronization messages are distributed using the DUNE Timing System (DTS) protocol described in https://edms.cern.ch/document/2209895. The timing system provides common firmware block to decode the timing protocol, which will be incorporated into the overall firmware design for the receiving FPGA in each endpoint component.
In addition to the clock, the timing system will distribute time synchronous commands. For the moment we have not identified the need for any ND-LAr Electronics specific time synchronous command. Should this need arise, the exact list of commands that are needed by the TPC will be agreed at a later stage. As discussed below, the DAQ consortium has a requirement that synchronous information from the timing system should be included in all data headers, using the available bits.

6.2.4. Control, Configuration, and Monitoring

TCP/IP over ethernet will be used to exchange control, configuration and monitoring data with the ND-LAr electronics. All commands initiated by the CCM will require an acknowledgement from the electronics to be considered successful.

6.3. Software Interfaces

6.3.1. Charge Electronics

DAQ and NDLAr commit to providing software libraries and tools to initialize, monitor and reset the data links at the respective ends. It shall be possible to interrupt and resume the flow of data from the NDLar charge electronics to the DAQ via software. It shall be possible to assess the data integrity at both ends via software tools.

6.3.2. Light Electronics

DAQ and NDLAr commit to providing software libraries and tools to initialize, monitor and reset the data links at the respective ends. It shall be possible to interrupt and resume the flow of data from the NDLar PS to the DAQ via software. It shall be possible to assess the data integrity at both ends via software tools.

6.3.3. Timing

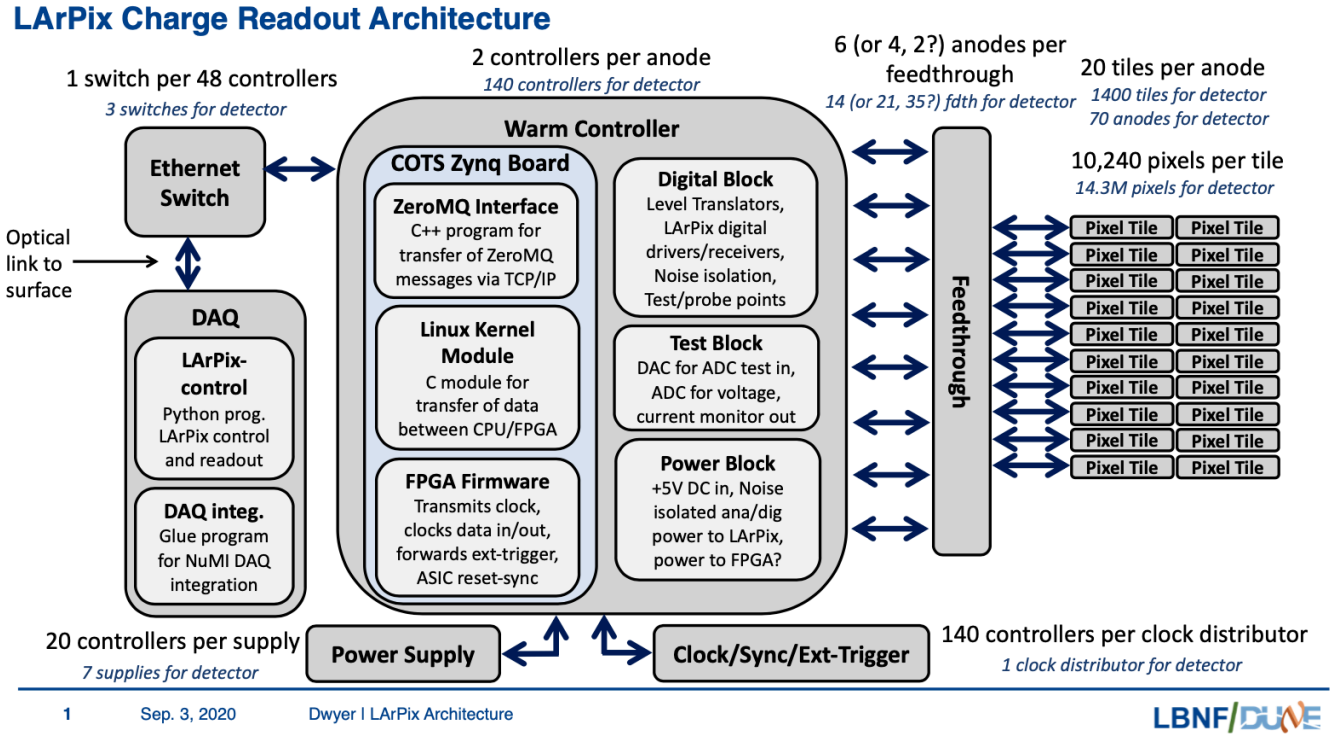
DAQ and TPC commit to providing software libraries and tools to initialize, monitor and reset the timing endpoints at the respective ends. It shall be possible to assess the timing connection status at both ends via software tools.

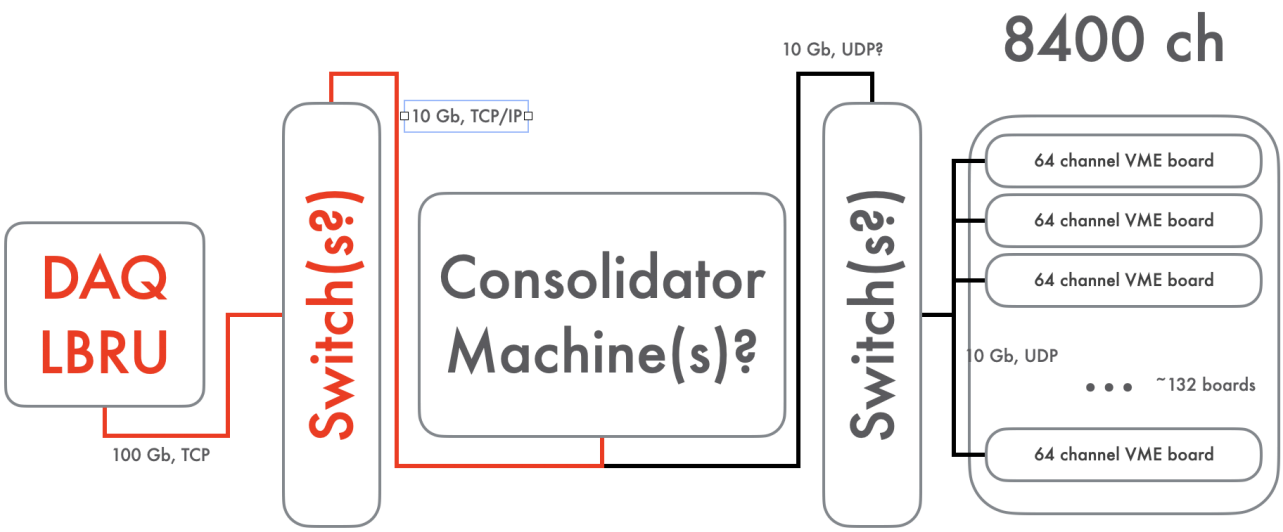
6.3.4. Control, Configuration, and Monitoring

The DAQ is responsible for providing a framework for controlling, configuring and monitoring any element in the data taking chain, including the charge and photon detector

Electronics. It is the responsibility of the ND-LAr consortium to provide the resources and expertise for the development of the specific control, configuration and monitoring for the Electronics, including both data transmission and timing aspects. The ND-LAr consortium shall also provide the software for uploading or reloading firmware. It is a choice of the ND-LAr consortium to define which parameters of the electronics are configured and controlled through the DAQ chain and which components shall be controlled and monitored via the SC.

The TPC and DAQ consortia will work together to define how the electronics and CCM interact when including/excluding individual boards into/from an ongoing run. The ND-LAr and DAQ consortia will work together to define how error conditions will be handled on both sides of the timing, control, and configuration links. The ND LAr and DAQ consortia will also work together to define how internal calibration of the ND LAr electronics are performed.




8400 ch
10 Gb, UDP?
10 Gb, TCP/IP
DAQ
LBRU
100 Gb, TCP
Switch(s?)
Consolidator
Machine(s)?
Switch(s?)
64 channel VME board
64 channel VME board
64 channel VME board
10 Gb, UDP
~132 boards
64 channel VME board