Study of FEMB Saturation Response

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Brookhaven National Laboratory

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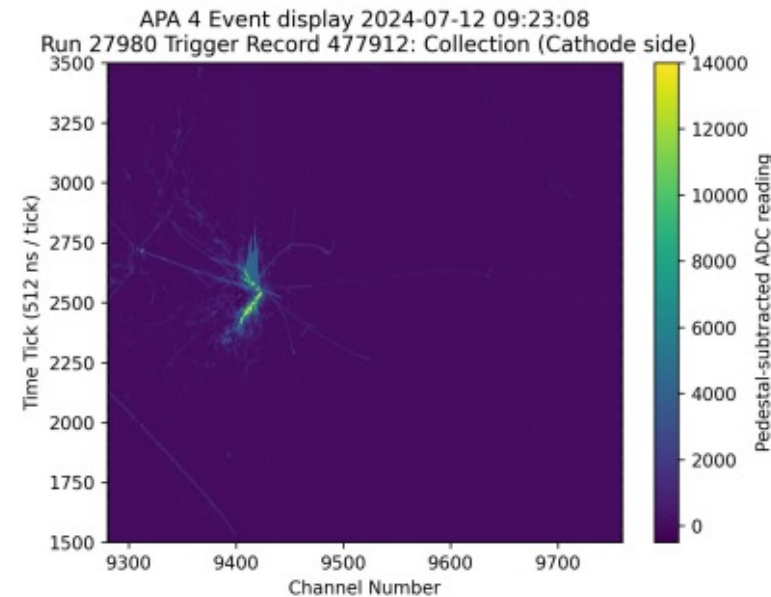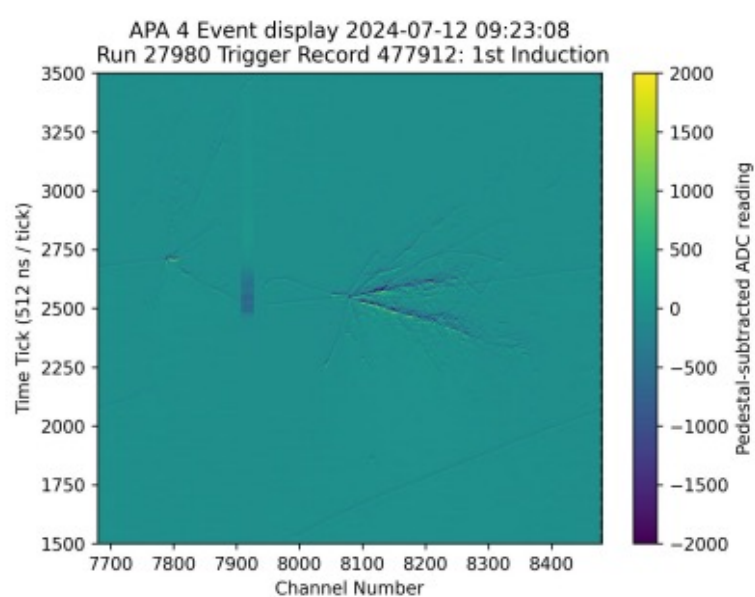
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DUNE

Introduction

- Roger's report on July 30 and August 6
  - https://indico.fnal.gov/event/65701/
  - https://indico.cern.ch/event/1444711/

Setup at BNL
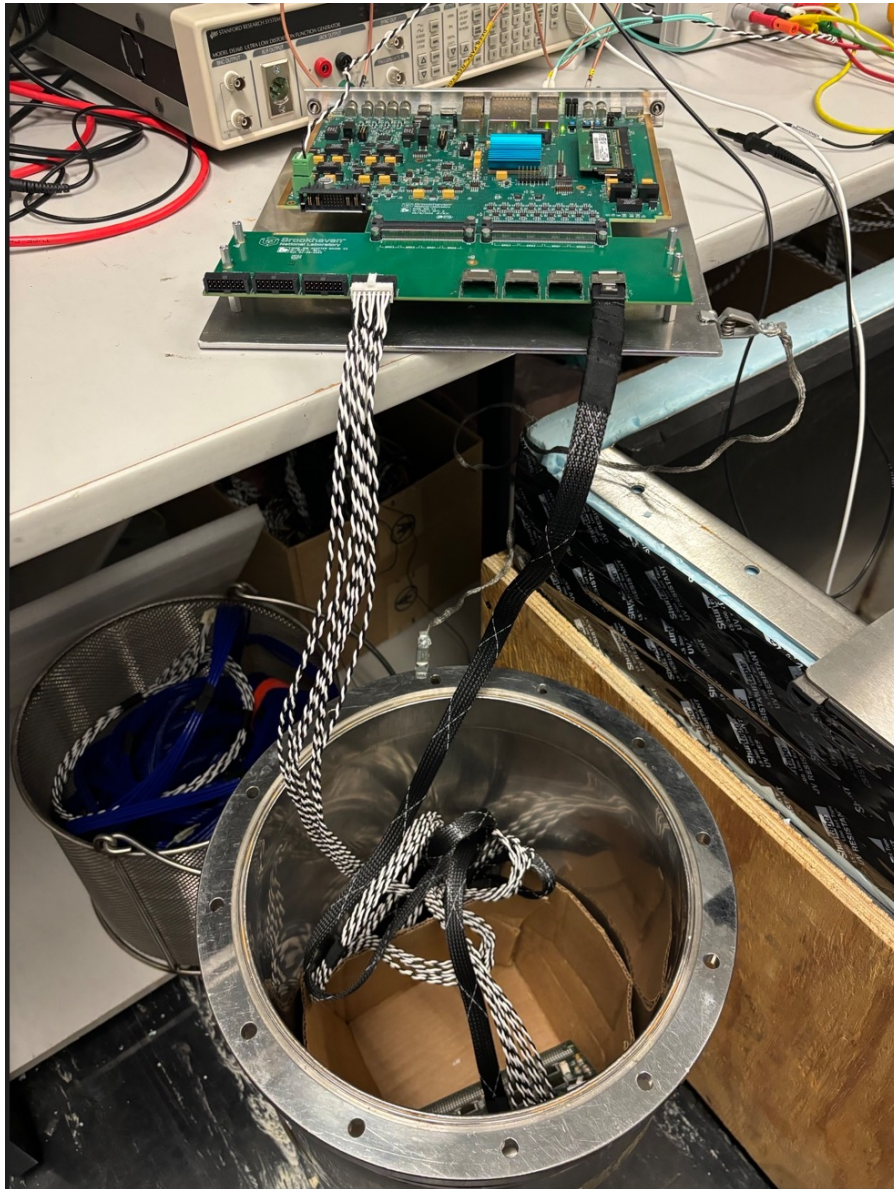
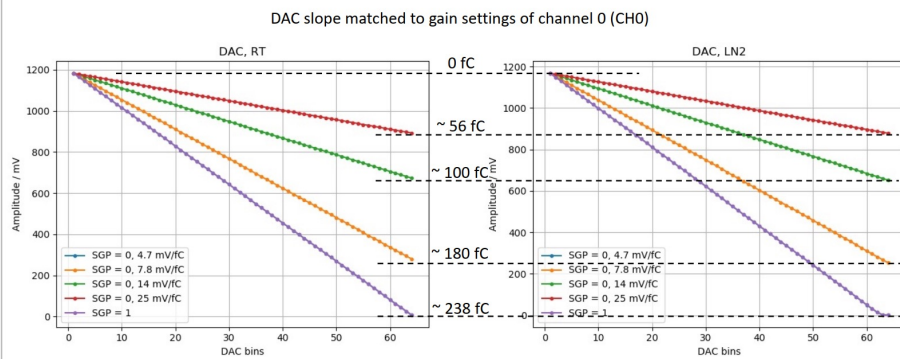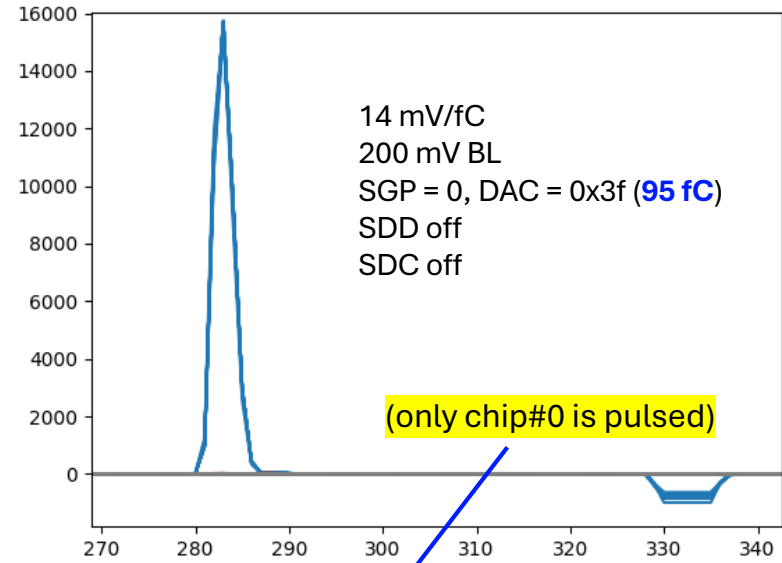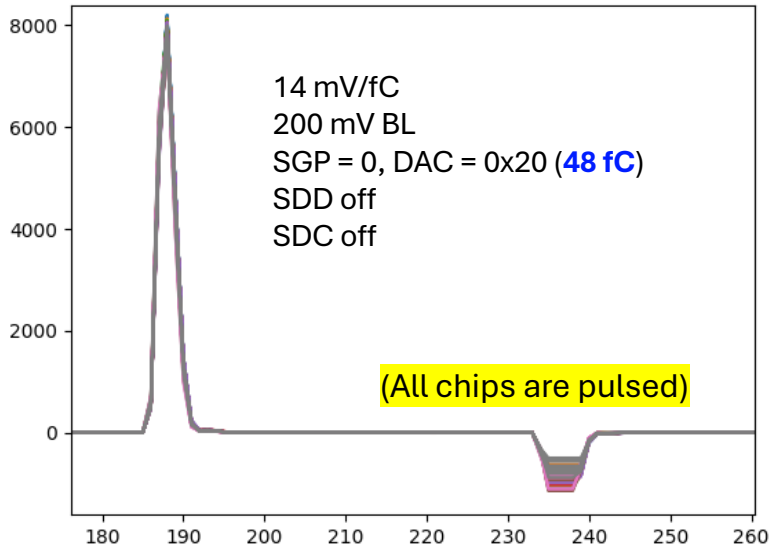Location of LArASIC (ColdADC I2C address)

| 0(0x08)	3(0x0B)		4(0x04)	7(0x07)
FEMB				
1(0x09)	2(0x0A)		5(0x05)	6(0x06)
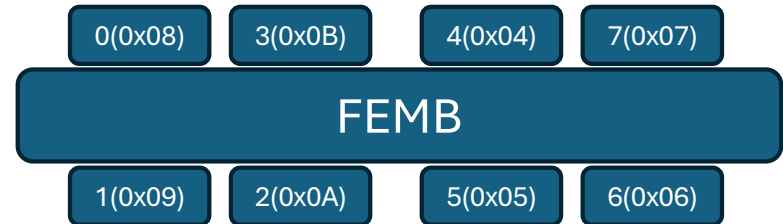
- Chip#0-3 (16x4 = 64 channels) share the same power rails on the half FEMB

- Chip#4-7 share the same power rails on the other half FEMB
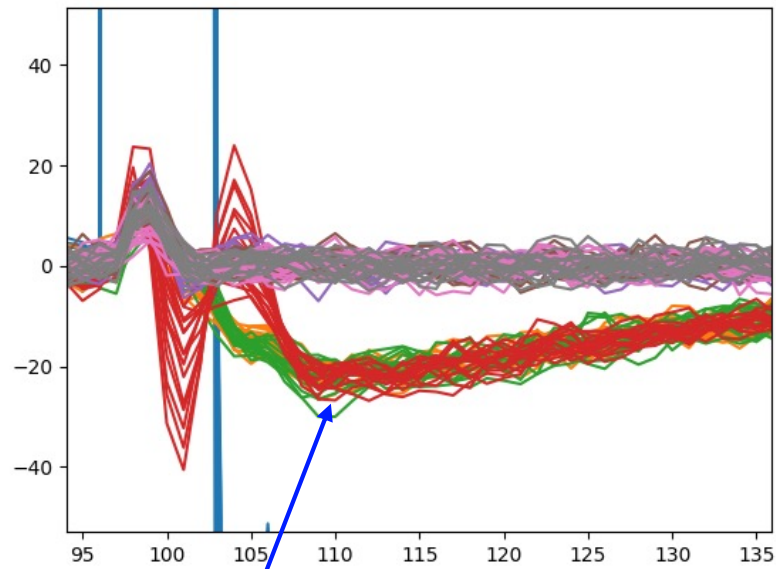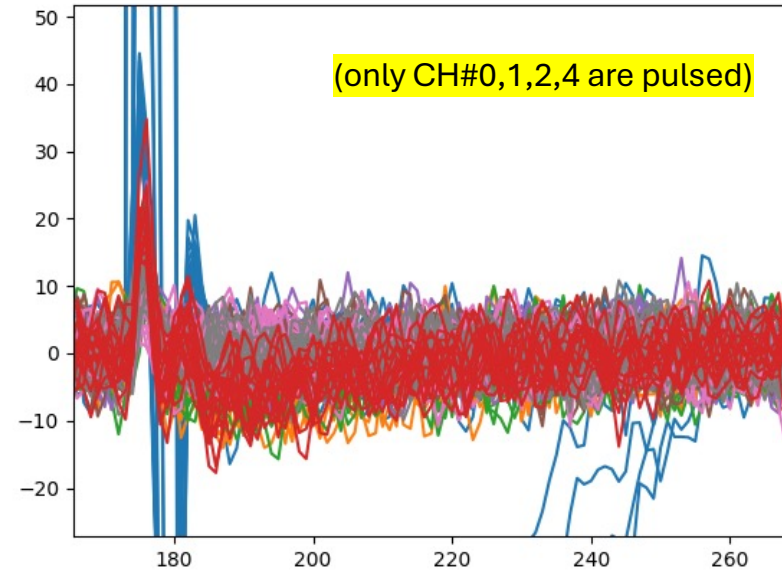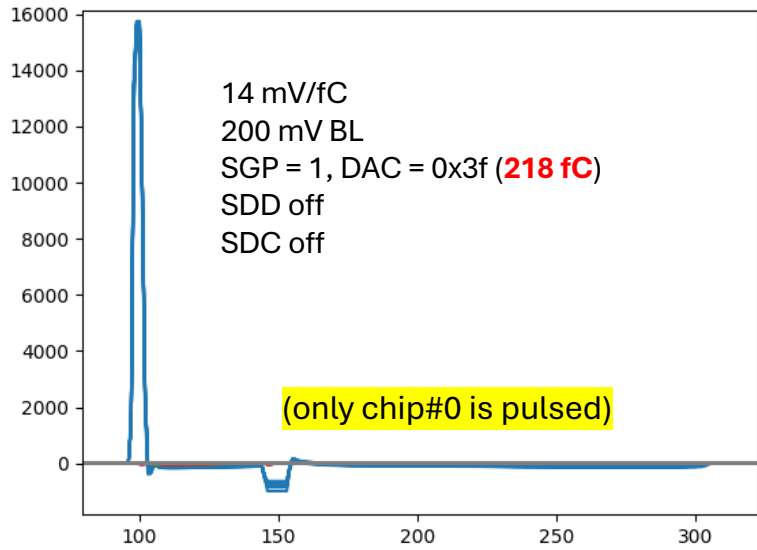
At room temperature (1)

14 mV/fC
200 mV BL
SGP = 0, DAC = 0x20 (**48 fC**)
SDD off
SDC off

(All chips are pulsed)

14 mV/fC
200 mV BL
SGP = 0, DAC = 0x3f (**95 fC**)
SDD off
SDC off

(only chip#0 is pulsed)

DAC slope matched to gain settings of channel 0 (CH0)

DAC, RT   0 fC
            ~ 56 fC
            ~ 100 fC
            ~ 180 fC
            ~ 238 fC

DAC, LN2

Chip#1   Chip#2

Chip#3   Chip#4,5,6,7

SGP = 0

4.7 mV/fC: DAC LSB = 18.66 mV (SGP = 1)
7.8 mV/fC: DAC LSB = 14.33 mV
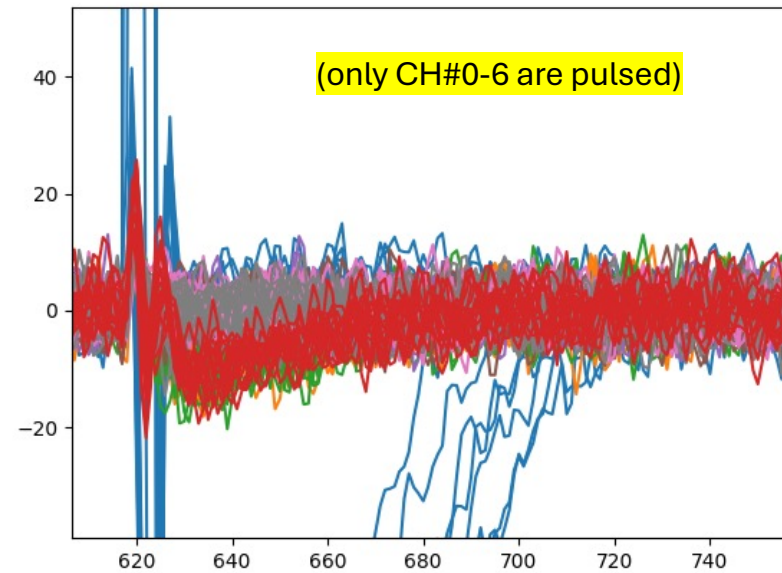14 mV/fC: DAC LSB = 8.08 mV
25 mV/fC: DAC LSB = 4.61 mV
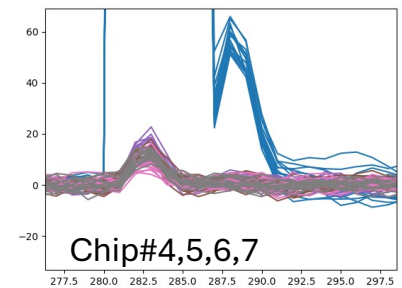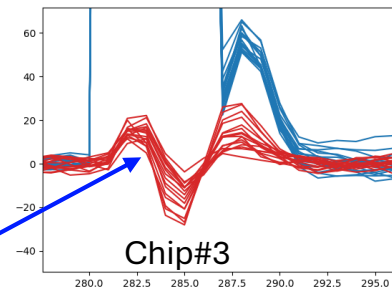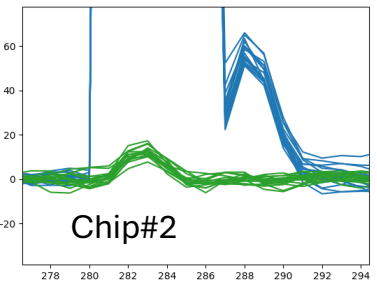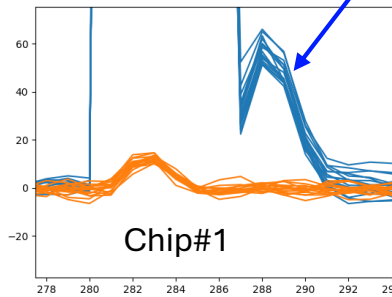
Note: Small spike (crosstalk) on chip#1,2,3,4,5,6,7 is affected by LArASIC_PULSE from COLDATA
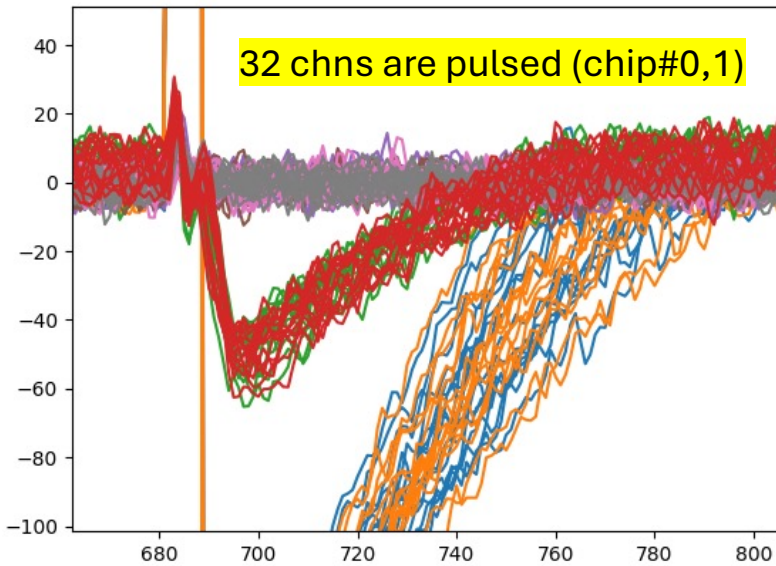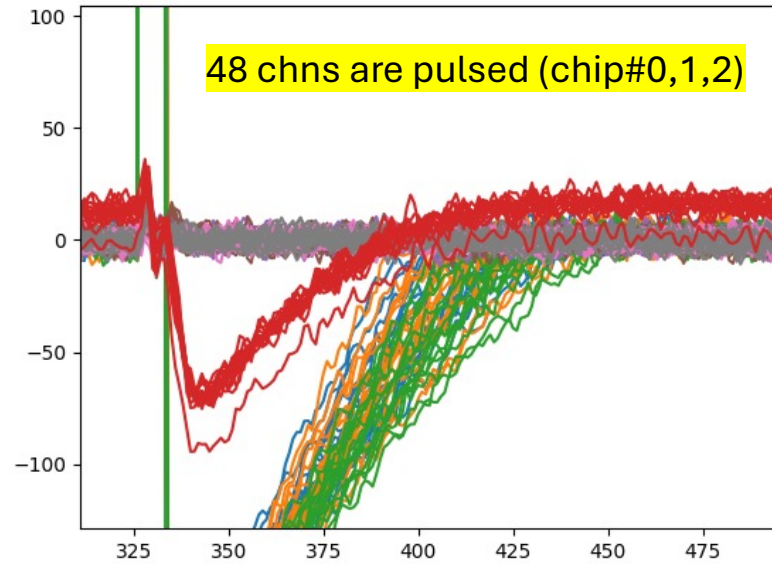Chip#3 and chip#0 are both on the top side

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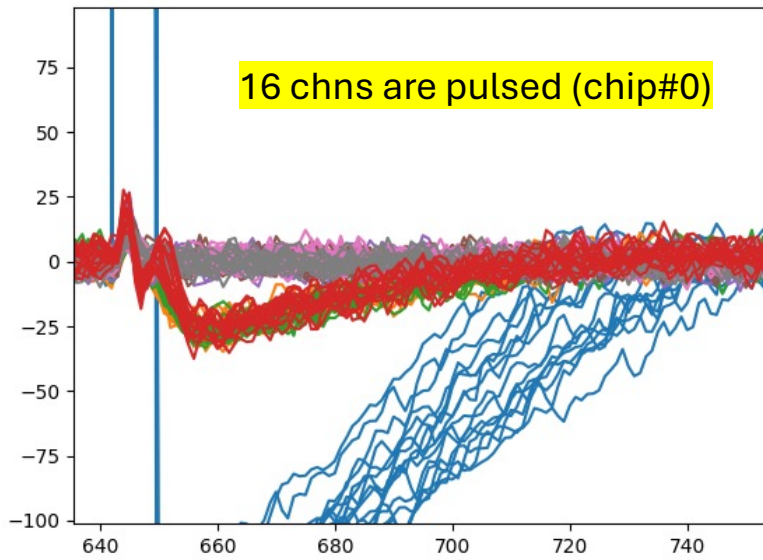# At room temperature (2)

14 mV/fC
200 mV BL
SGP = 1, DAC = 0x3f (**218 fC**)
SDD off
SDC off

(only chip#0 is pulsed)

(only CH#0,1,2,4 are pulsed)

(only CH#0-6 are pulsed)

Negative tail observed on chip#1,2,3

At room temperature (3)

16 chns are pulsed (chip#0)

48 chns are pulsed (chip#0,1,2)

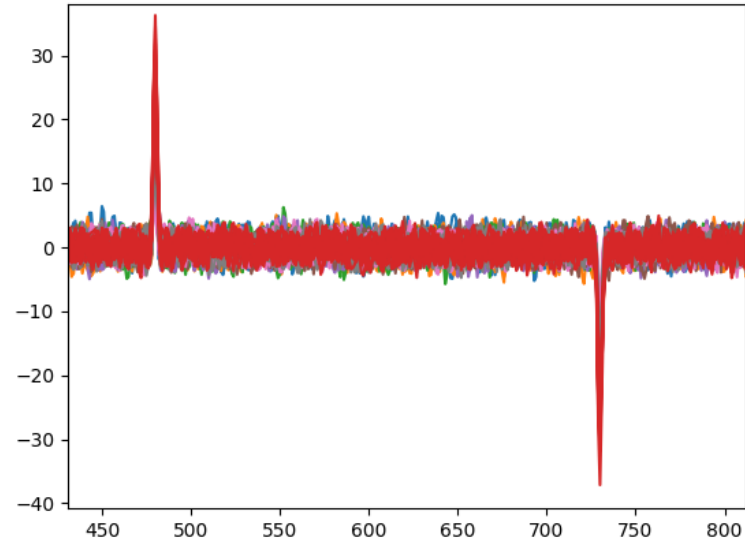32 chns are pulsed (chip#0,1)

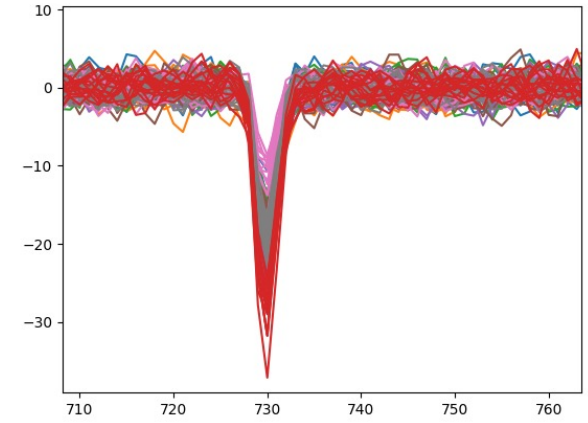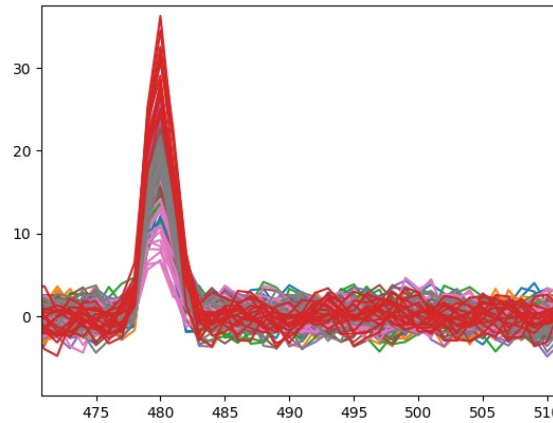**Note**: Saturation response is independent of the baseline setting

At LN2

LN2
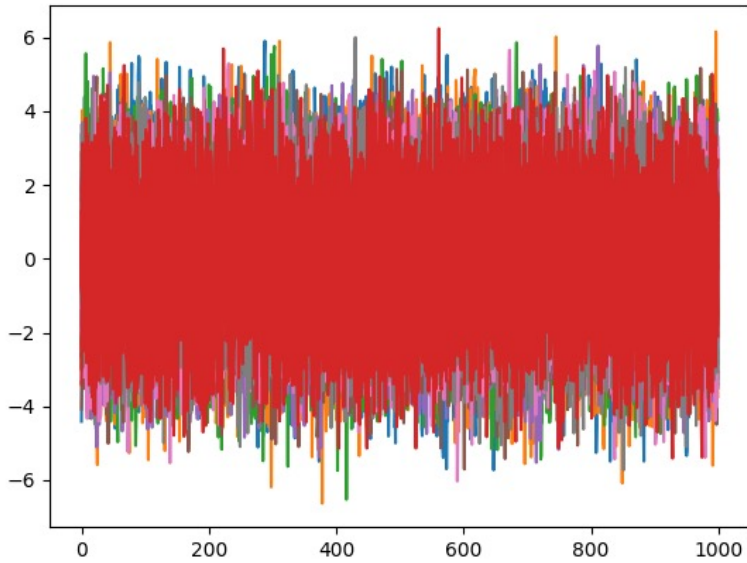
Pedestal data @ 14 mV/fC
Disable all calibration sources

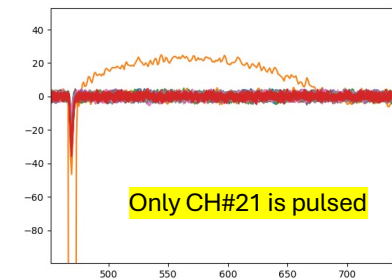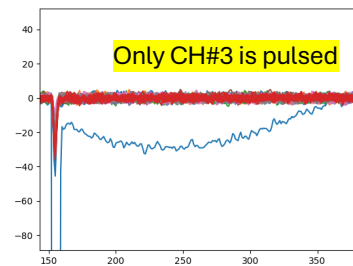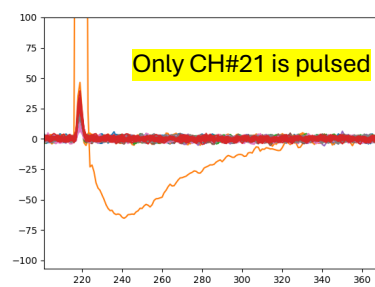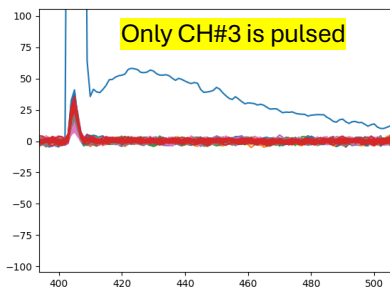LArASIC calibration is disabled
Pulser control signals generated by COLDATAs are on

Crosstalk needs to be taken into account in the calibration data processing

LN2: All channels are pulsed

14 mV/fC, **46 fC** (sgp=0, dac=0x1f), 900 mV BL
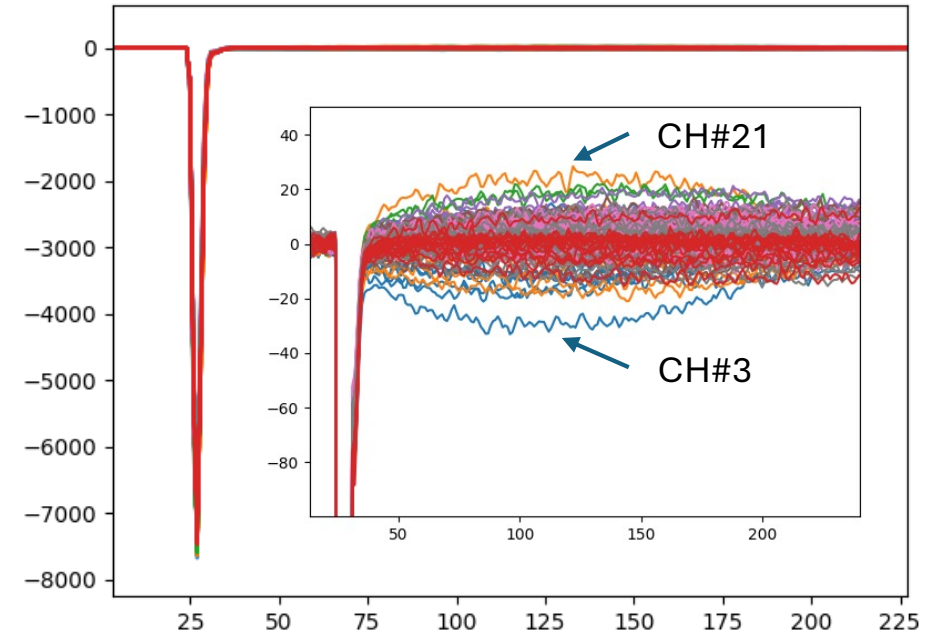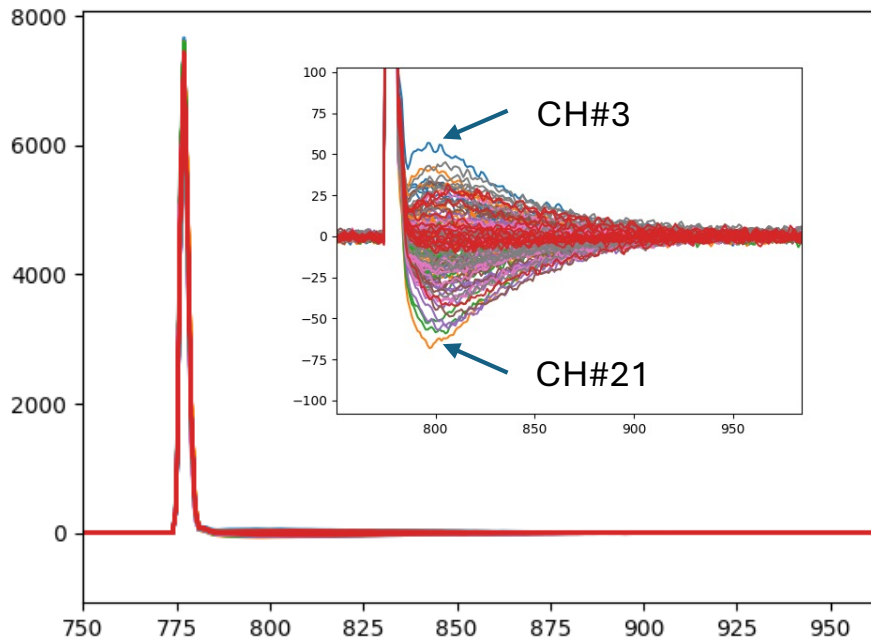
- **Non-ideal pole-zero cancellation (return to baseline) is more pronounced at LN2 temperature due to mismatch, response is independent among different channels**
- **Negative tail is negligible when FE is not saturated**

LN2: Chip#0 (16 chns) is pulsed

- sgp=1, dac=0x3f (**218 fC**), 14 mV/fC, chip#0 is 200 mV BL (other 900 mV BL)
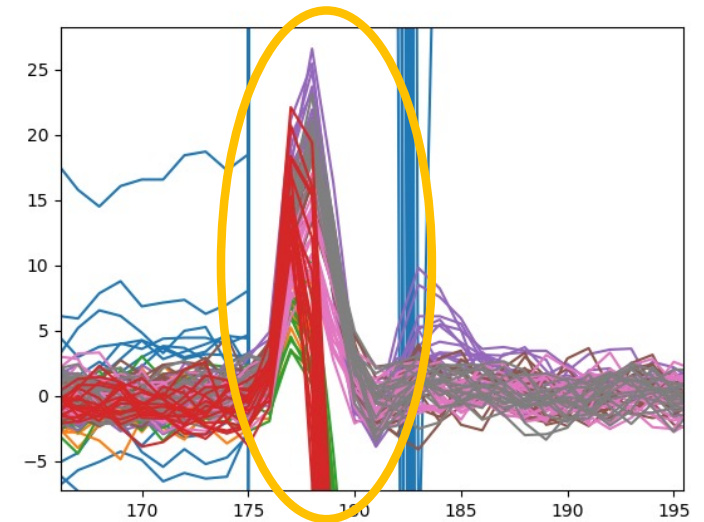

CH#16-63 on the same half FEMB show **negative tail**

CH#64-127 on the other half FEMB have minimum impact, mostly due to the COLDATA pulser control signals
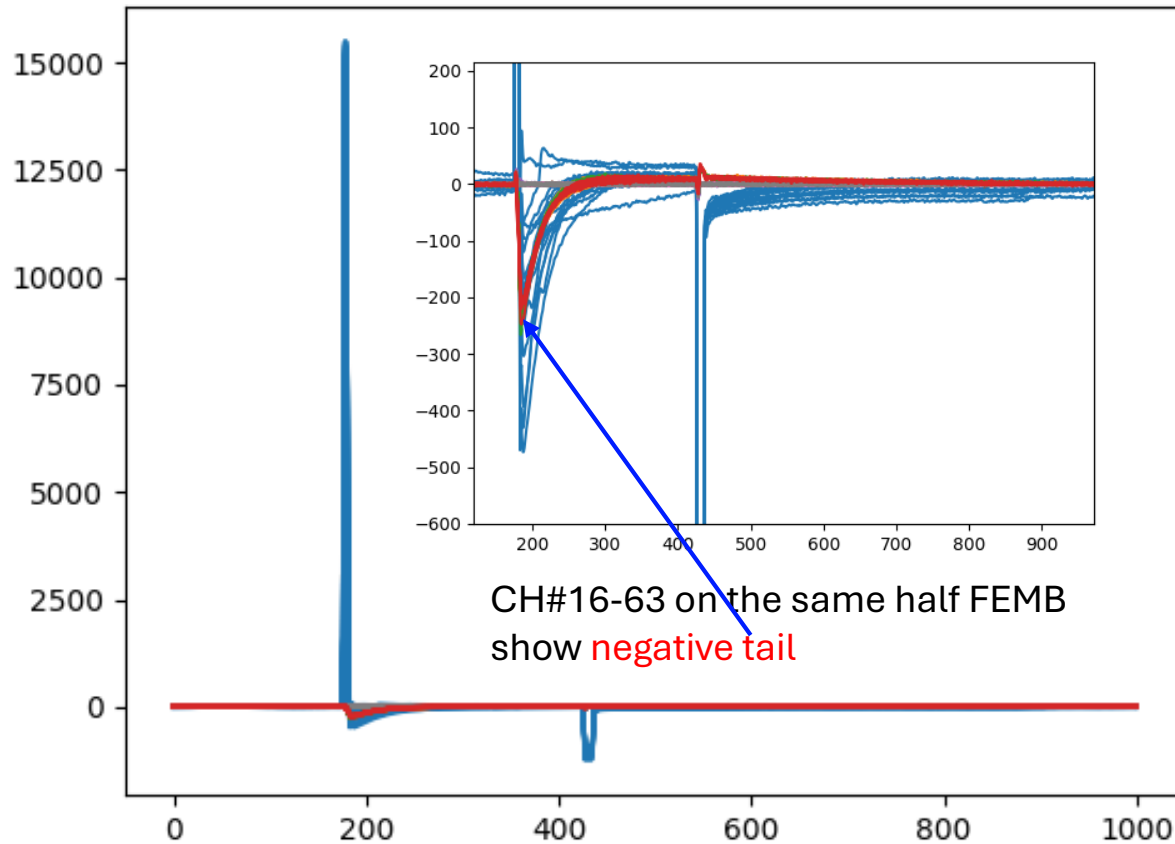
LN2: Chip#0,1,2 (48 chns) are pulsed with 95fC
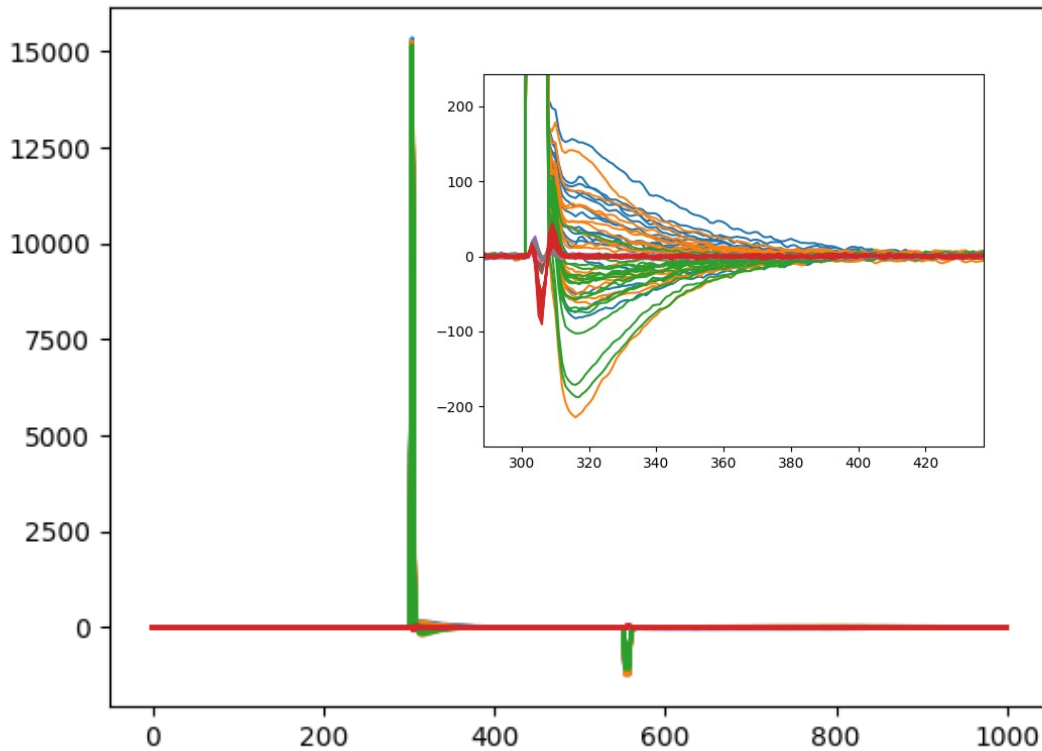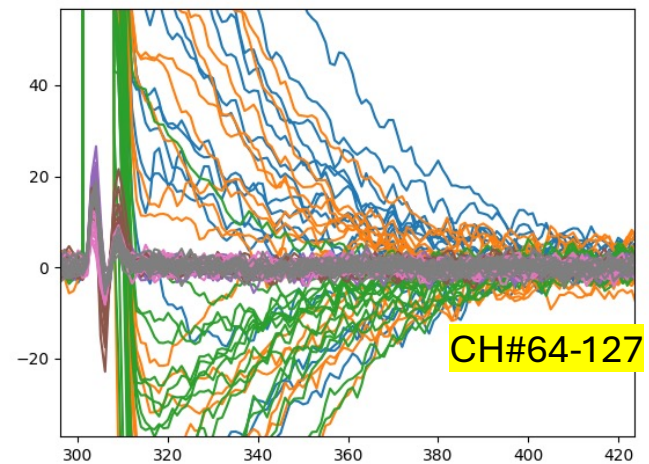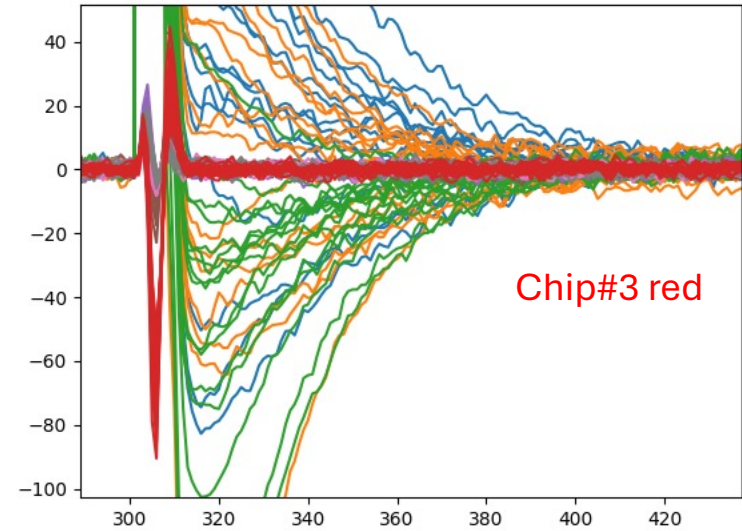
- sgp=0, dac=0x3f (**95 fC**), 14 mV/fC, chip#0,1,2 are 200 mV BL (other 900 mV BL)
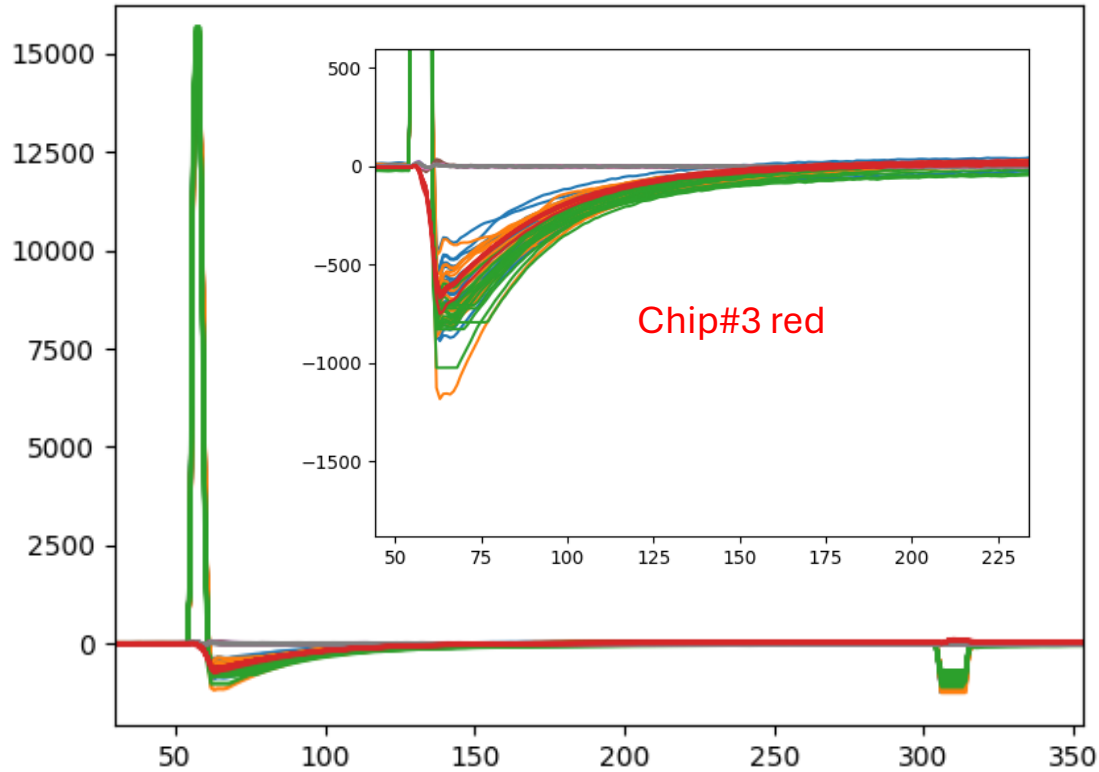

Negative tail on the same half FEMB is relatively small when FE just reaches its maximum dynamic range
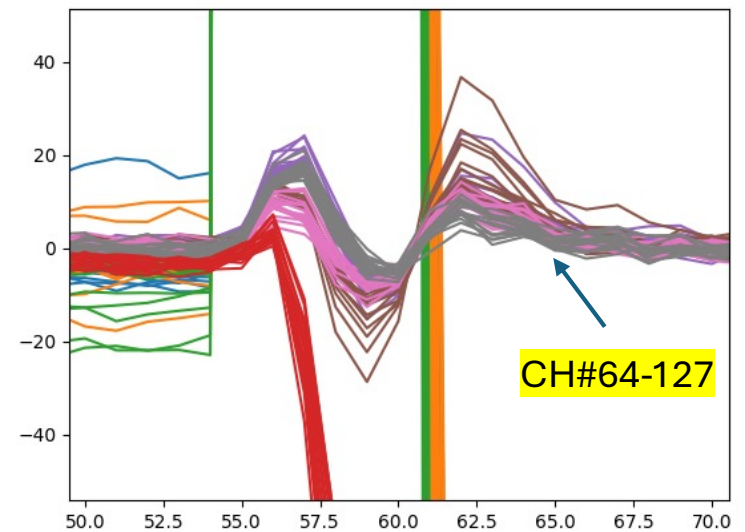
Chip#3 red

CH#64-127

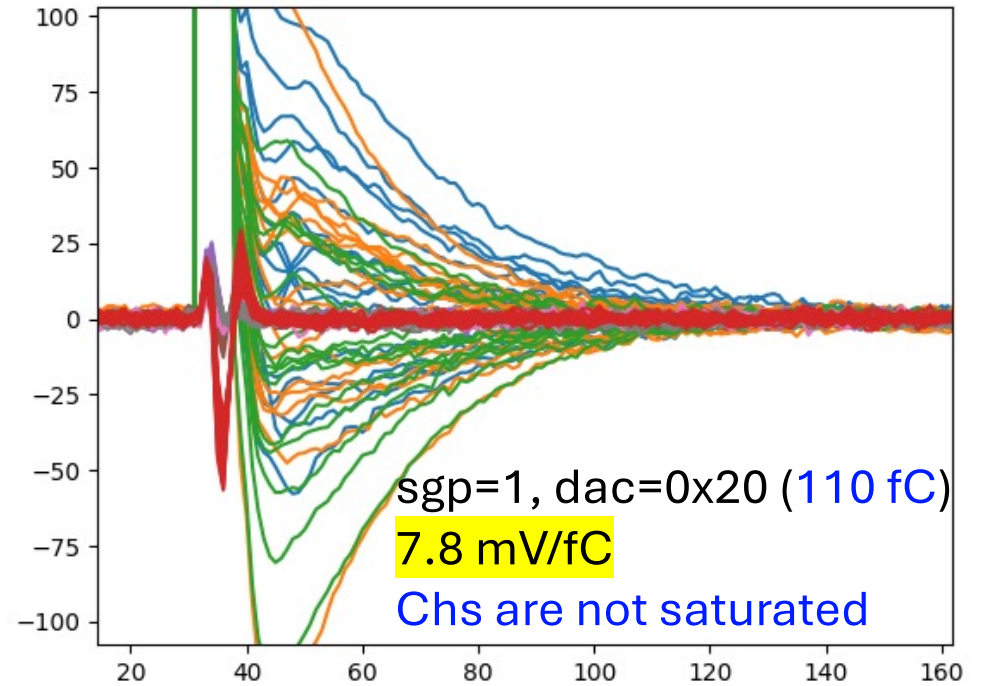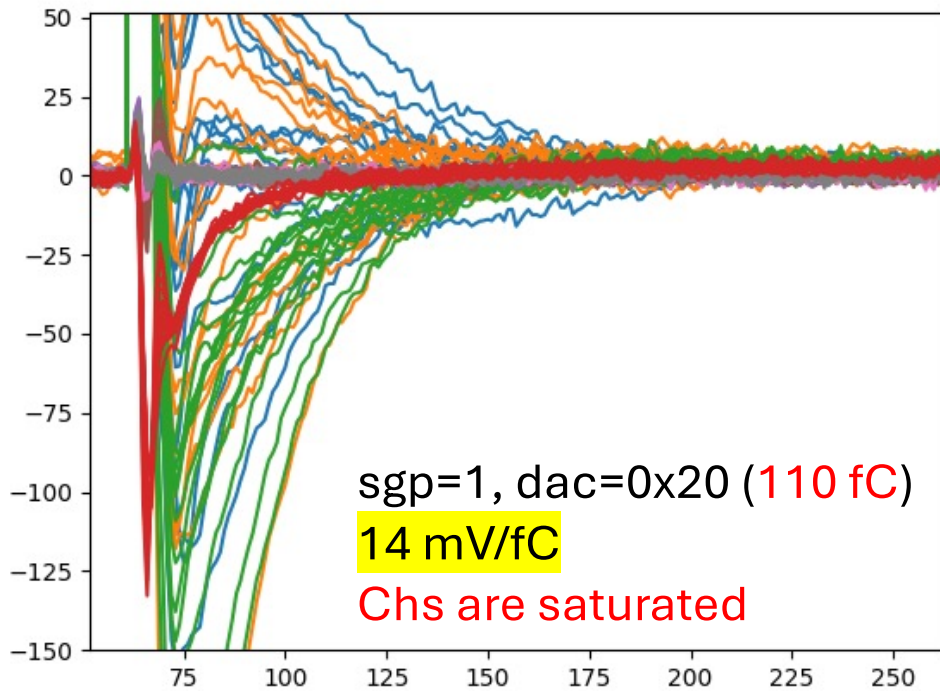# LN2: Chip#0,1,2 (48 chns) are pulsed with 218 fC

- sgp=1, dac=0x3f (**218 fC**), 14 mV/fC, chip#0,1,2 are 200 mV BL (other 900 mV BL)

Chip#3 red

- Negative tail of the half FEMB shows up when FE channels enter deep saturation

CH#64-127

LN2: 3 chips (48 chns) are pulsed at 110 fC

sgp=1, dac=0x20 (110 fC)
14 mV/fC
Chs are saturated

sgp=1, dac=0x20 (110 fC)
7.8 mV/fC
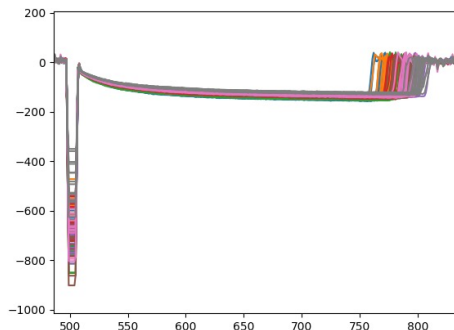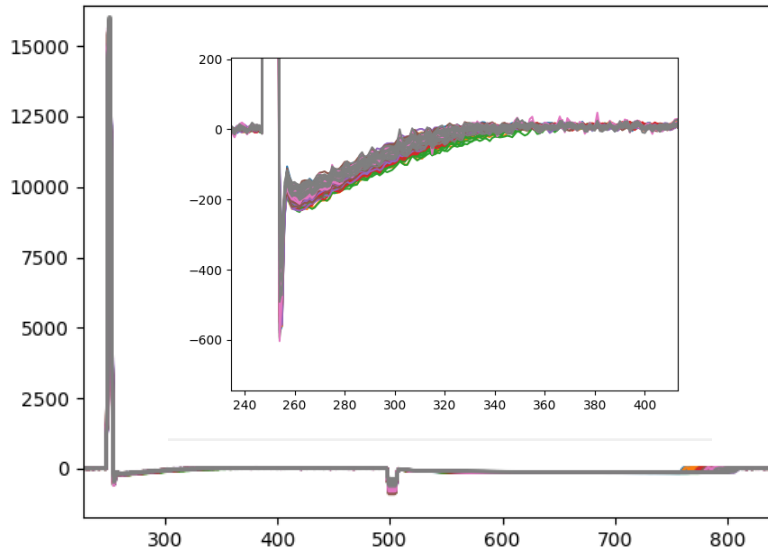Chs are not saturated

LN2: Summary of observations

- Many more detailed measurements are in backup slides
  - Similar observations with both internal and external calibration injections
- Negative tail shows up when channel enters saturation
  - At LN2, even only one channel is deeply saturated, other channels on the same half FEMB show negative tail
- The amplitude of negative tail becomes larger when more channels are deeply saturated
  - The amplitude of negative tail has more dependency on the number of saturated channels rather than the deep saturation charge
- Negative tail is mostly independent of
  - Leakage current setting
  - Gain setting when channels are deeply saturated
  - Peaking time setting (>= 1us)
  - Output mode setting when channels are deeply saturated
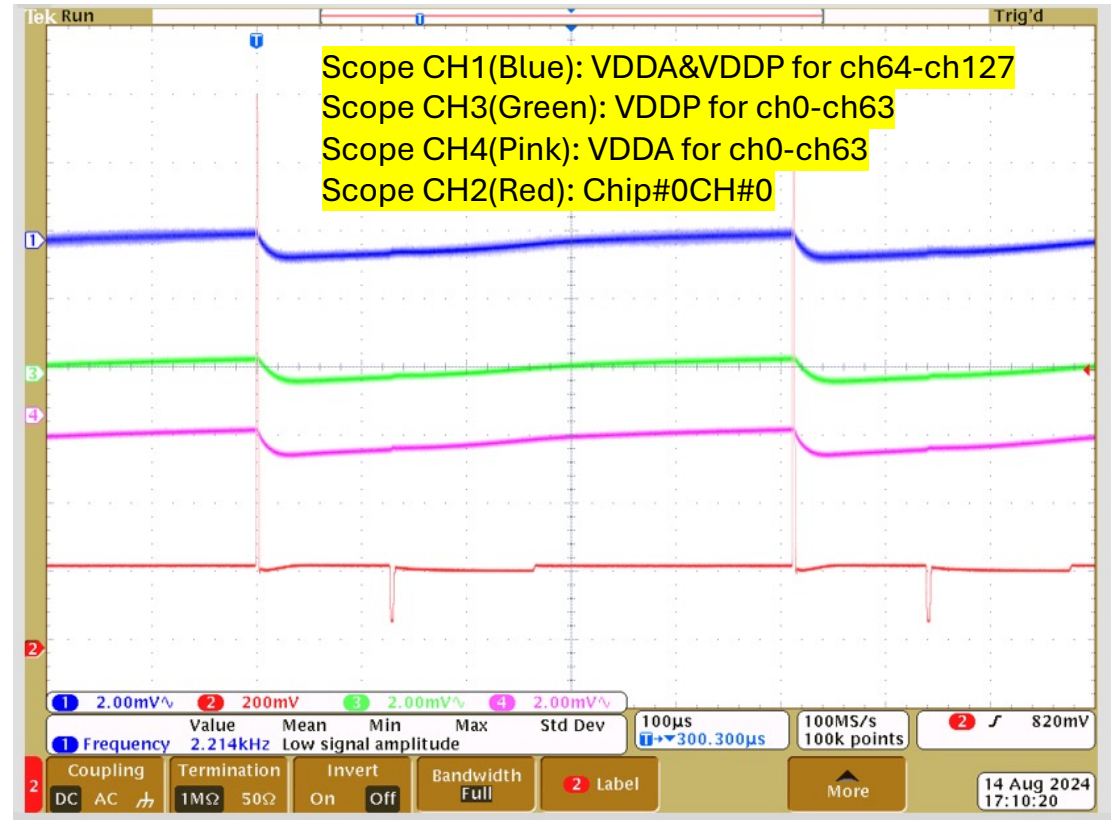
Investigation of power rails

RT: Chip#0CH#0 is selected for monitoring

- All channels are pulsed at 218 fC

VDDA&VDDP of CH64-CH127 tied together
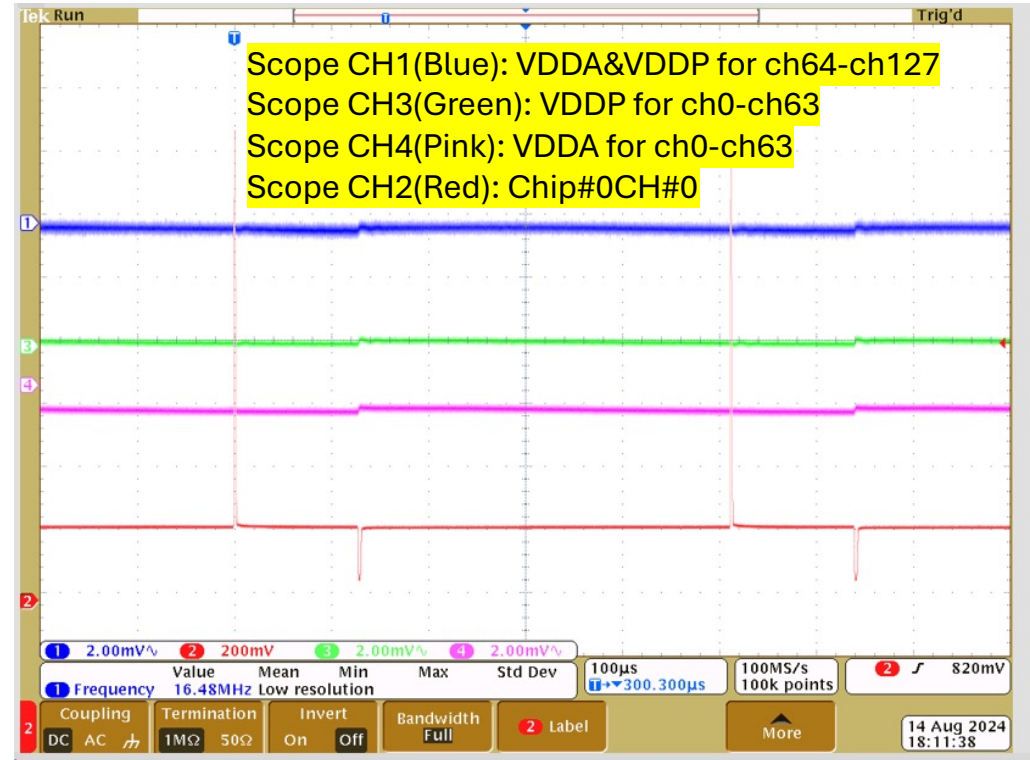VDDA&VDDP of CH0-CH63 tied together

Scope CH1(Blue): VDDA&VDDP for ch64-ch127
Scope CH3(Green): VDDP for ch0-ch63
Scope CH4(Pink): VDDA for ch0-ch63
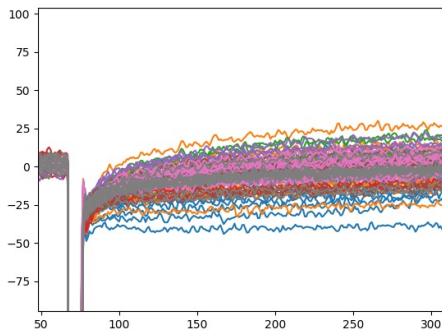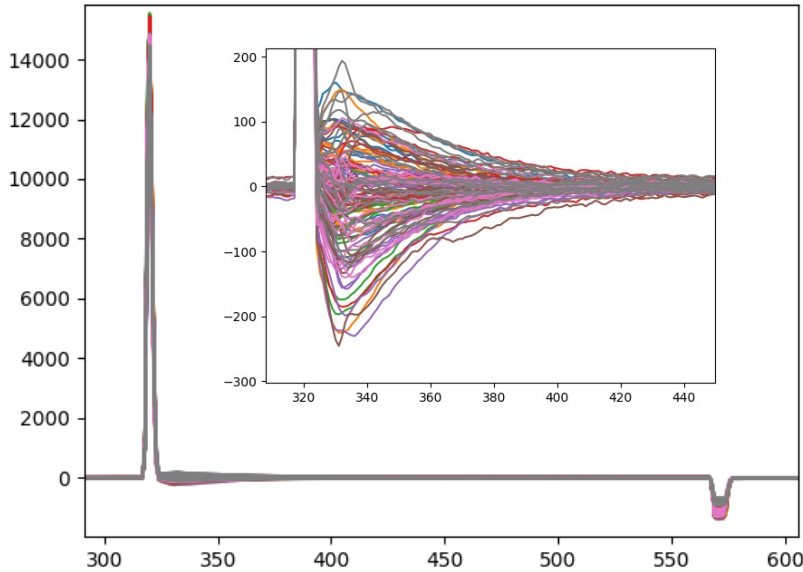Scope CH2(Red): Chip#0CH#0

200mV BL

Sagging of 1.8V power rail is observed

LN2: Chip#0CH#0 is selected for monitoring

- ## All channels are pulsed at 95 fC

VDDA&VDDP of CH64-CH127 tied together
VDDA&VDDP of CH0-CH63 tied together

Scope CH1(Blue): VDDA&VDDP for ch64-ch127
Scope CH3(Green): VDDP for ch0-ch63
Scope CH4(Pink): VDDA for ch0-ch63
Scope CH2(Red): Chip#0CH#0
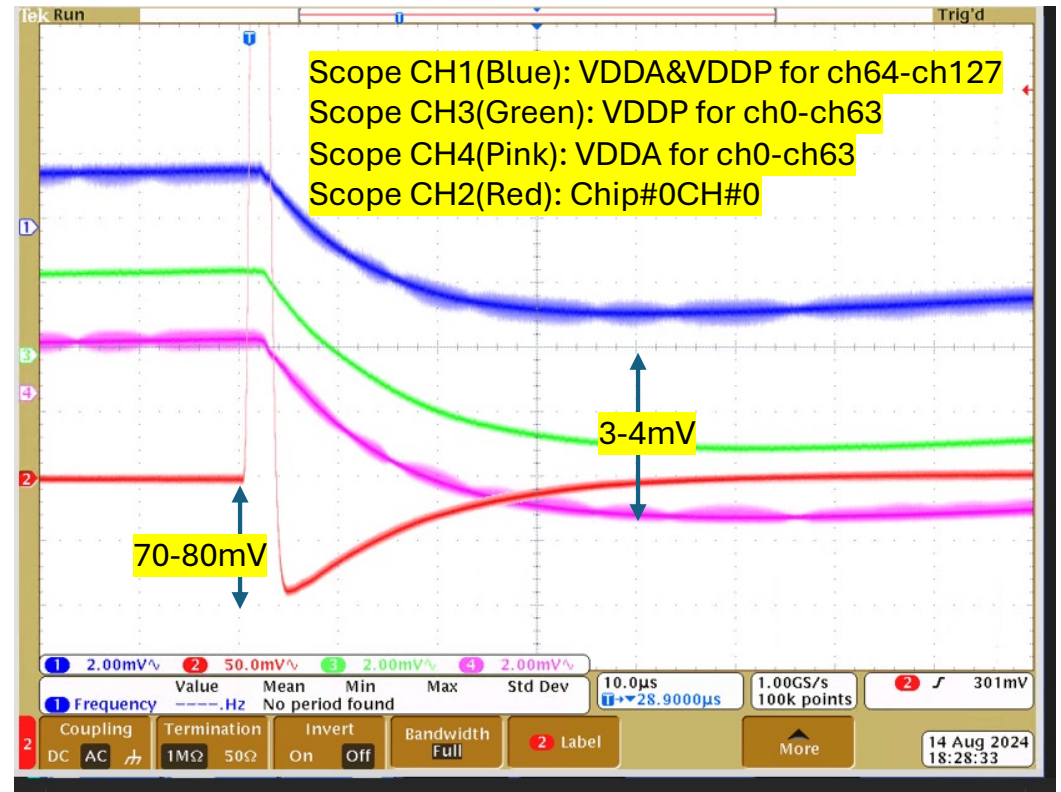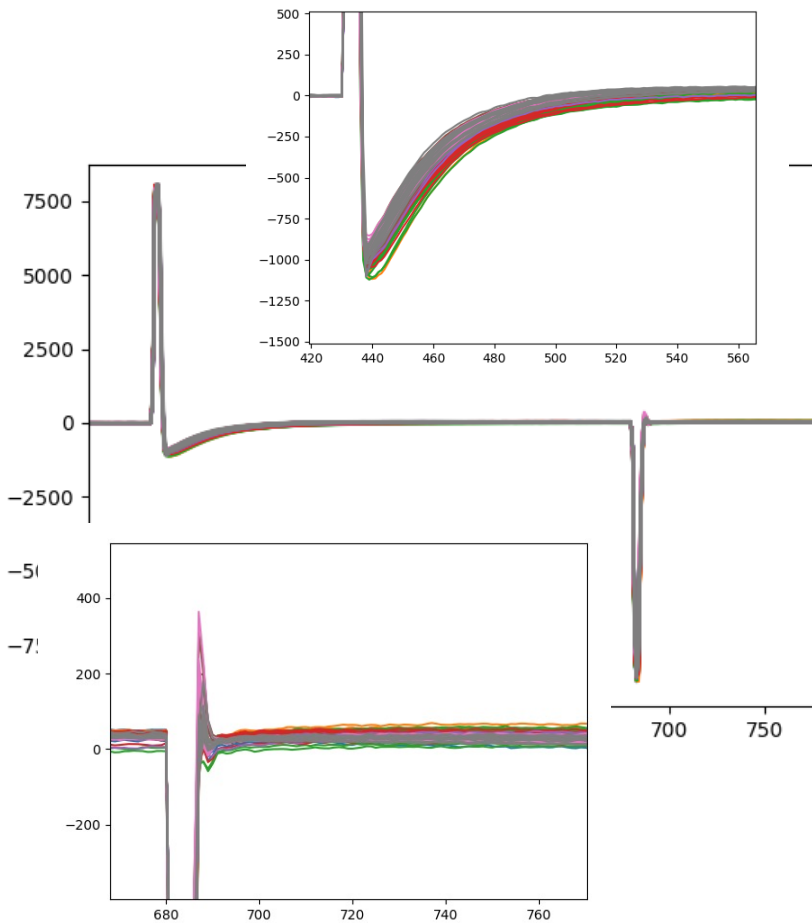
No obvious sagging of 1.8V power rail before FE saturation

LN2: Chip#0CH#0 is selected for monitoring

- All channels are pulsed at 218 fC

VDDA&VDDP of CH64-CH127 tied together
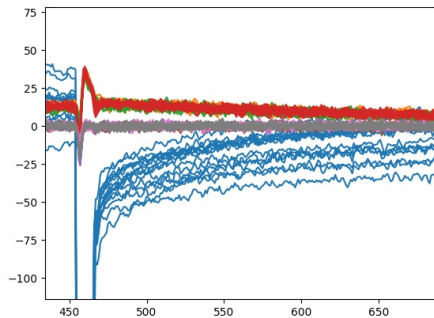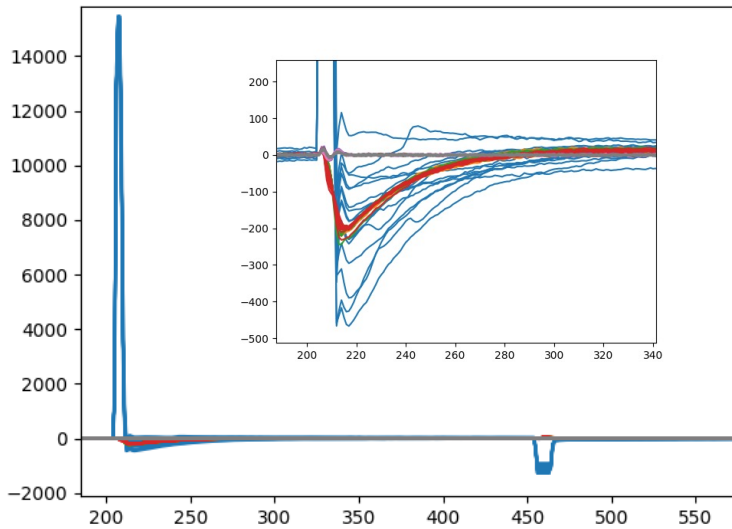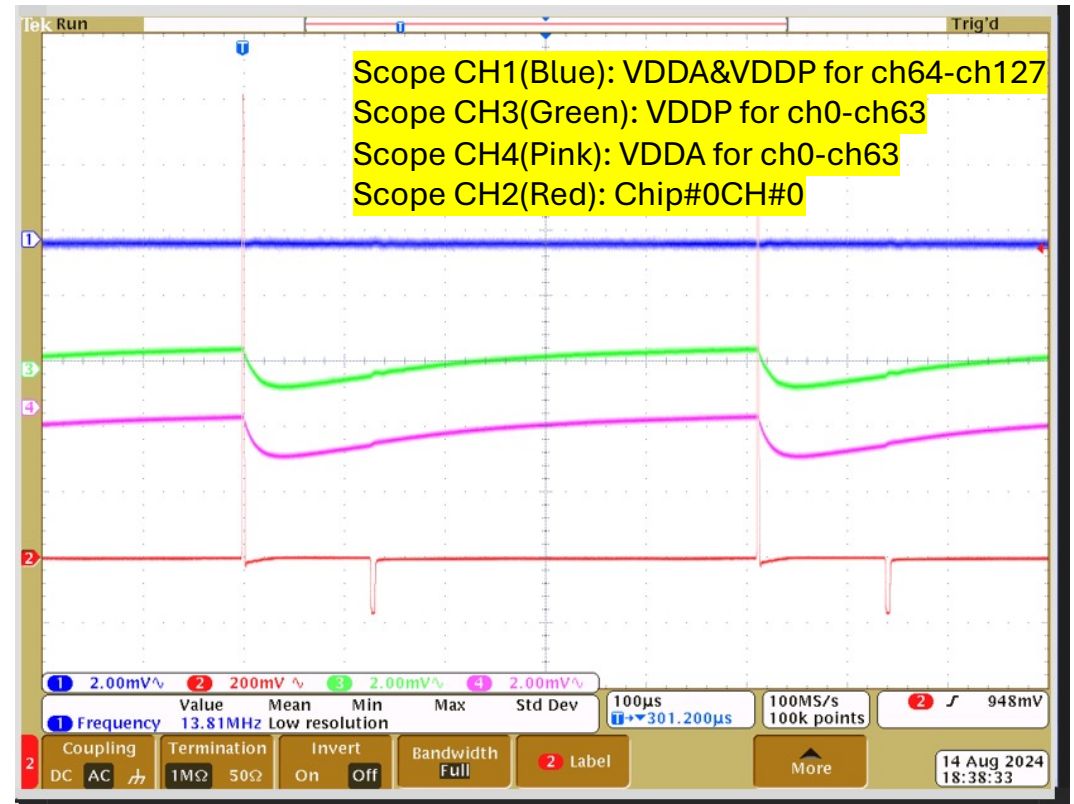VDDA&VDDP of CH0-CH63 tied together

Scope CH1(Blue): VDDA&VDDP for ch64-ch127
Scope CH3(Green): VDDP for ch0-ch63
Scope CH4(Pink): VDDA for ch0-ch63
Scope CH2(Red): Chip#0CH#0

3-4mV

70-80mV

Sagging of 1.8V power rail is observed

900 mV BL

Note: Negative tail is sensitive to insufficient power

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LN2: Chip#0CH#0 is selected for monitoring

- Chip#0(16 chns) is pulsed at 218 fC

VDDA&VDDP of CH64-CH127 tied together
VDDA&VDDP of CH0-CH63 tied together

200 mV BL

Scope CH1(Blue): VDDA&VDDP for ch64-ch127
Scope CH3(Green): VDDP for ch0-ch63
Scope CH4(Pink): VDDA for ch0-ch63
Scope CH2(Red): Chip#0CH#0

Sagging of 1.8V power rail is observed

- Negative tail is correlated to the sagging of power rails
- Many more detailed measurements are in backup slides
  - Similar observations with both internal and external calibration injections
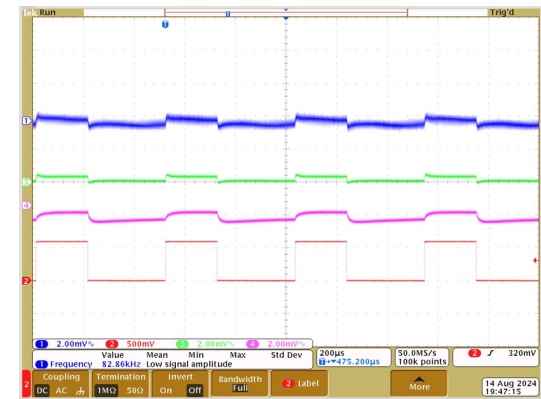
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Separate VDDP and VDDA

CH#0-63: VDDA & VDDP are separated
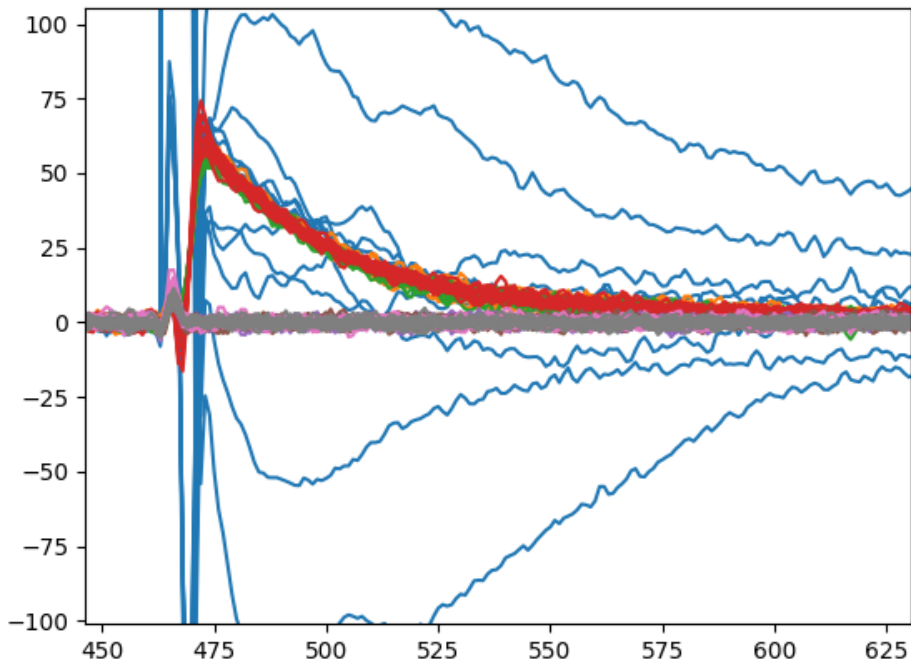
- External calibration pulser from WIB

14 mV/fC
185 fC

14 mV/fC
110 fC
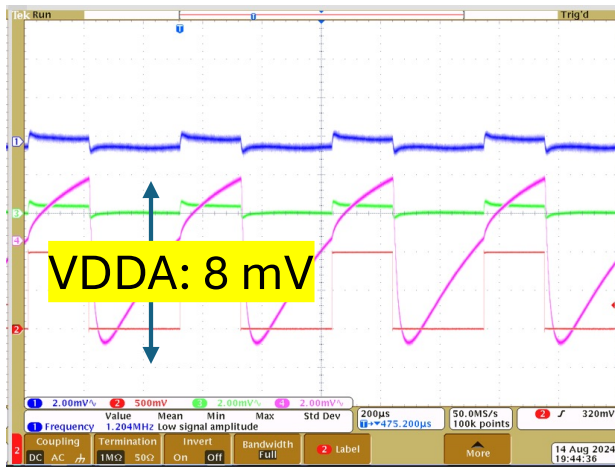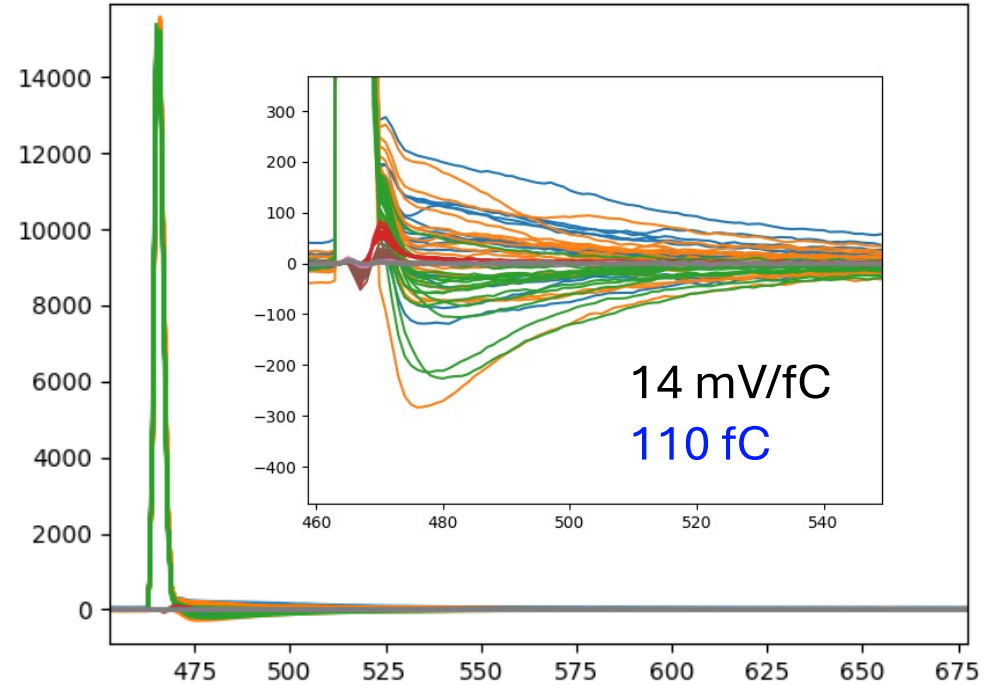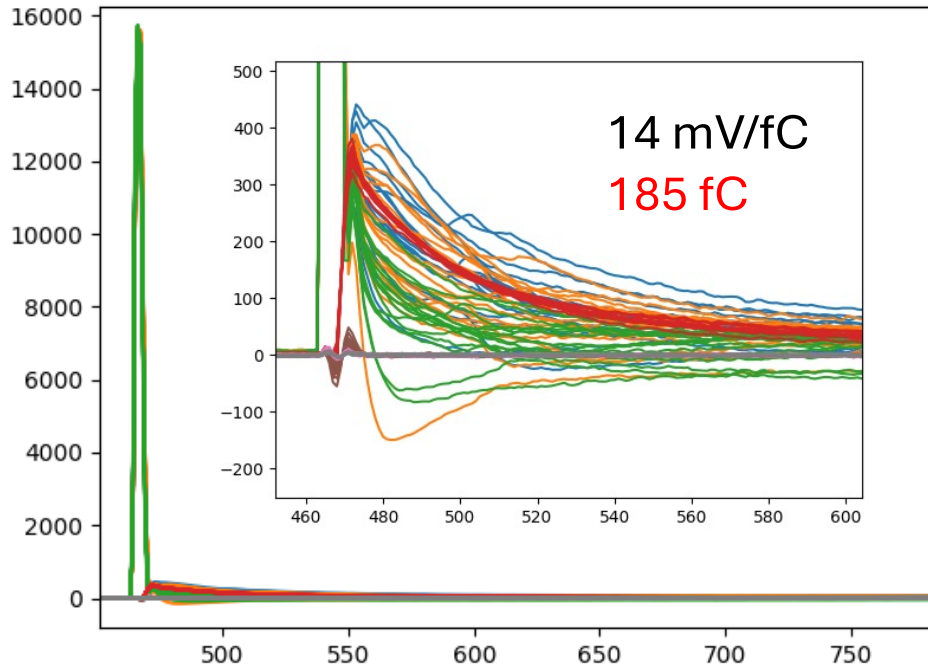
Chip#0,1,2 (48chns) are pulsed

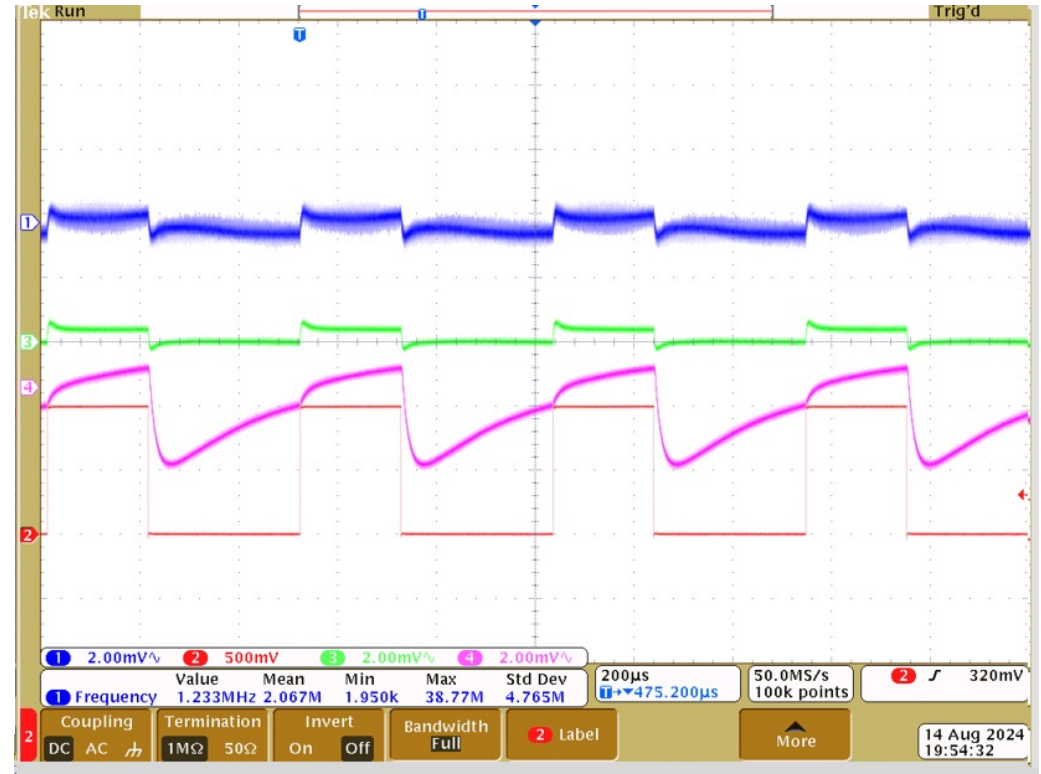Sagging of VDDA is observed

VDDA: 8 mV

CH#0-63: VDDA & VDDP are separated
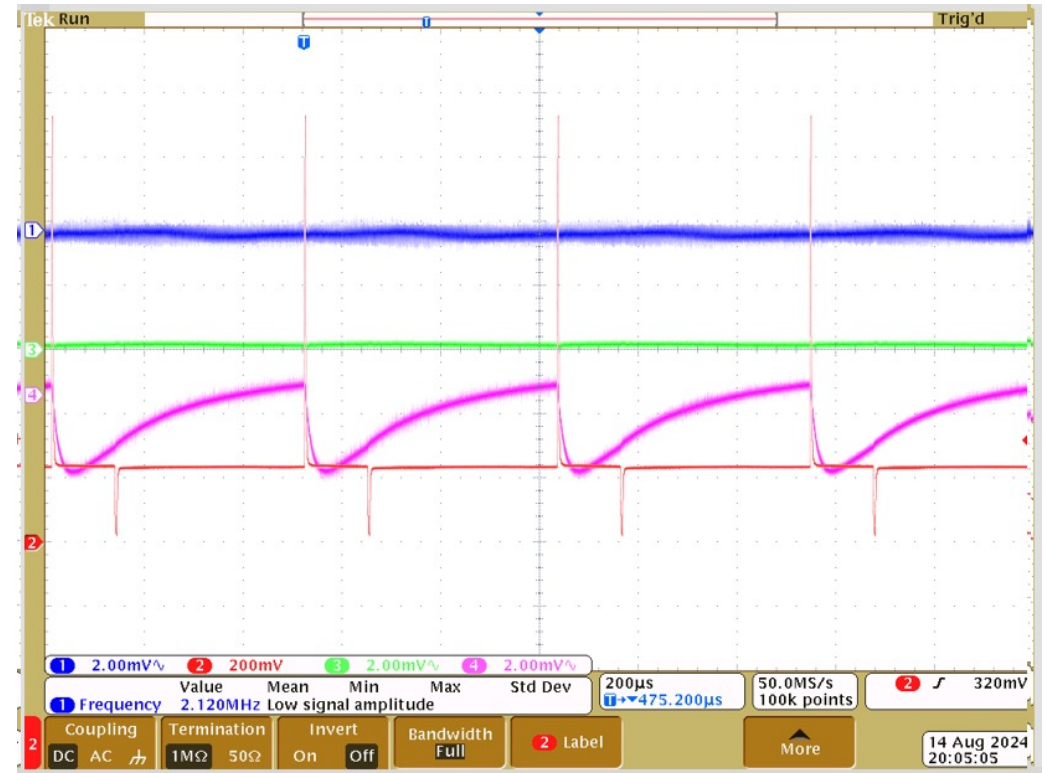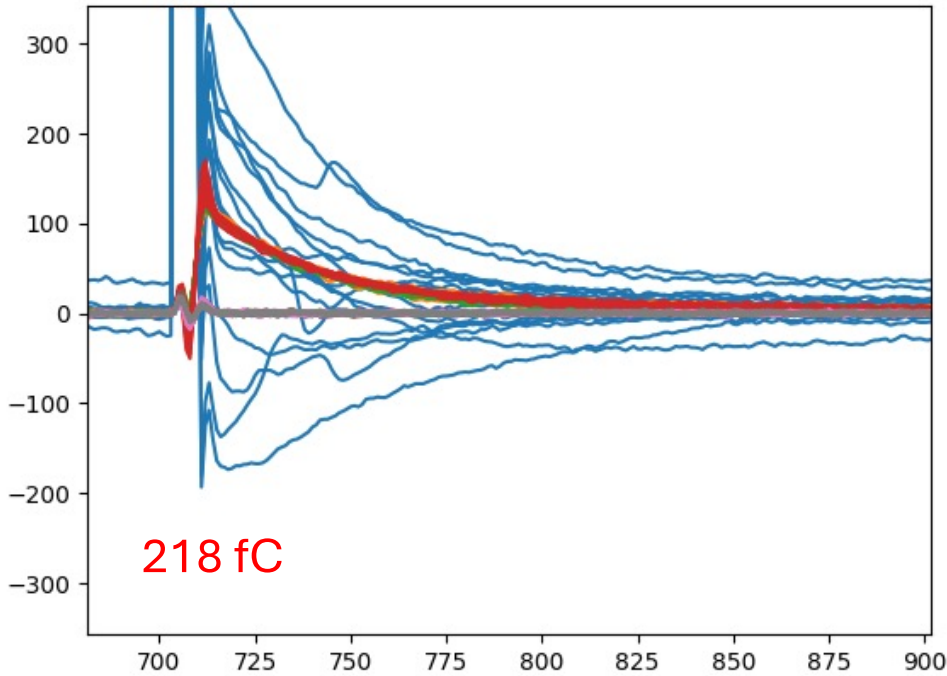
- Chip#0 (8chns) are pulsed

1000 mV (185 fC)

- Long tail is correlated to the sagging of VDDA (shaper)
- Separation of VDDP and VDDA changes the tail polarity, positive tail is observed with slightly reduced amplitude

Adjust RC filter

CH#0-63: VDDA & VDDP are separated

- Chip#0 (16chns) are pulsed with LArASIC-DAC

218 fC
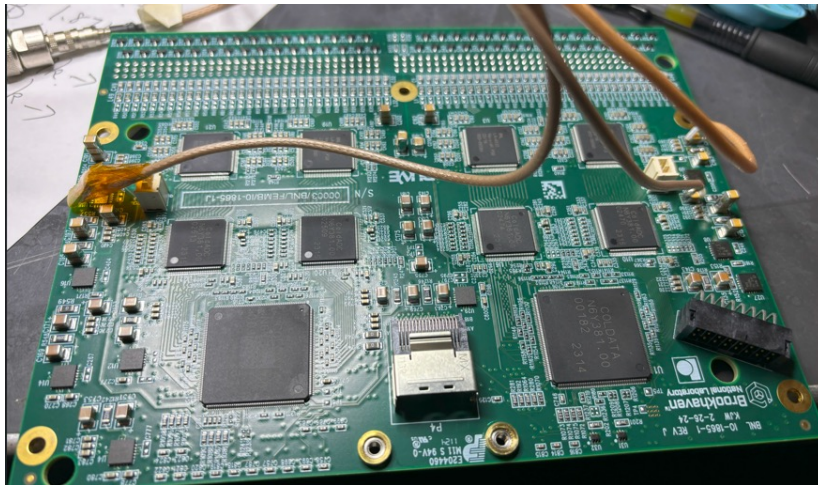
RC filter: R = 1 Ohm

CH#0-63: VDDA & VDDP are separated

- Chip#0 (16chns) are pulsed by signal generator (185 fC)
  - Power rail VDDA recovers faster with smaller R, but the long tail doesn't decrease significantly
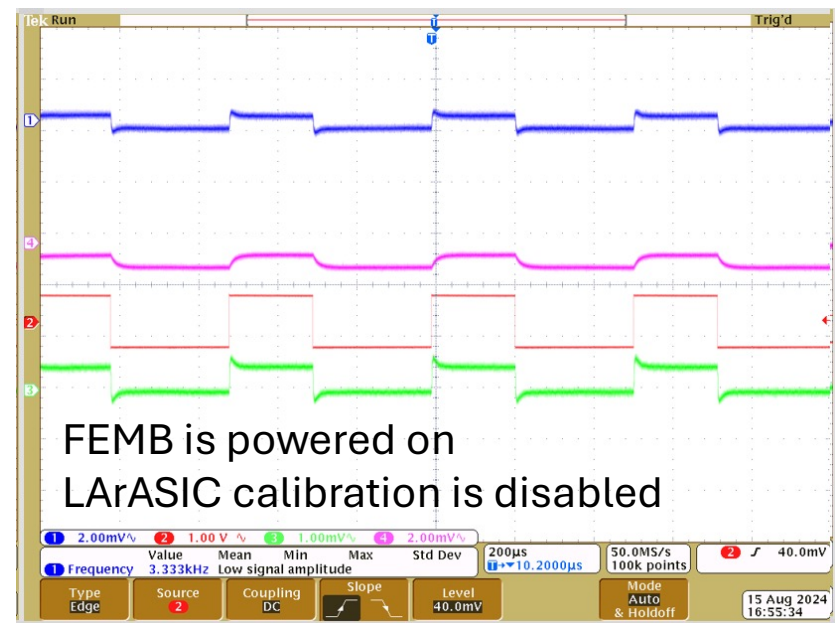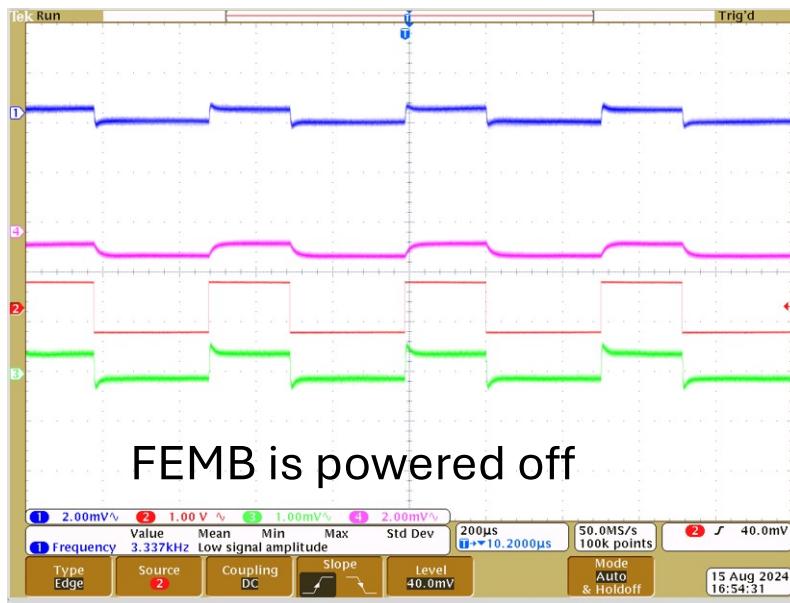

(16 channels are pulsed)
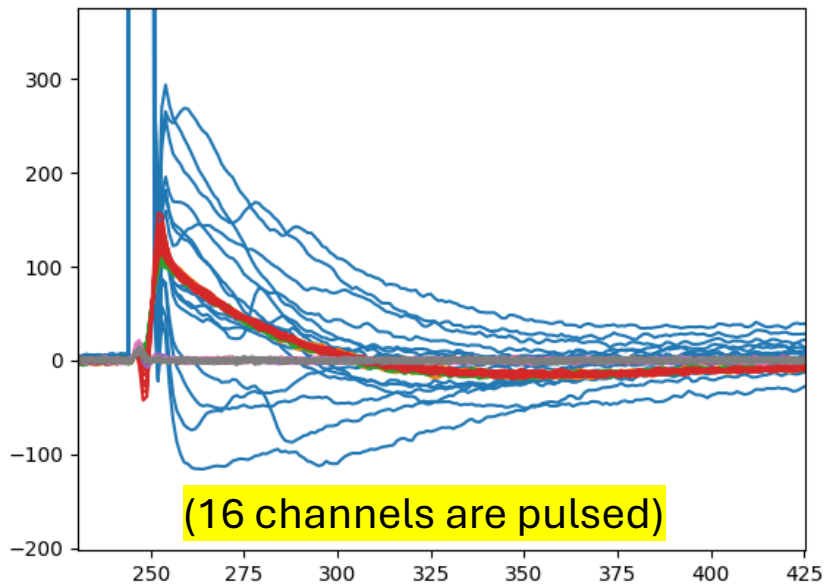
RC filter: VDDA R = 0.1Ohm

(16 channels are pulsed)
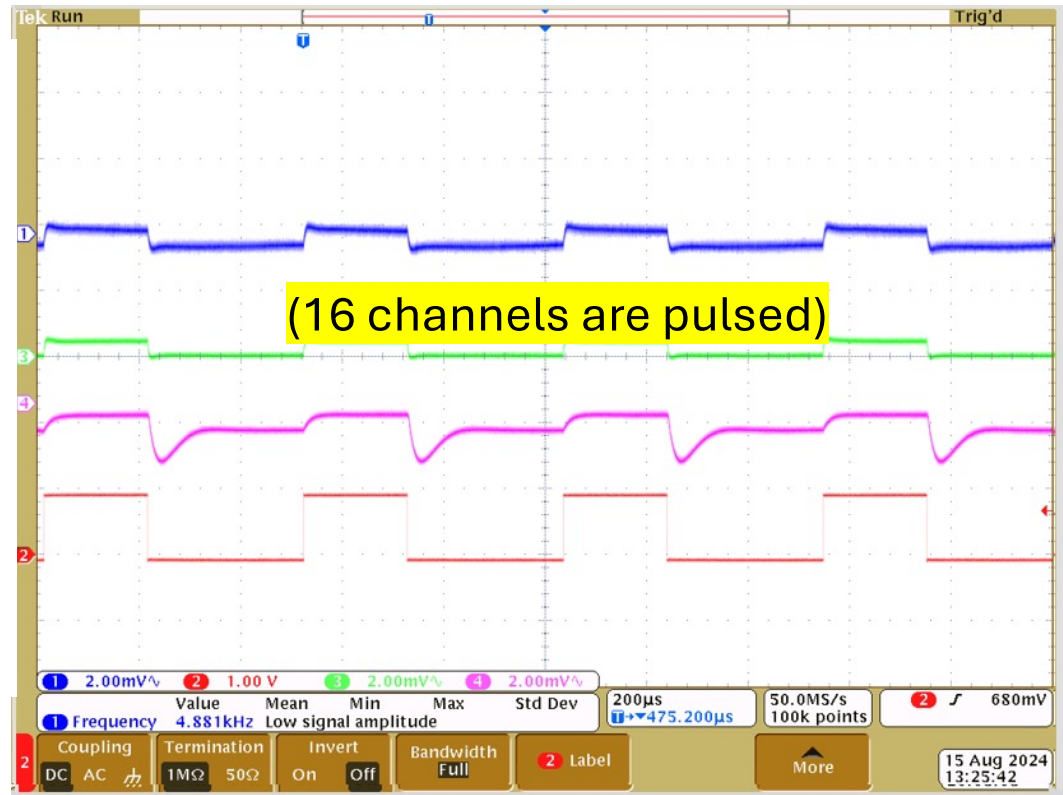
Experiment more 330 uF capacitors

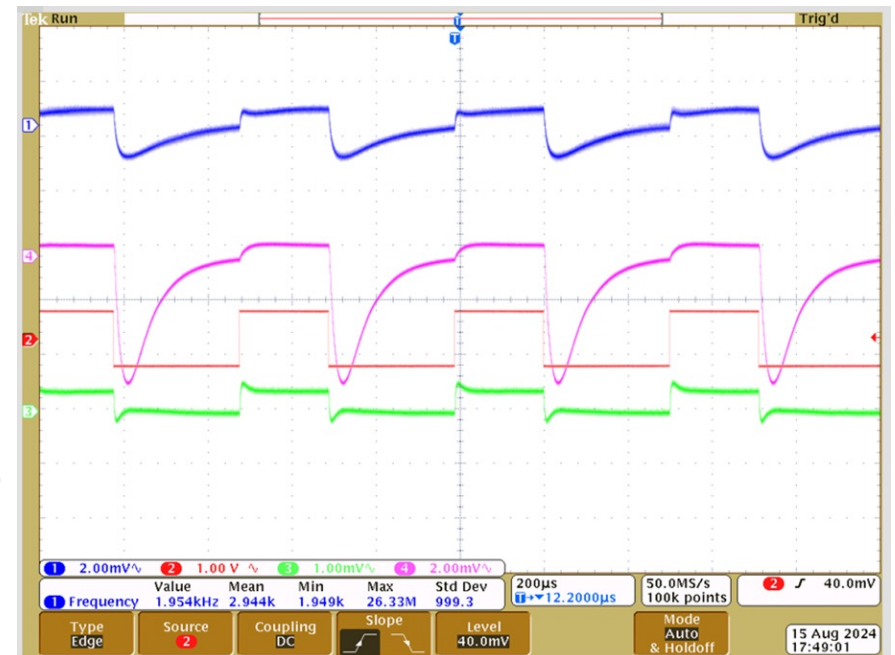- External Pulser from Signal Generator: Note coupling of scope channels

FEMB is powered off

FEMB is powered on
LArASIC calibration is disabled

External Pulser from Signal Generator

- Chip#1,2,3,5,6,7 are pulsed at 185 fC

Chip#0: blue

Chip#4: Purple
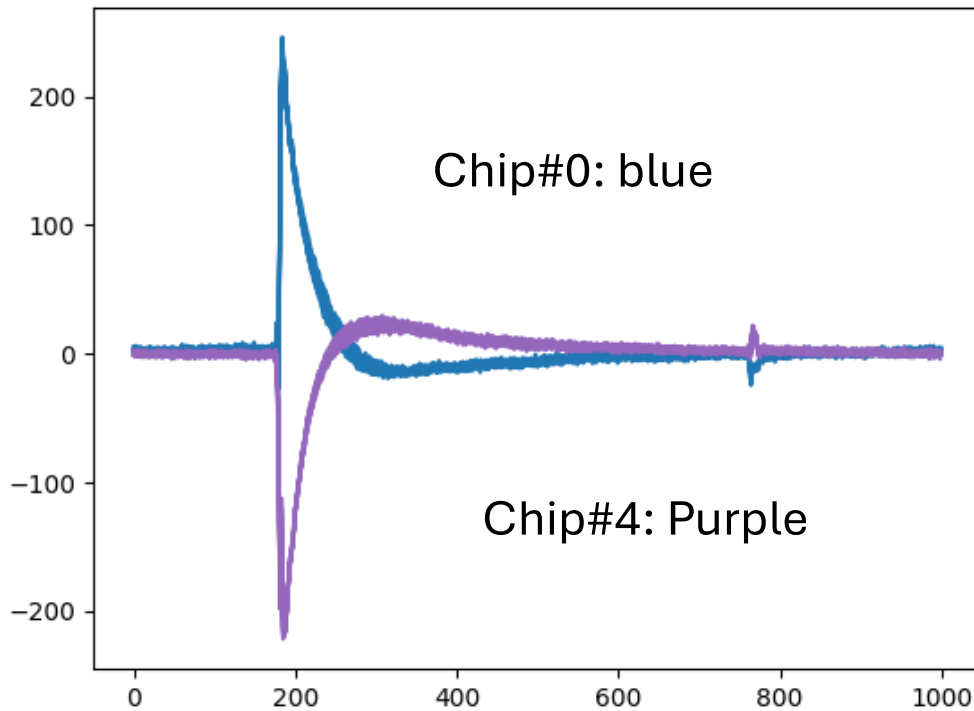
VDDA for chip0-3: 0.1 Ohm, 2x C
VDDP for chip0-3: 0.1 Ohm, 1x C
VDDA/VDDP (tied together) for chip 4-8: 0.1Ohm, 3x C

Scope CH1(Blue): VDDA&VDDP for ch64-ch127
Scope CH3(Green): VDDP for ch0-ch63
Scope CH4(Pink): VDDA for ch0-ch63
Scope CH2(Red): CH#0

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External Pulser from Signal Generator

- Chip#1,2,3,5,6,7 are pulsed at 185 fC

VDDA for chip0-3: 0.1 Ohm, 4x C
VDDP for chip0-3: 0.1 Ohm, 1x C
VDDA/VDDP (tie together) for chip 4-8: 0.1Ohm, 3x C

Chip#0: blue

Chip#4: Purple
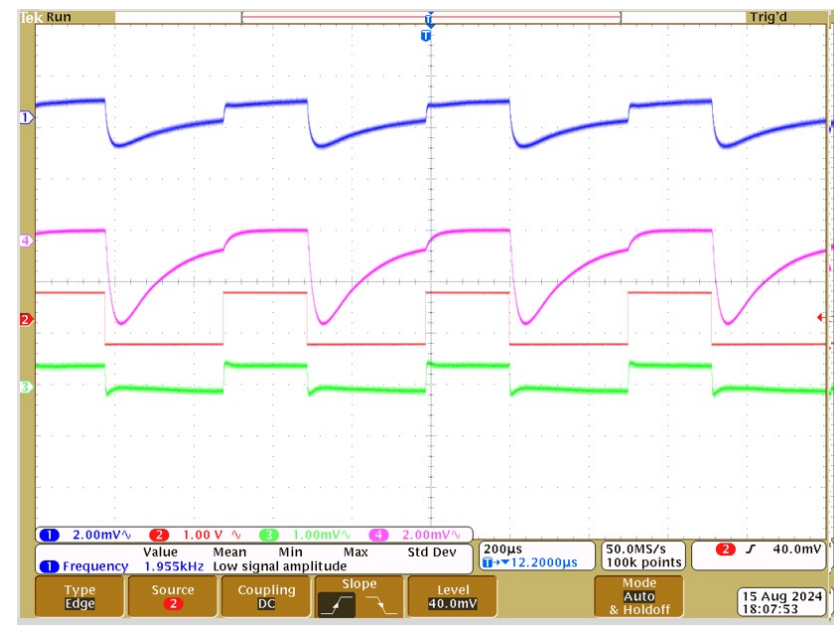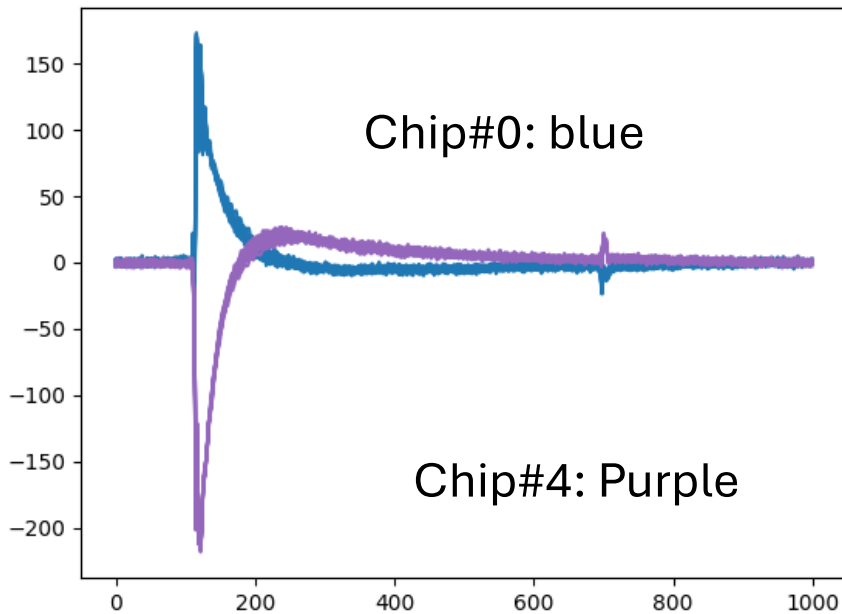
- Many more detailed measurements are in backup slides

- Adding capacitors can help mitigate the long tail

- However, FEMB has very little room to add twice or even four times of capacitors

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Summary

- Negative tail of the half FEMB observed in NP04 has been re-produced in lab bench tests
  - Negative tail shows up when channel enters saturation
  - The amplitude of negative tail becomes larger when more channels are deeply saturated
- Investigation shows the negative tail is correlated to the sagging of VDDA when FE channel is deeply saturated
  - Separate VDDA and VDDP will change the polarity of long tail, although which is not recommended from the FE ASIC design
    - See page 23 of the ASIC FDR document
    - https://edms.cern.ch/ui/file/2314428/2/LArASICDevelopment.20210714_docx_cpdf.pdf
  - Adjustment of RC filter, particularly adding capacitors, helps mitigate the long tail but can't eliminate it
  - Adding more capacitors on FEMB would be challenging
- Proposed next steps
  - Reduce the gain of FE ASIC to 7.8 mV/fC will extend the dynamic range and reduce the probability of saturation
    - Collection plane ~180 fC and induction plane ~90 fC
    - Impact on physics analysis to be evaluated
  - Data processing to make offline correction of negative tail could be explored, related to the crosstalk and pole-zero cancellation studies

Backup Slides

LN2: CH#0 is pulsed with 218 fC

- sgp=1, dac=0x3f (**218 fC**), 14 mV/fC, chip#0 CH#0 (other 900mV BL)
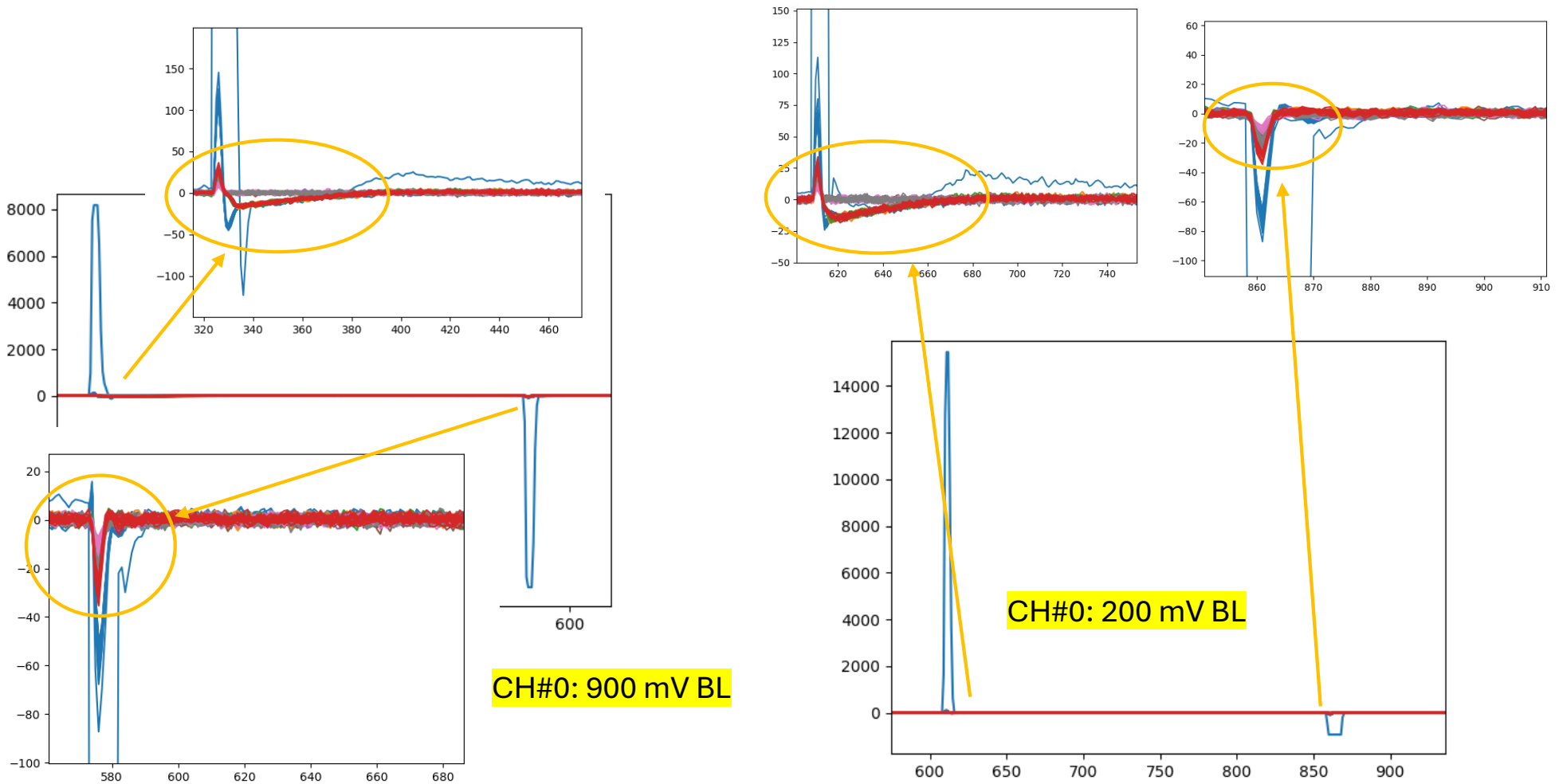
CH#0: 900 mV BL

CH#0: 200 mV BL

At LN2, even only one channel is deeply saturated, other channels on the same half FEMB show negative tail

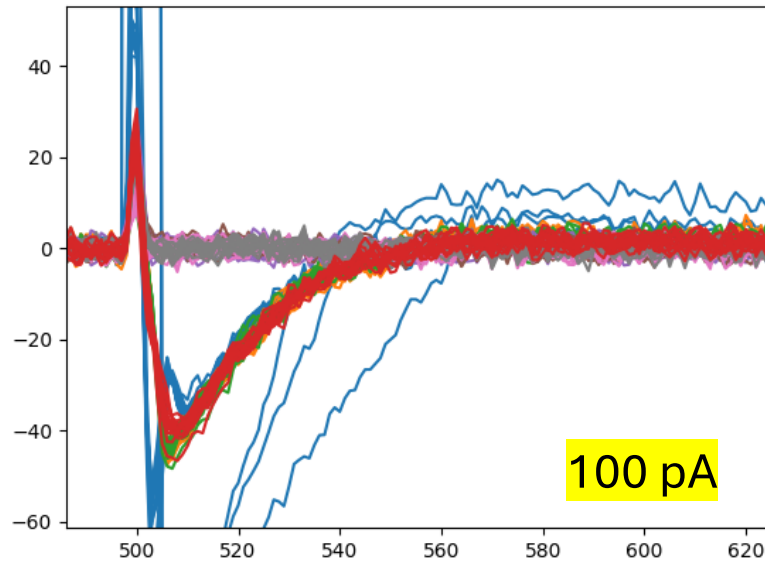# LN2: pulsed with 218 fC, 2 chns vs. 3 chns

- sgp=1, dac=0x3f (**218fC**), 14 mV/fC, chip#0 200 mV BL (other 900mV BL)

CH#0,1 are pulsed

CH#0,1,2 are pulsed
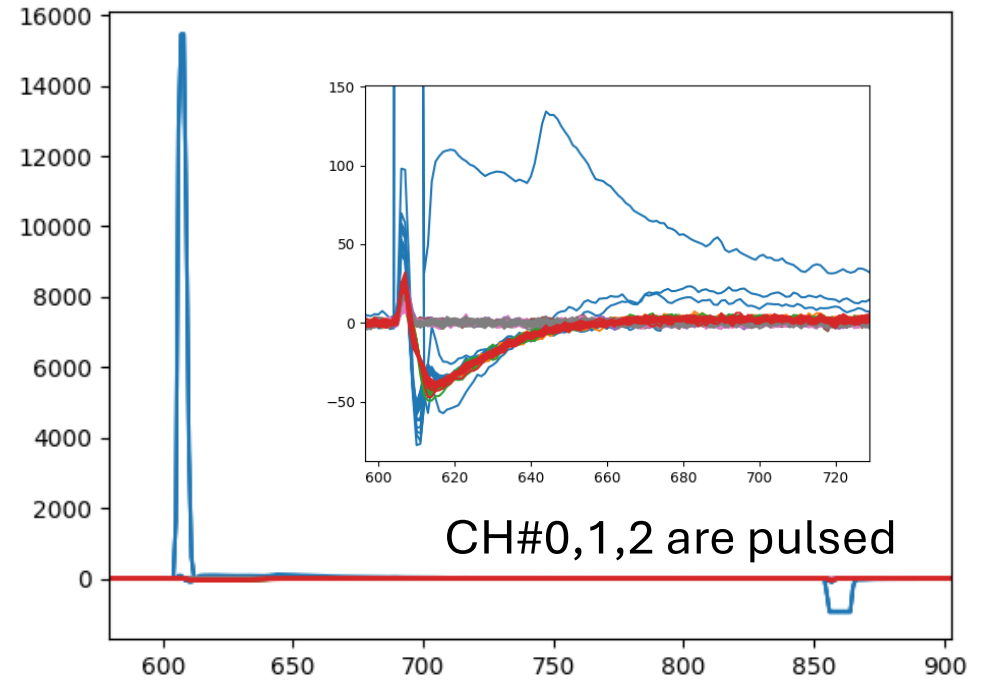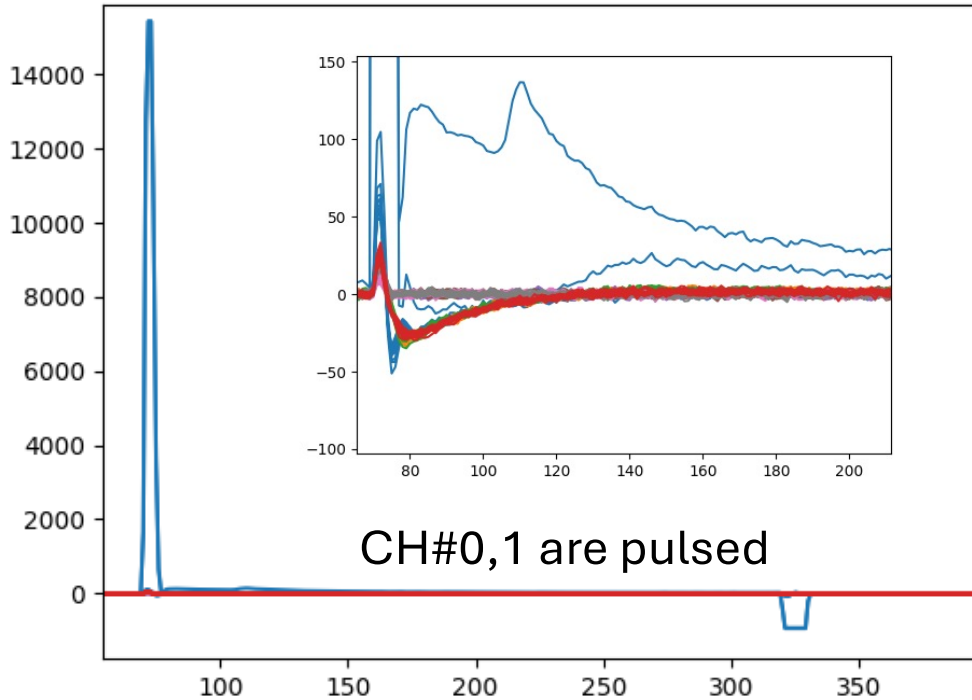
The amplitude of negative tail becomes larger when more channels are deeply saturated.

LN2: 3 chns pulsed with 218 fC, different leakage current settings
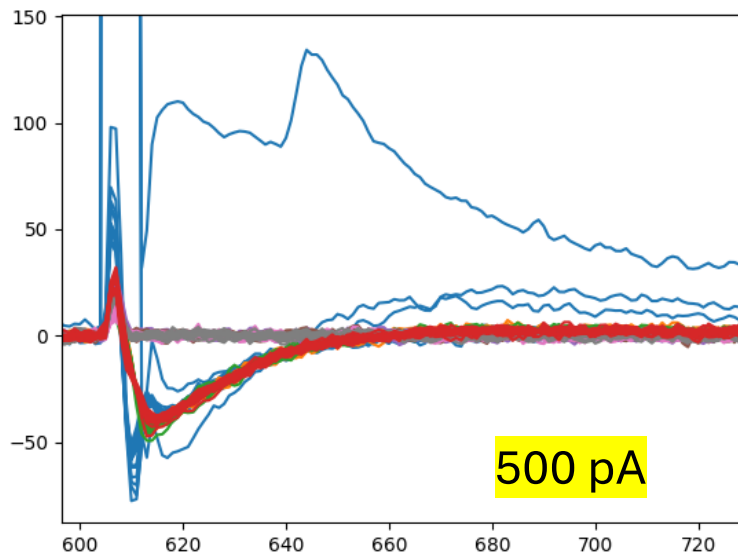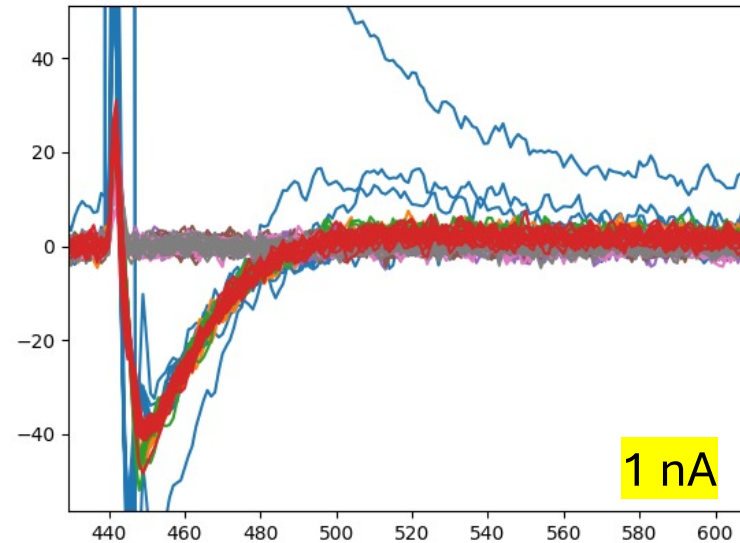
Changing leakage current setting doesn't affect the negative tail much, though it affects the pole-zero cancellation behavior of pulsed channels.

LN2: 3 chns pulsed with 218 fC, different gains
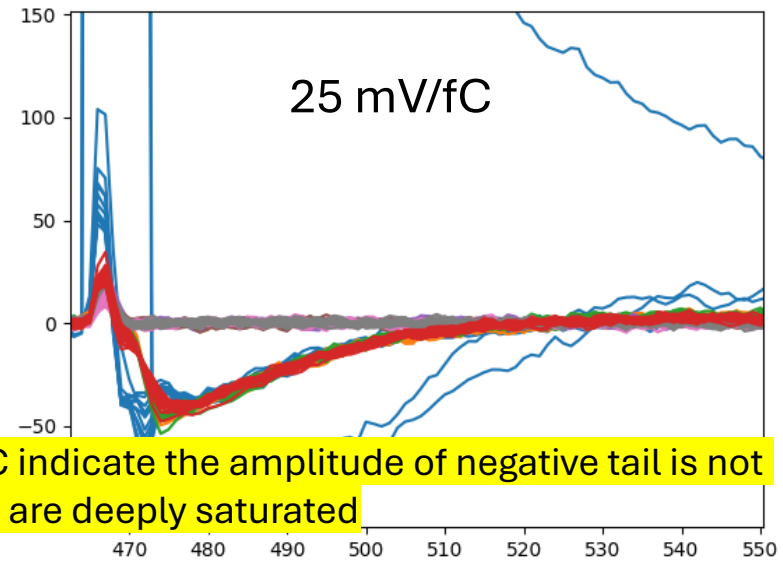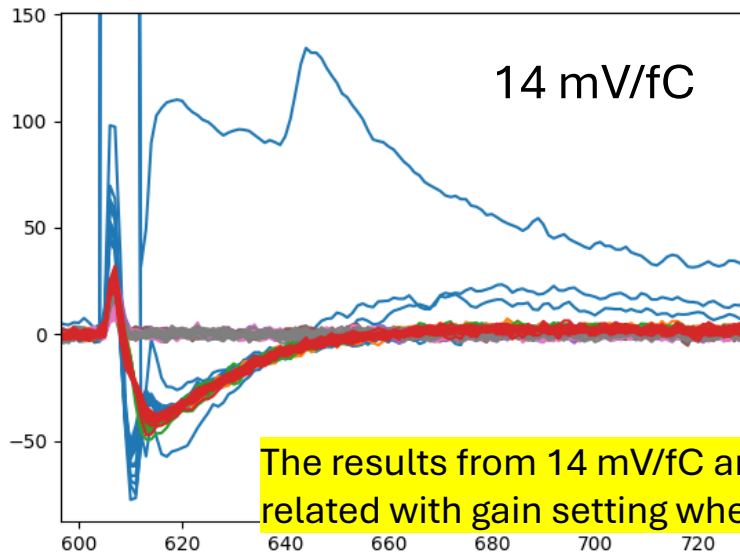
14 mV/fC

25 mV/fC

The results from 14 mV/fC and 25 mV/fC indicate the amplitude of negative tail is not related with gain setting when channels are deeply saturated

7.8 mV/fC

4.7 mV/fC, not saturated yet
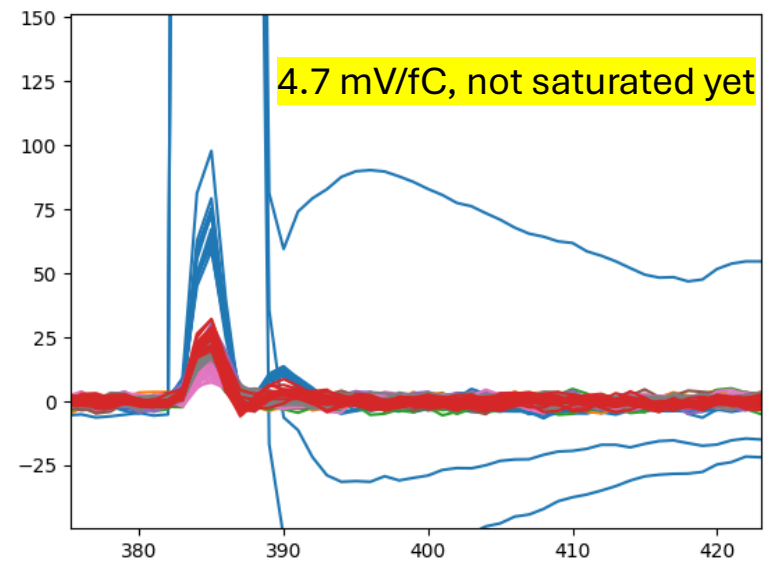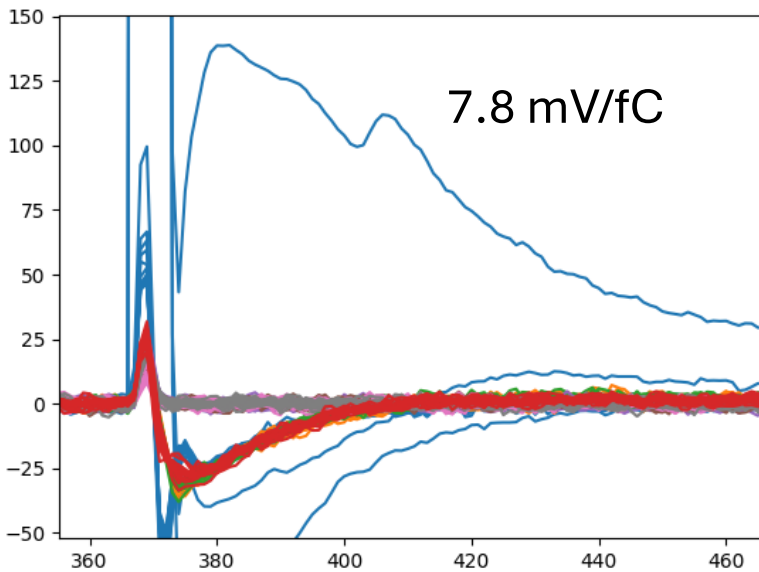
LN2: 3 chips (48 chns) are pulsed

- sgp=1, dac=0x3f

4.7 mV/fC
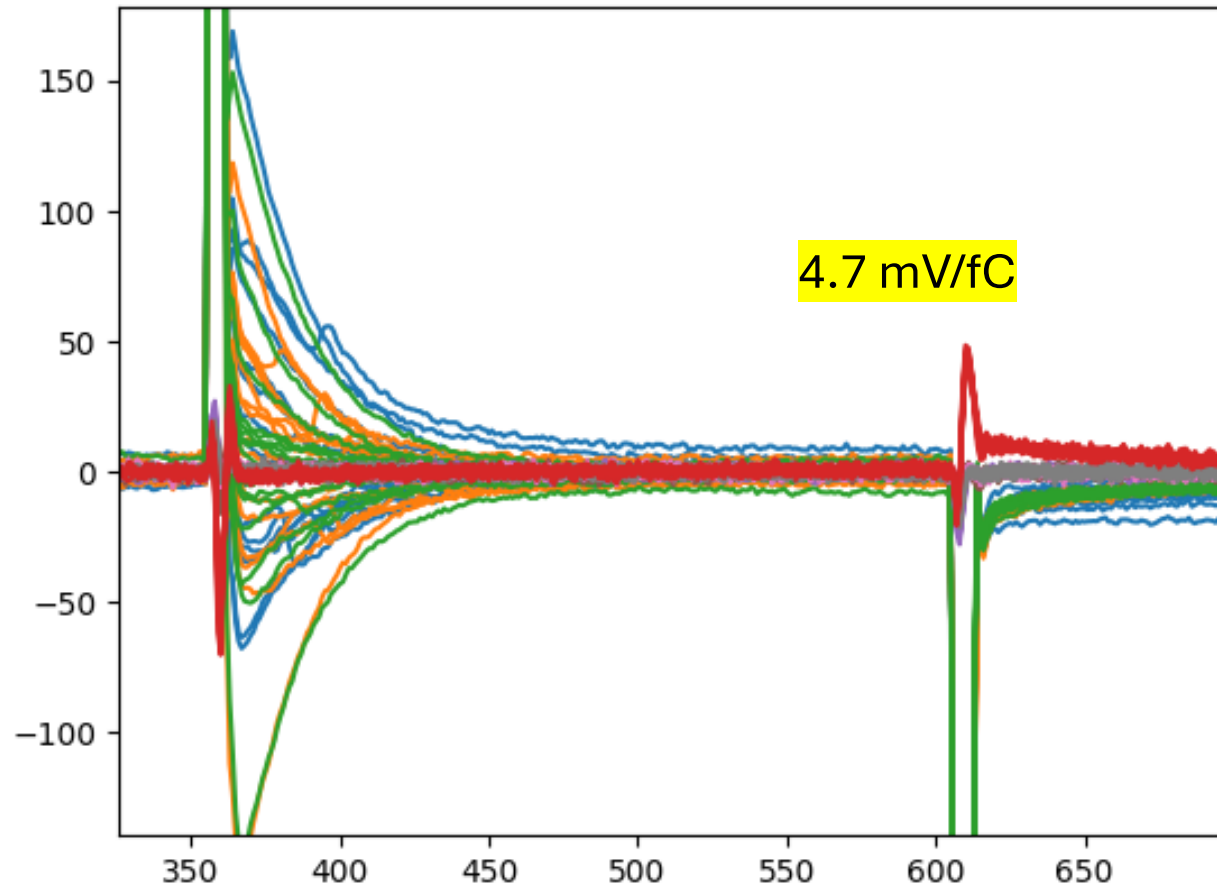
Negative tail is not significant

LN2: 3 chips (48 chns) are pulsed at 218 fC

- Different peaking times (>= 1us) have minimum impact
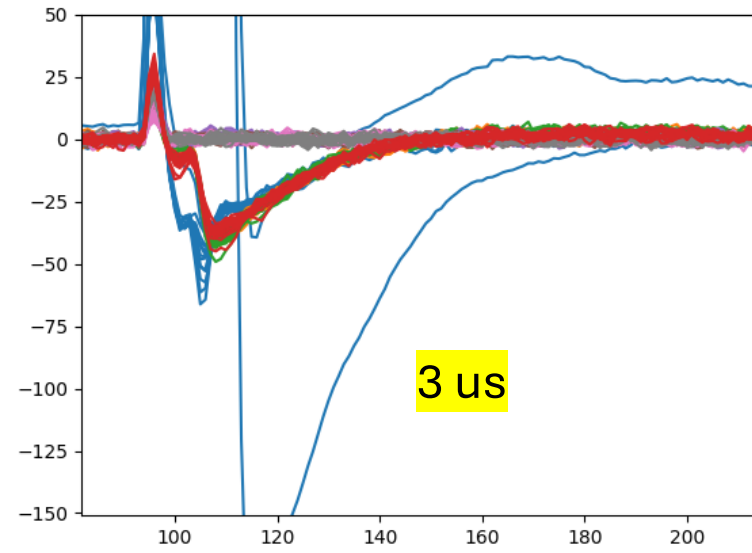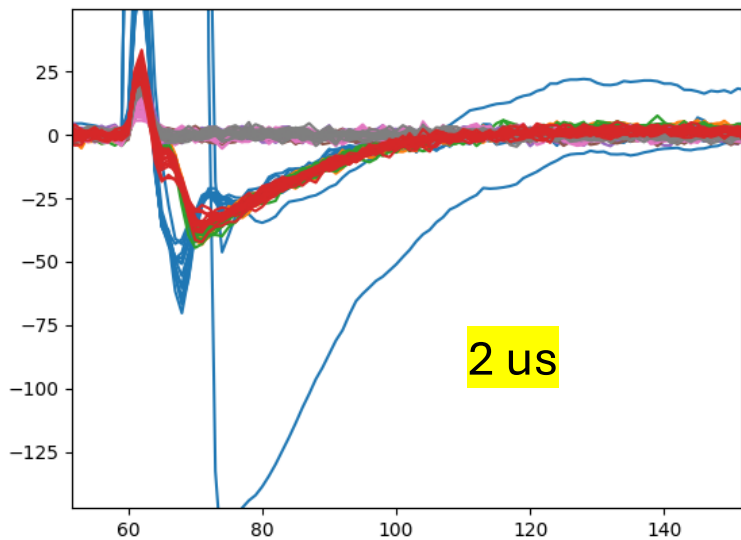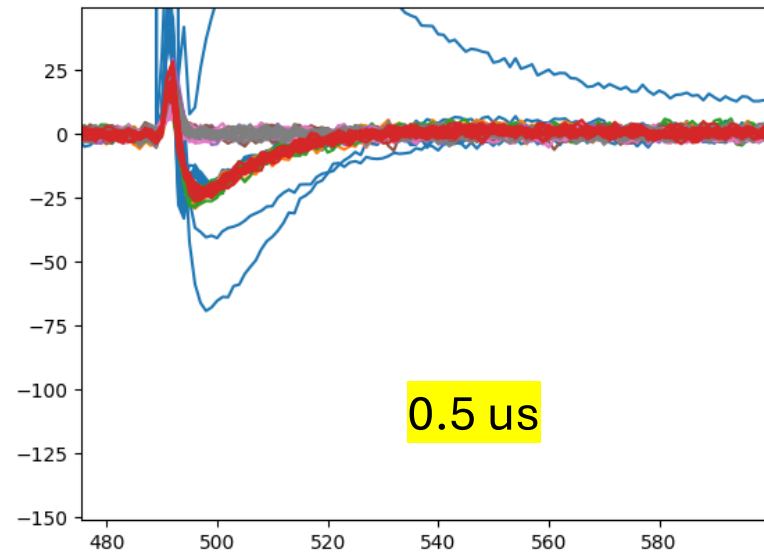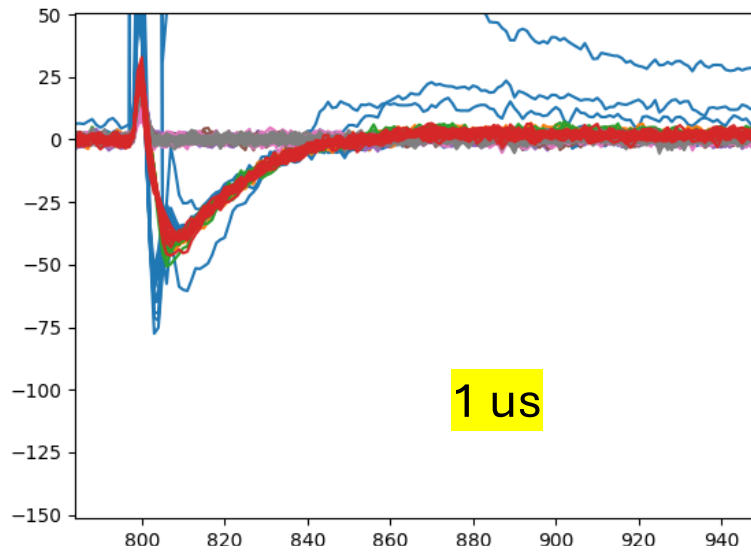
LN2: all channels are pulsed at 218 fC
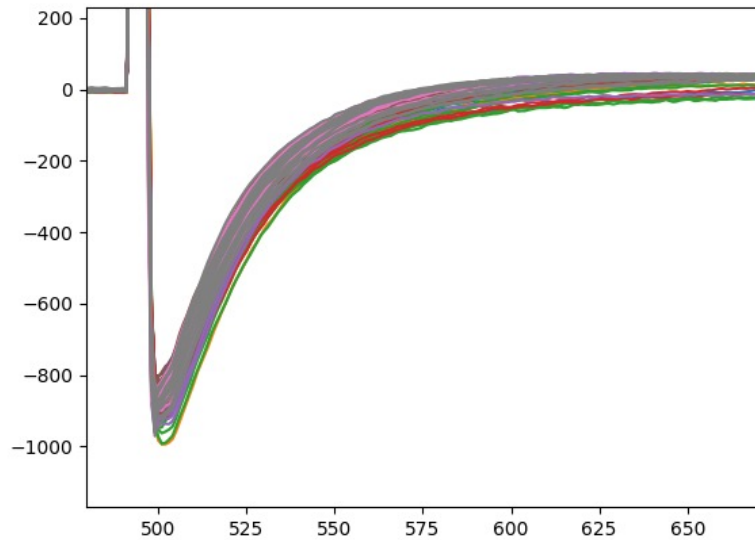
14 mV/fC, SE and SDF off
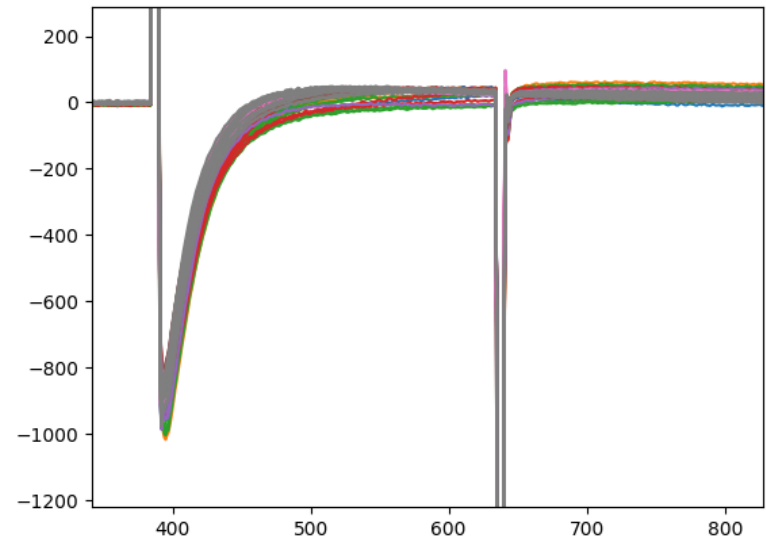
14 mV/fC, SE and SDF on

14 mV/fC, DIFF on

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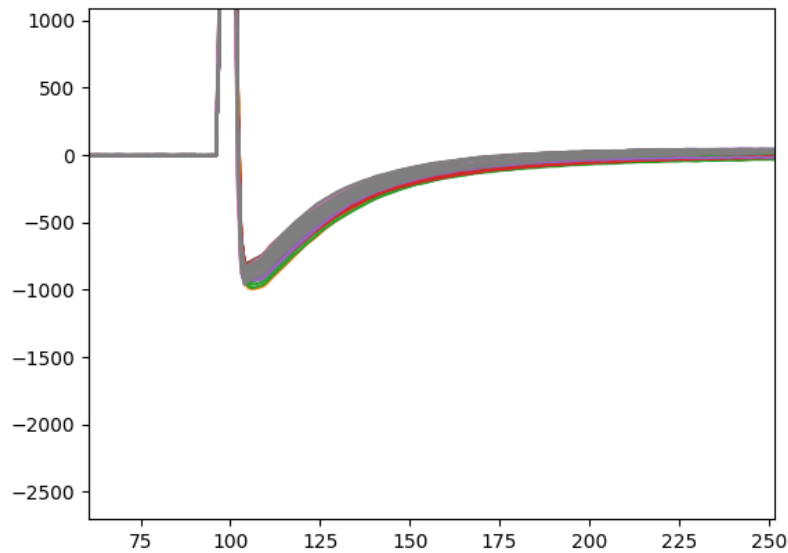
LN2: External calibration pulser from signal generator

- 540 mV * 185 fF = 100 fC, 14 mV/fC
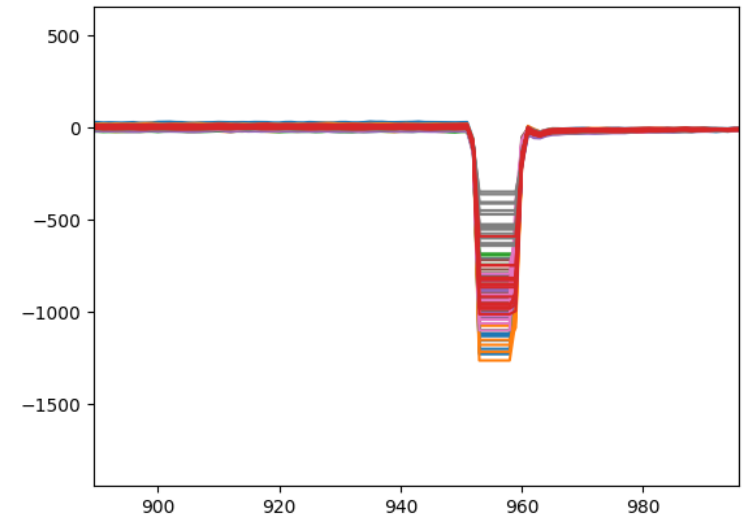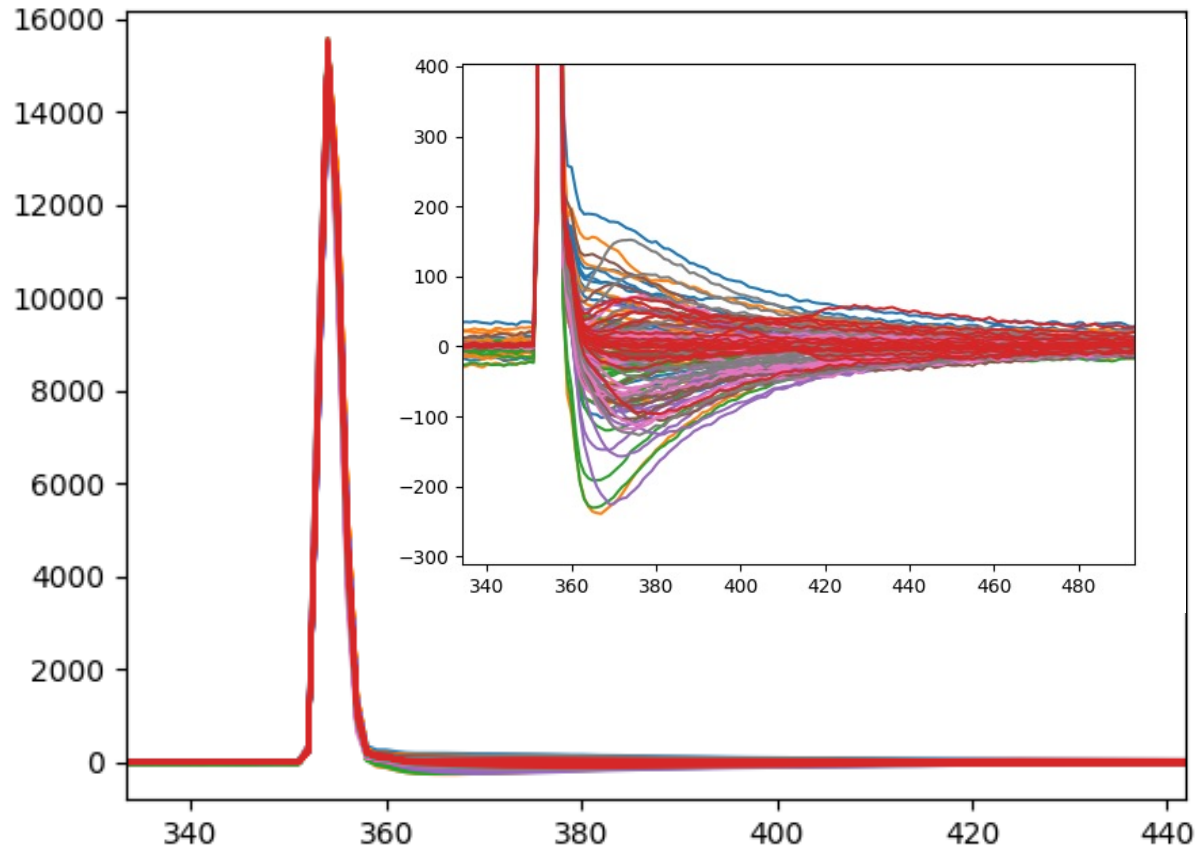
LN2: External calibration pulser from signal generator

- 3 chns are pulsed

540 mV * 185 fF = 100 fC, 14 mV/fC

1080 mV * 185 fF = 200 fC, 14mV/fC

1620 mV * 185 fF = 300 fC , 14 mV/fC
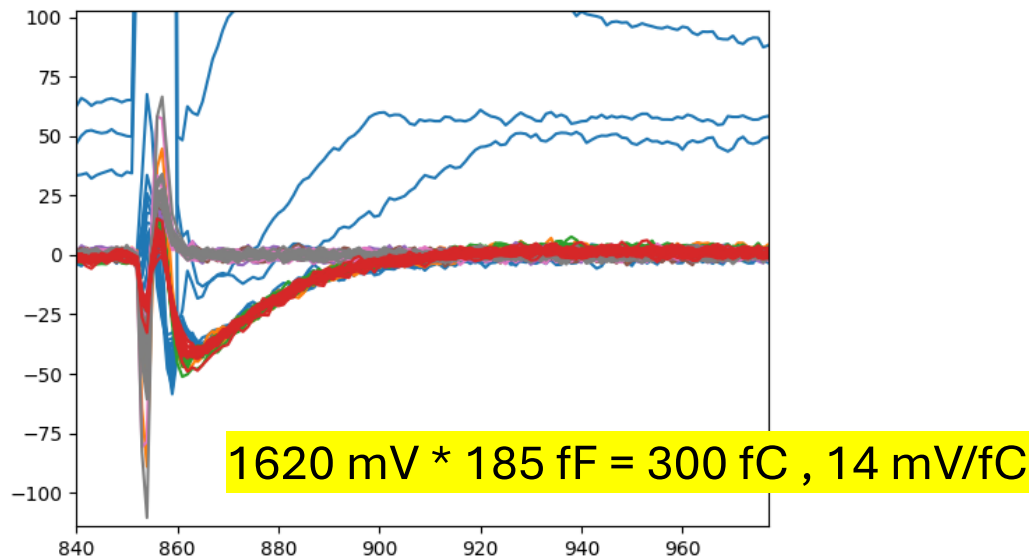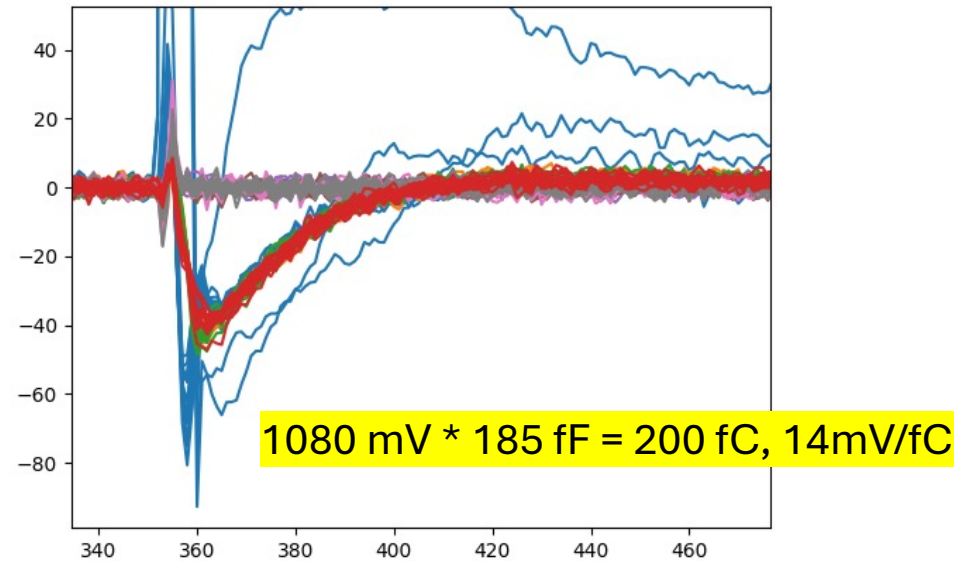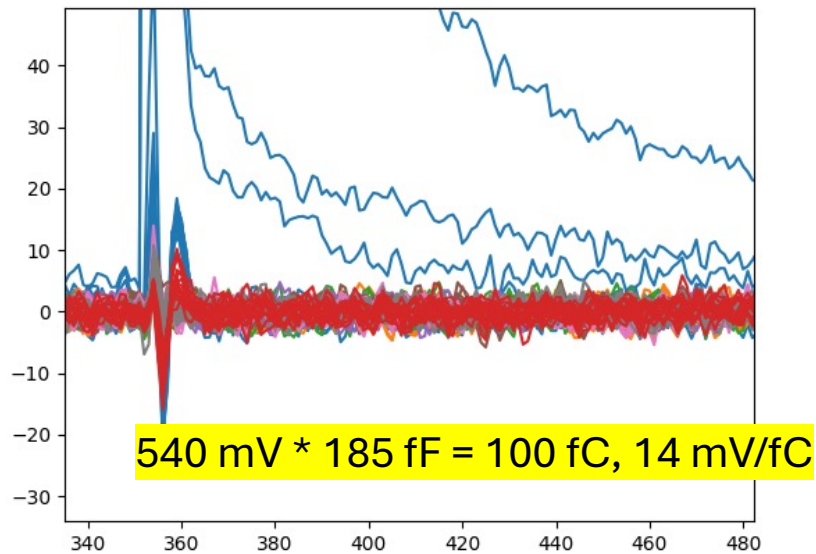
LN2: External calibration pulser from signal generator

- **3 chips (48 chns)** are pulsed   1080 mV * 185 fF = 200 fC, 14 mV/fC

Ch64-127

Chip#3 red plots
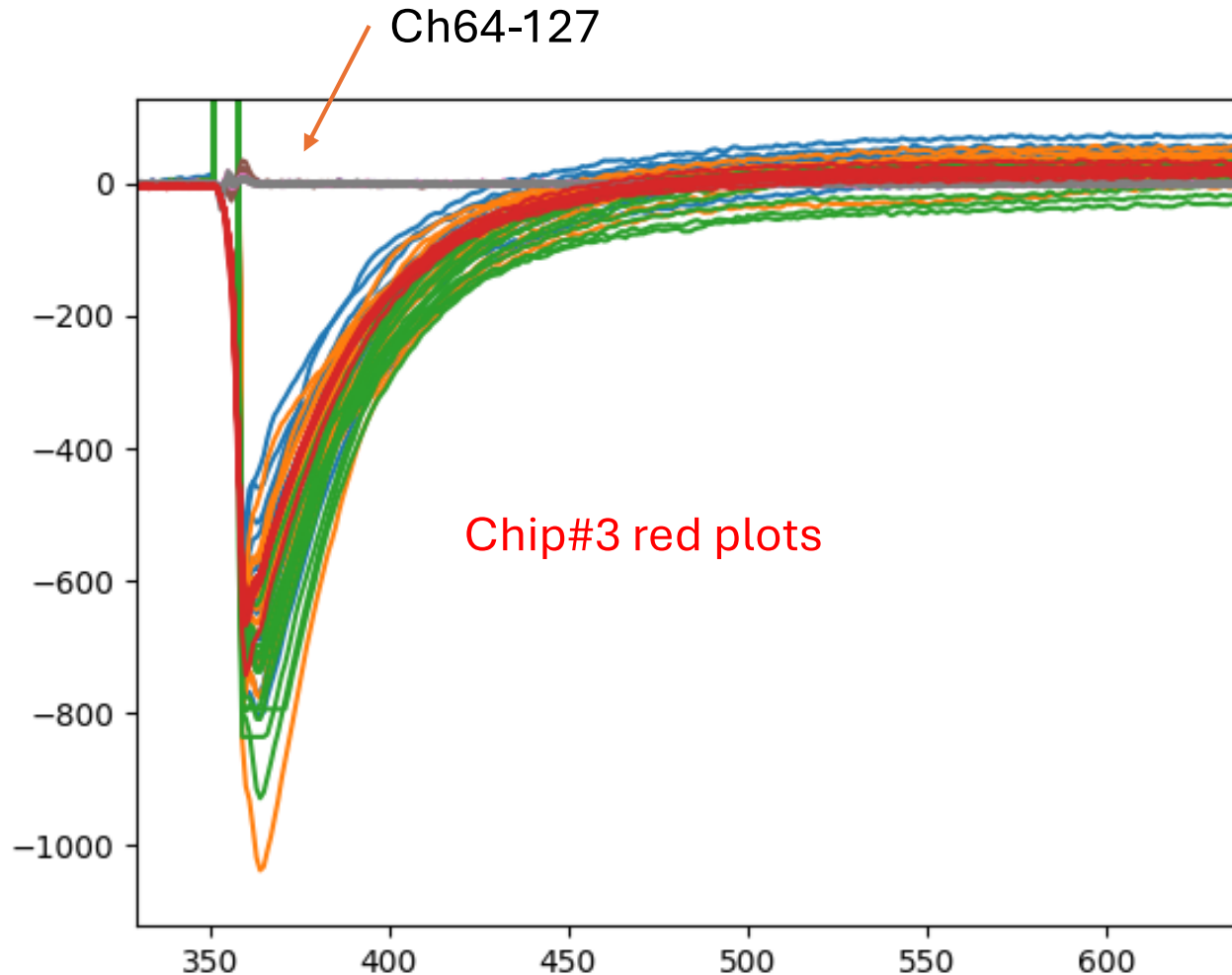
It offers a hint that the negative tail could be corrected via offline processing

LN2: Chip#0CH#0 is selected for monitoring

- All channels are pulsed at 218 fC

VDDA&VDDP of CH64-CH127 tied together
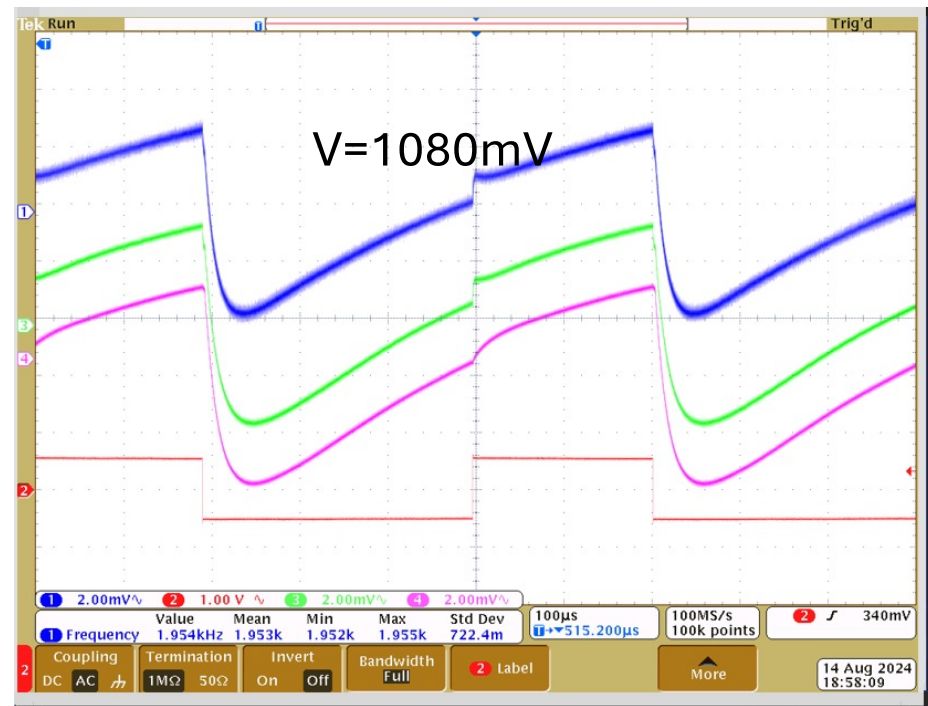VDDA&VDDP of CH0-CH63 tied together

Scope CH1(Blue): VDDA&VDDP for ch64-ch127
Scope CH3(Green): VDDP for ch0-ch63
Scope CH4(Pink): VDDA for ch0-ch63
Scope CH2(Red): Chip#0CH#0

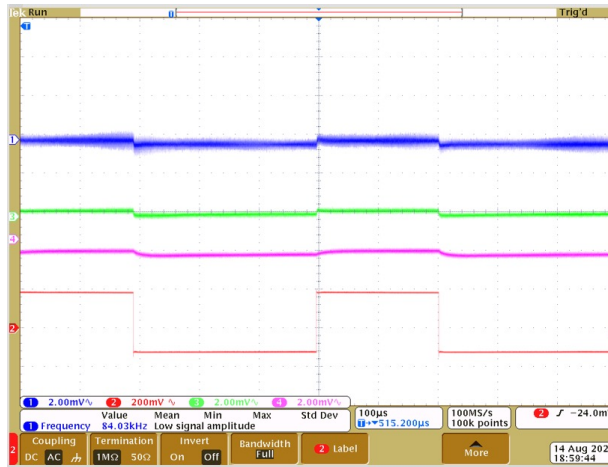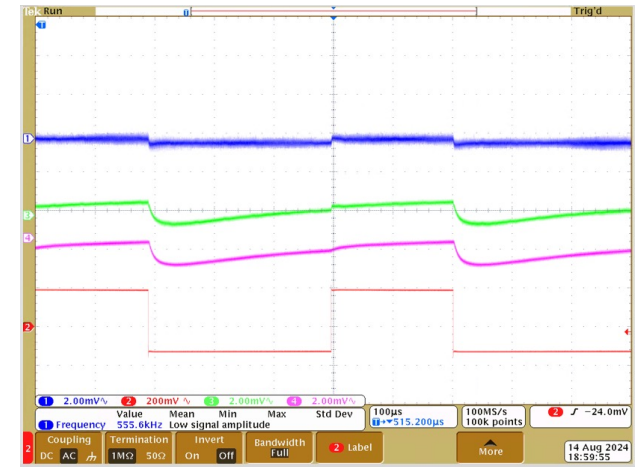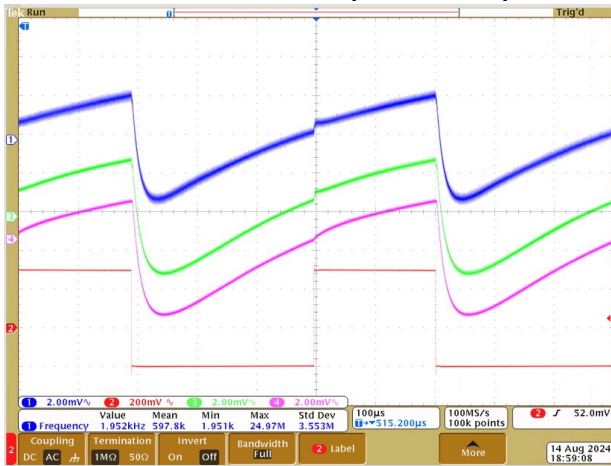200 mV BL

Sagging of 1.8V power rail is observed

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LN2: Chip#0CH#0 is selected for monitoring

- All channels are pulsed at 218 fC

VDDA&VDDP of CH64-CH127 tied together
VDDA&VDDP of CH0-CH63 tied together

Scope CH1(Blue): VDDA&VDDP for ch64-ch127
Scope CH3(Green): VDDP for ch0-ch63
Scope CH4(Pink): VDDA for ch0-ch63
Scope CH2(Red): Chip#0CH#0
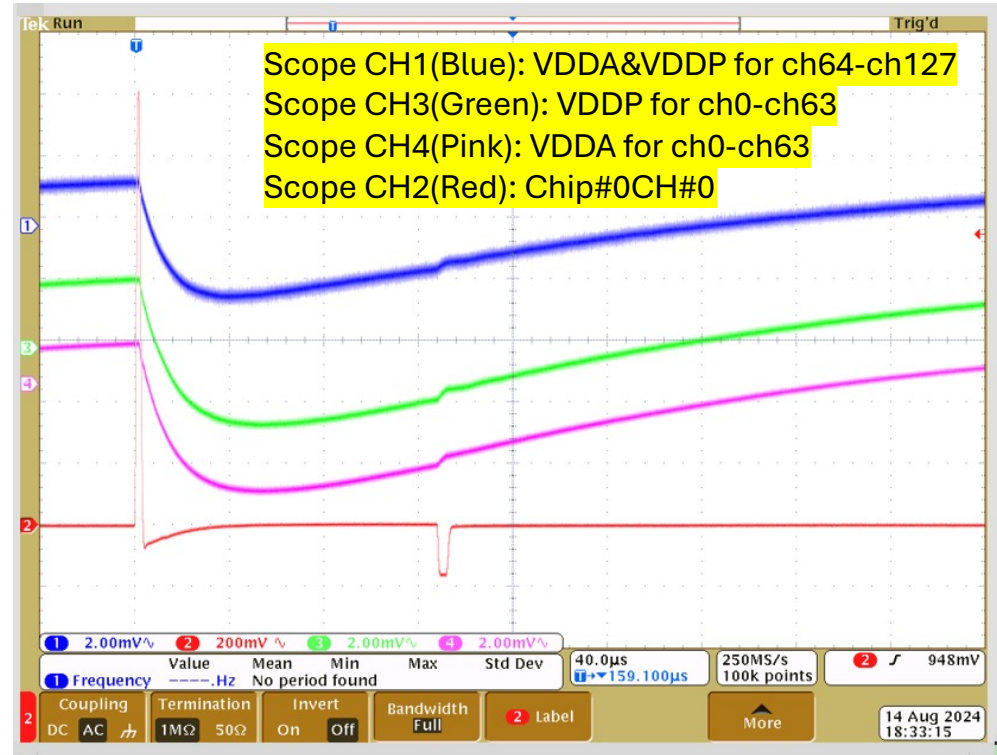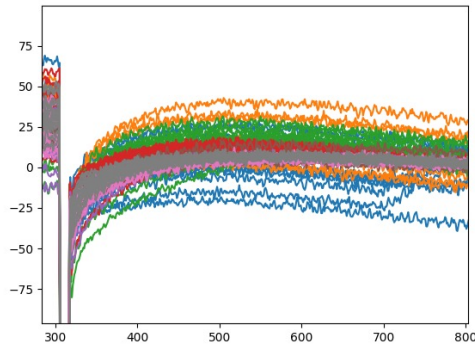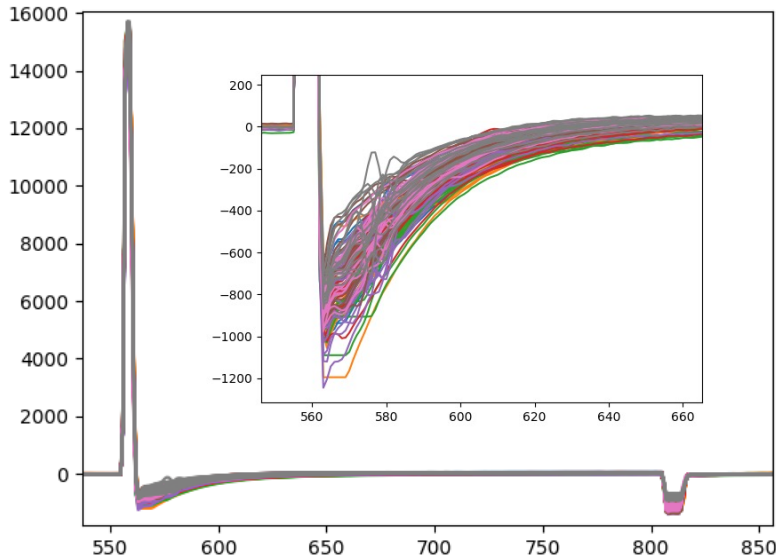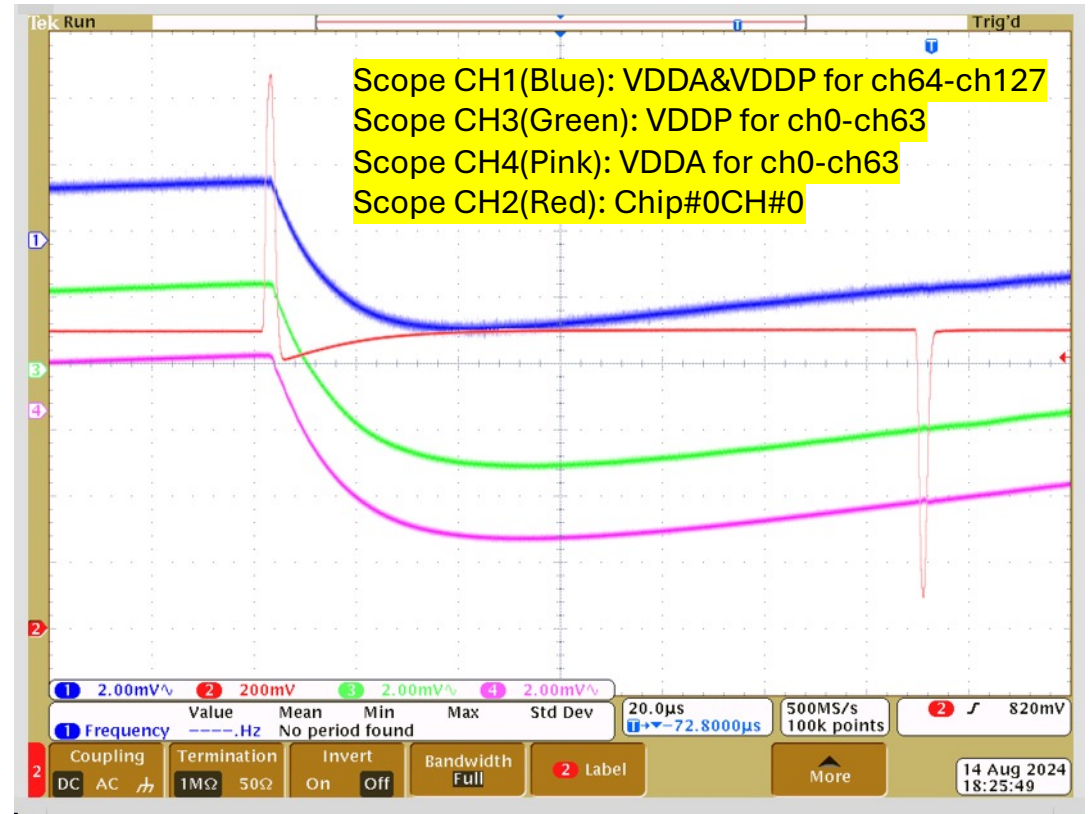
Sagging of 1.8V power rail is observed

900 mV BL

LN2: External pulser from signal generator

- All channels
  - Q = 185 fF * V
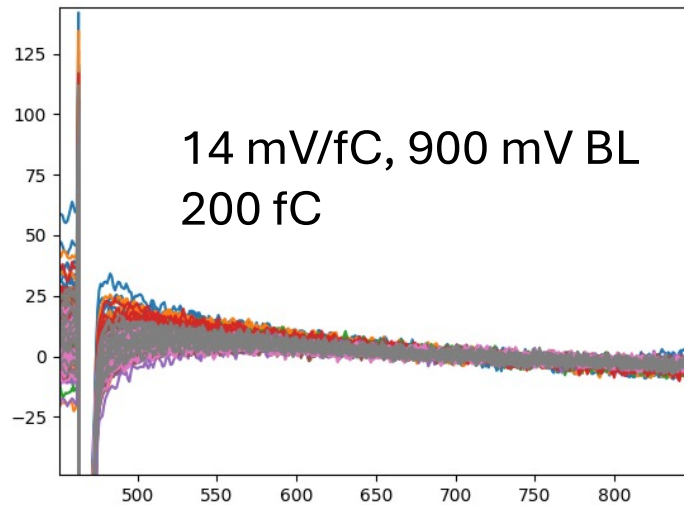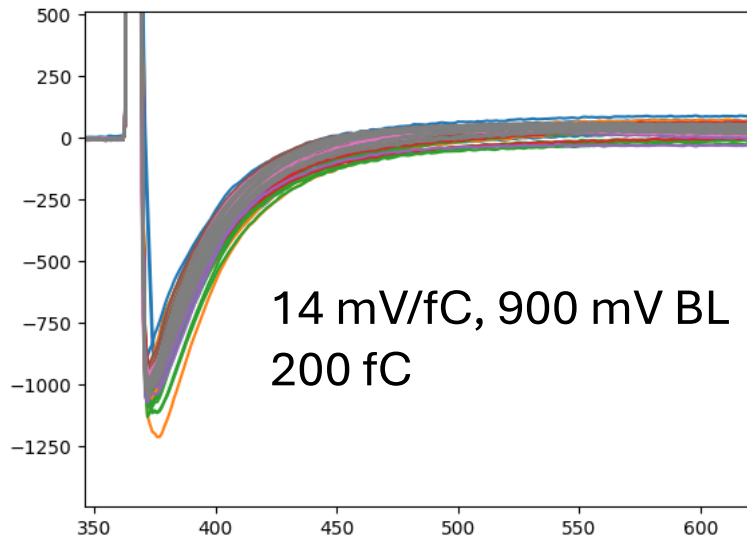
14 mV/fC, 900 mV BL
200 fC

14 mV/fC, 900 mV BL
200 fC

Scope CH1(Blue): VDDA&VDDP for ch64-ch127
Scope CH3(Green): VDDP for ch0-ch63
Scope CH4(Pink): VDDA for ch0-ch63
Scope CH2(Red): Calibration Pulser

V=1080mV

LN2: External pulser from signal generator
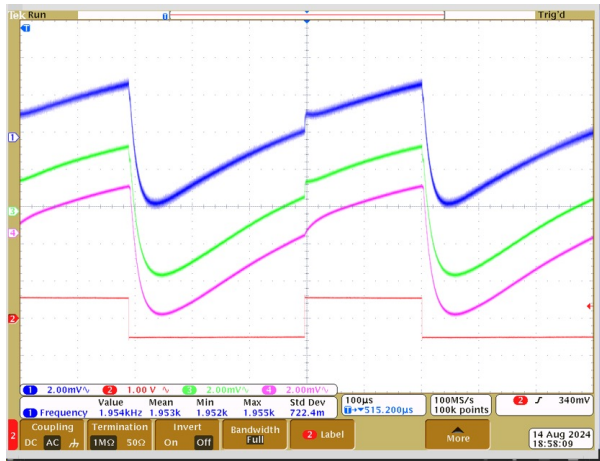
14mV/fC, 900mV BL

V=1080 mV (200 fC)

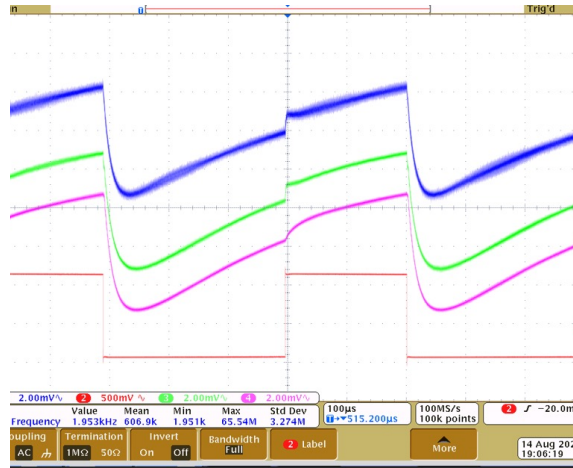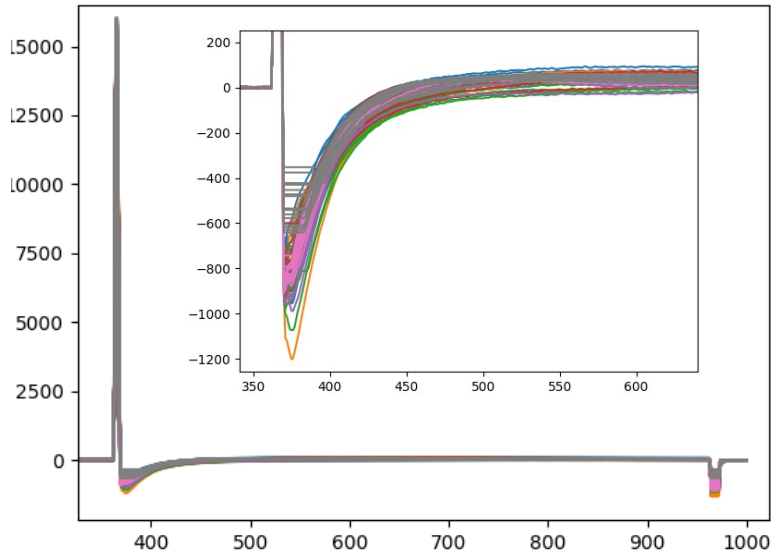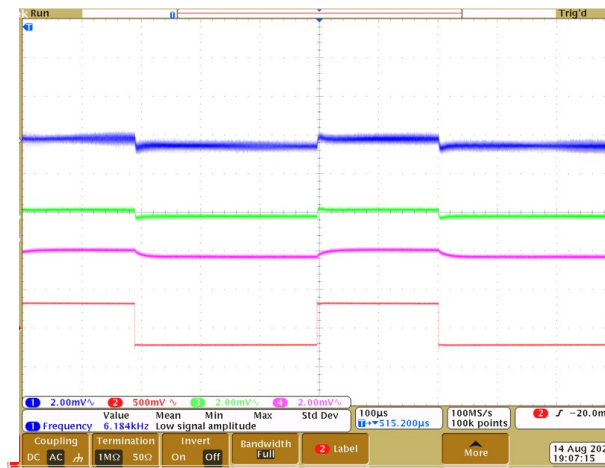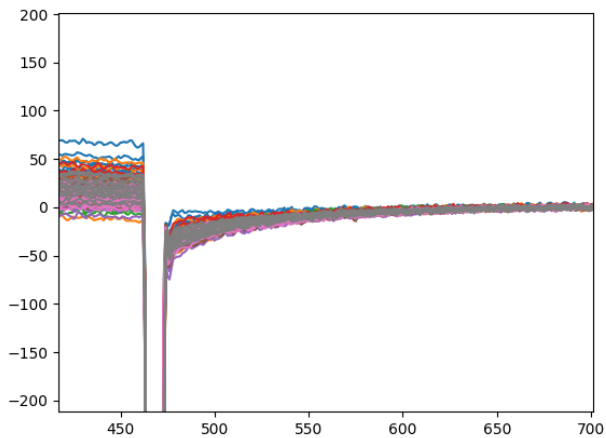V=310 mV (57 fC)

V=320mV (60 fC)

V=500 mV (93 fC)
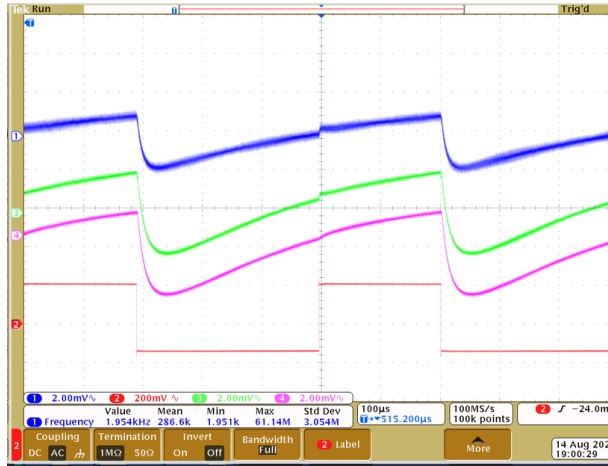
V=350 mV (65 fC)

V=300 mV (55 fC)
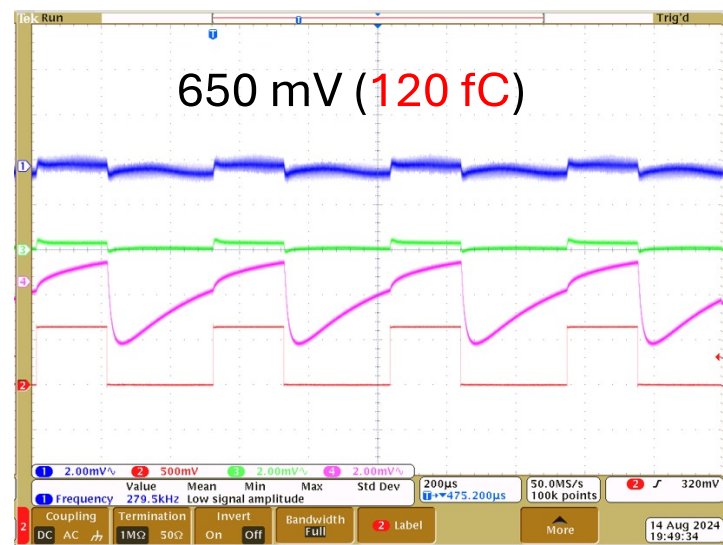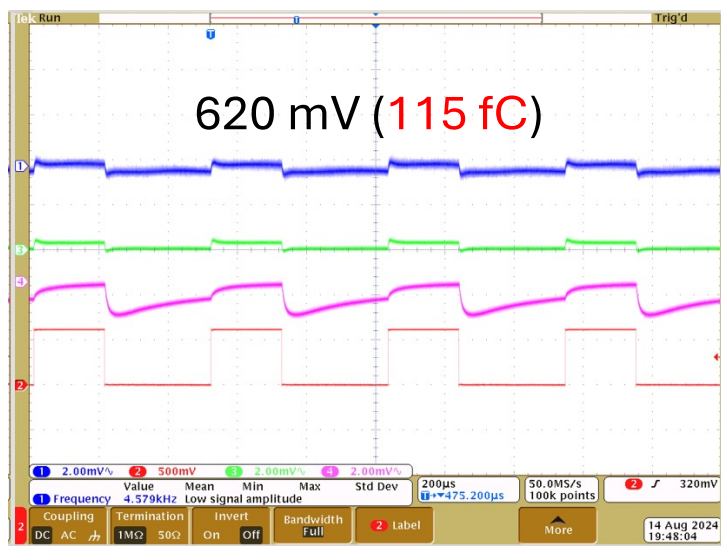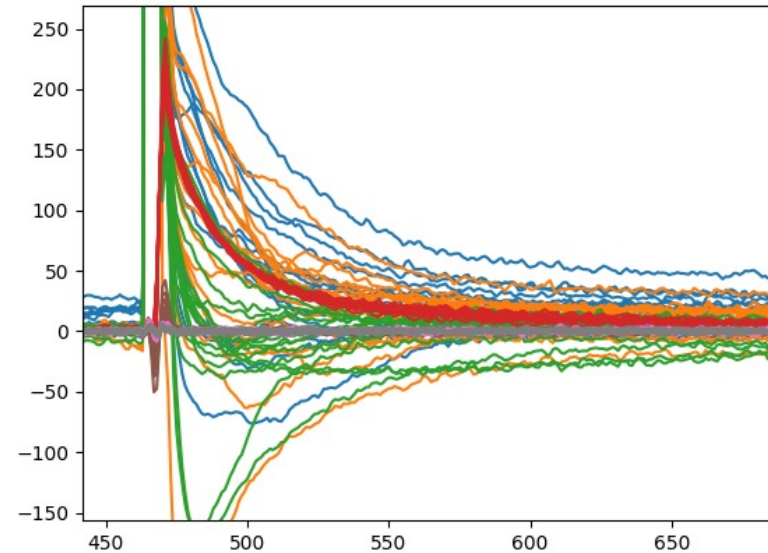
44
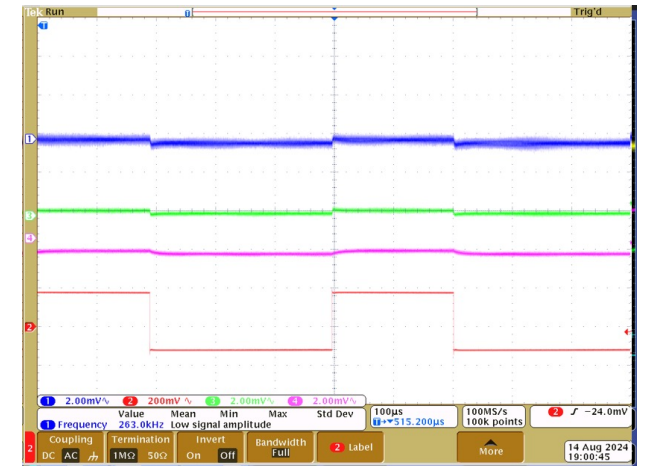
LN2: External pulser from signal generator
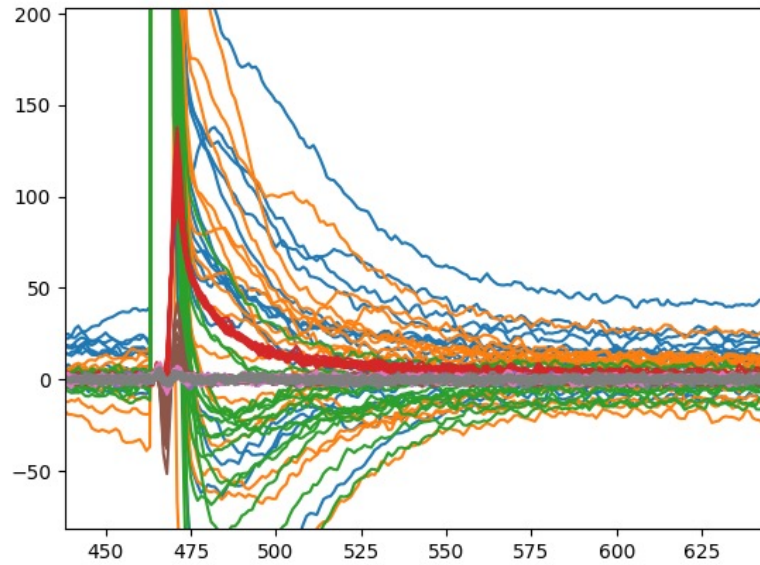
14mV/fC, 200mV BL
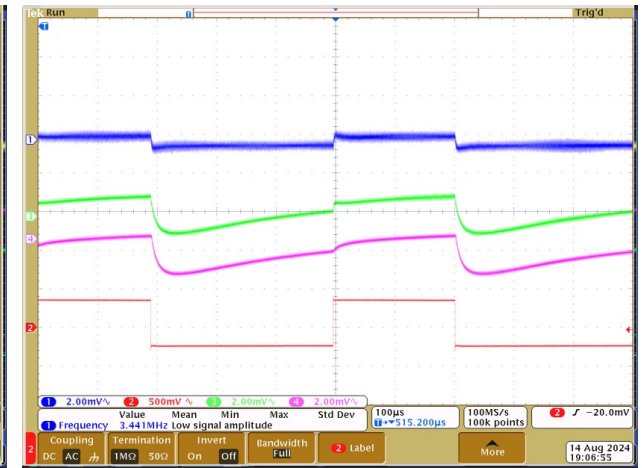
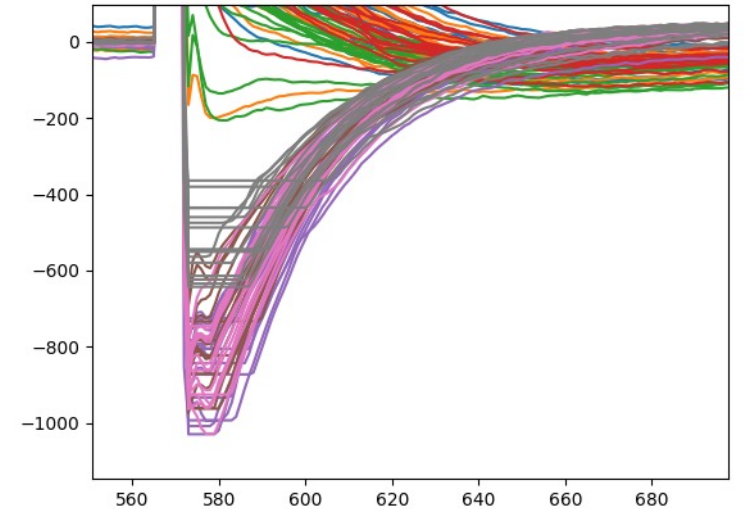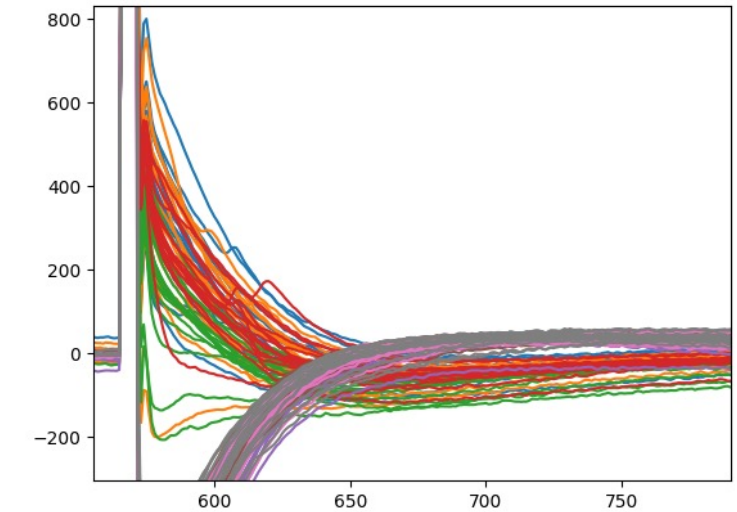V=1080 mV (200 fC)

V=600 mV (110 fC)

V=550 mV (102 fC)

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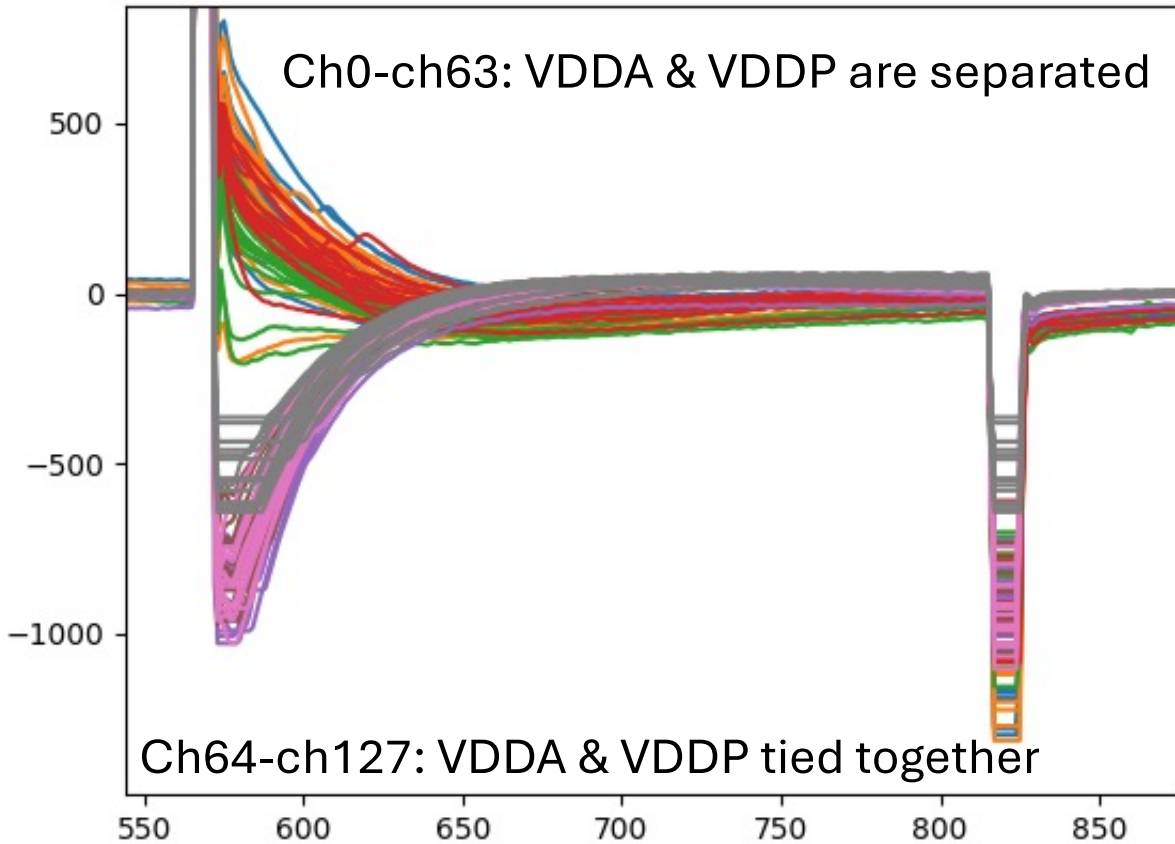# CH#0-63: VDDA & VDDP are separated

- Chip#0,1,2 (48 chns) are pulsed

620 mV (115 fC)

650 mV (120 fC)

CH#0-63: VDDA & VDDP are separated

- Internal calibration (218 fC) to all channels
  - Both VDDA&VDDP (CH#0-63) R to 0.1 Ohm

Ch0-ch63: VDDA & VDDP are separated
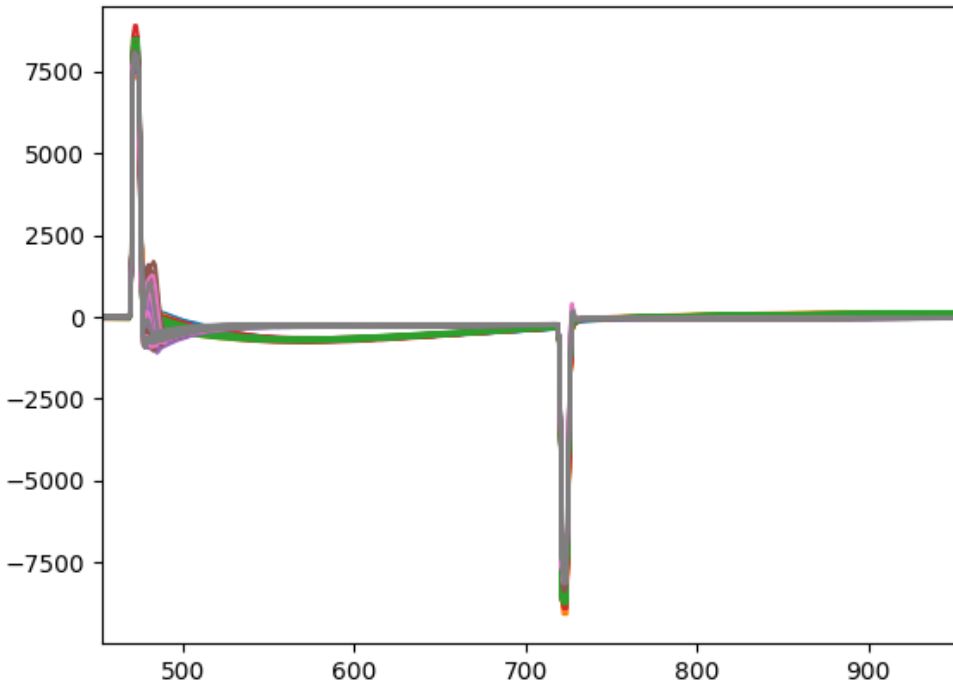
Ch64-ch127: VDDA & VDDP tied together

CH#0-63: VDDA & VDDP are separated

- Internal calibration (218 fC)

Chip#0,1,2 pulsed

Chip#0,2,3 pulsed

Chip#0,1,3 pulsed

Scope CH1(Blue): VDDA&VDDP for ch64-ch127
Scope CH3(Green): VDDP for ch0-ch63
Scope CH4(Pink): VDDA for ch0-ch63
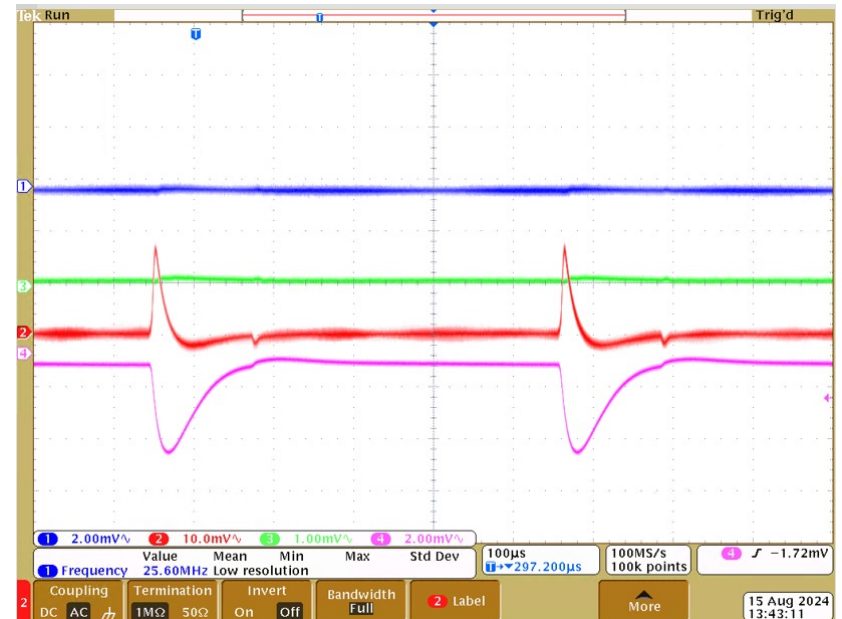Scope CH2(Red): CH#0
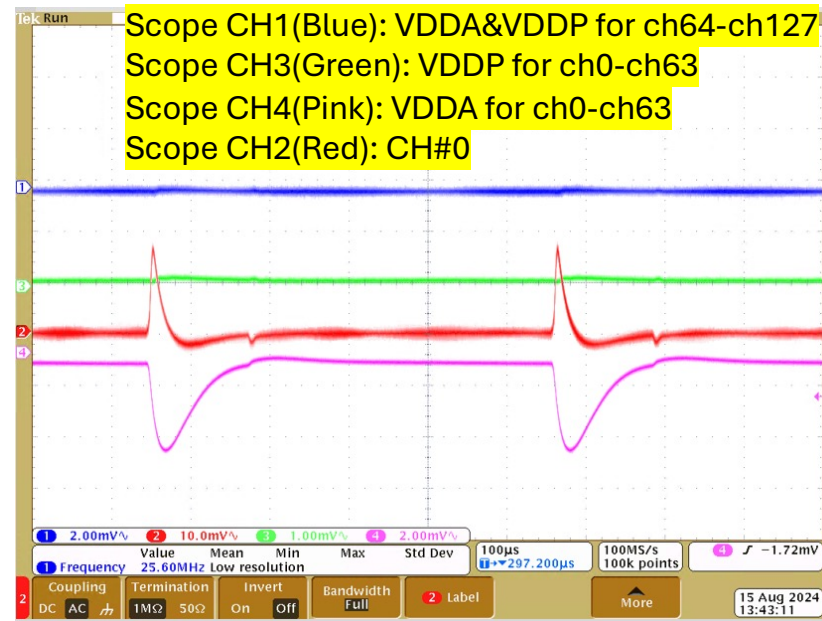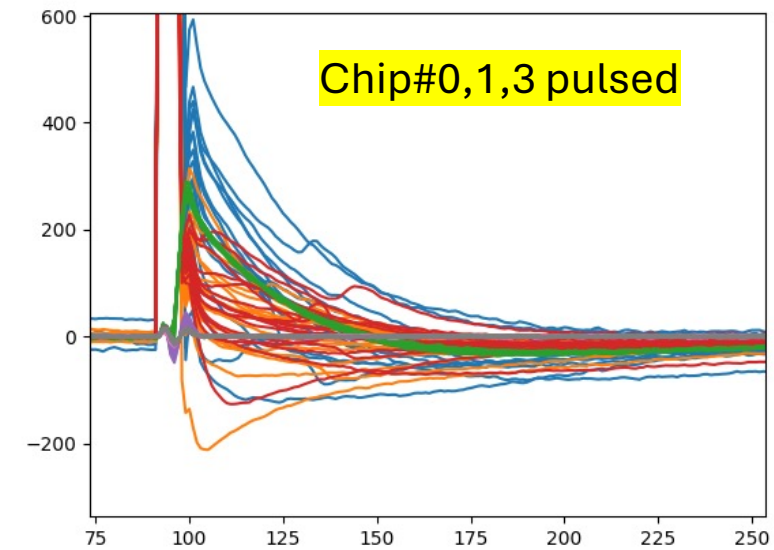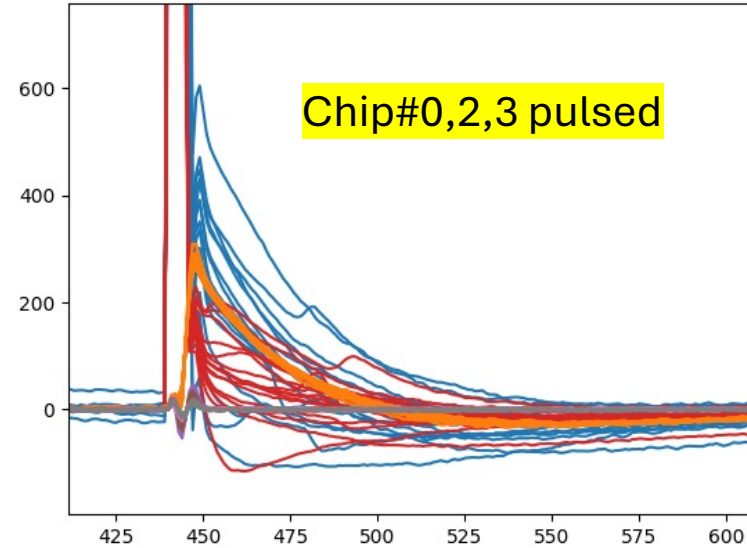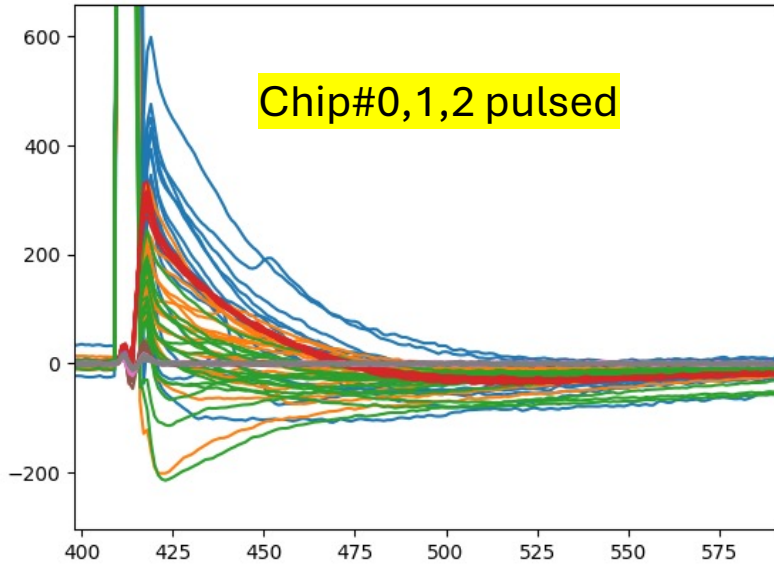
CH#0-63: VDDA & VDDP are separated
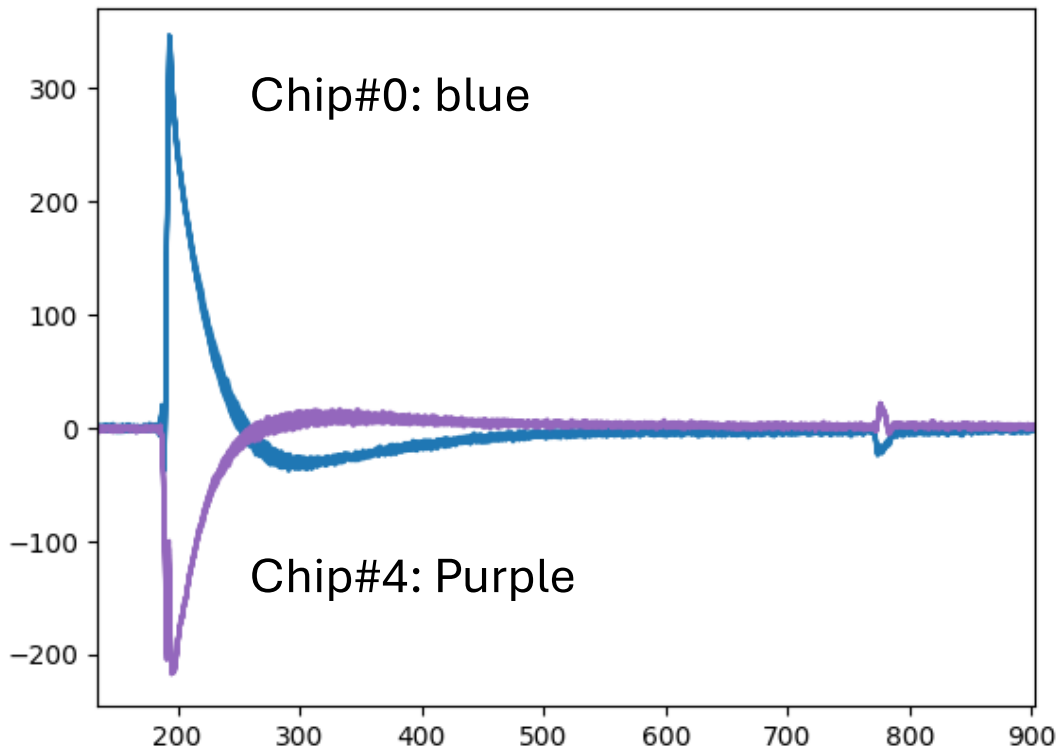
- Internal calibration (218 fC) for all channels
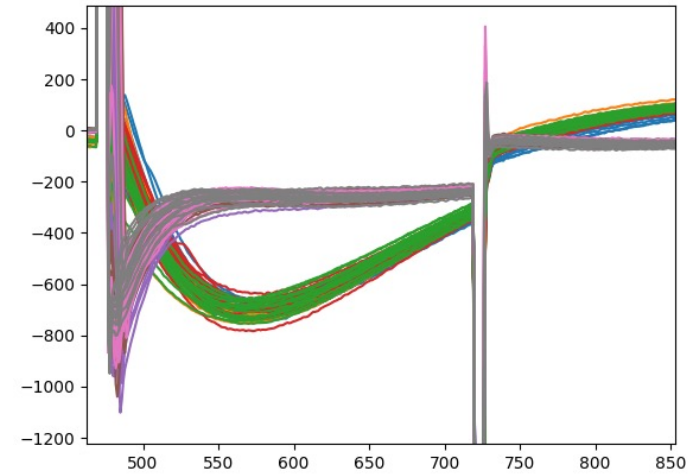
AC coupling mode has no impact

External Pulser from Signal Generator
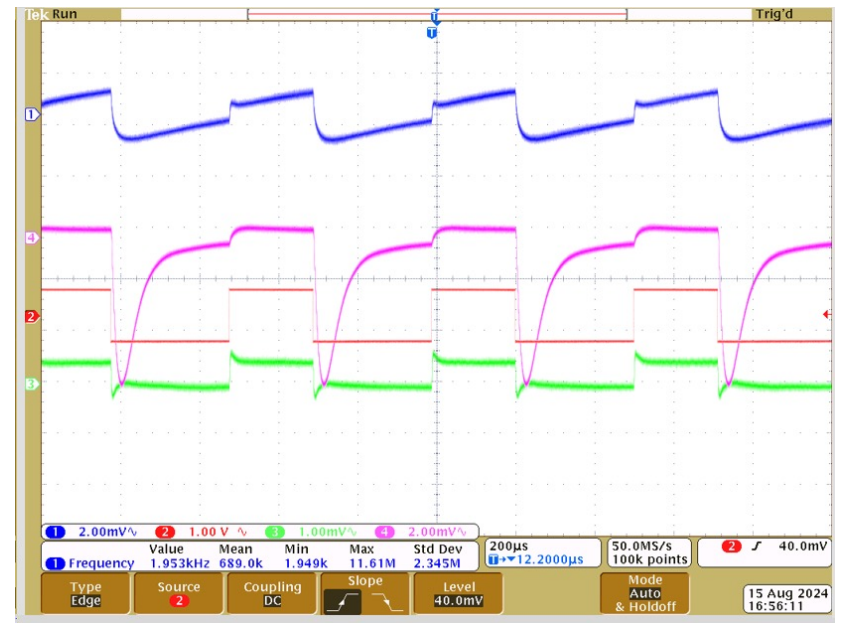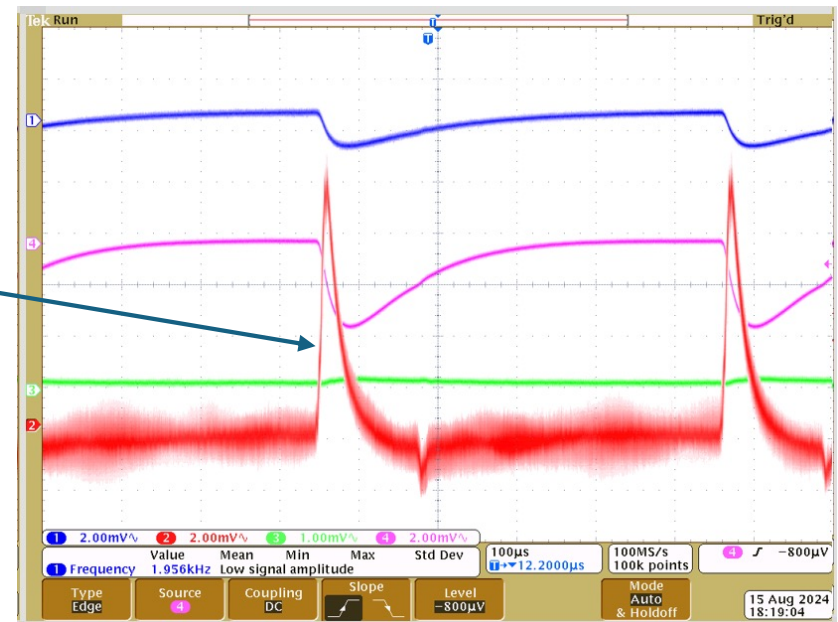
- Chip#1,2,3,5,6,7 are pulsed at 185 fC

Chip#0: blue

Chip#4: Purple
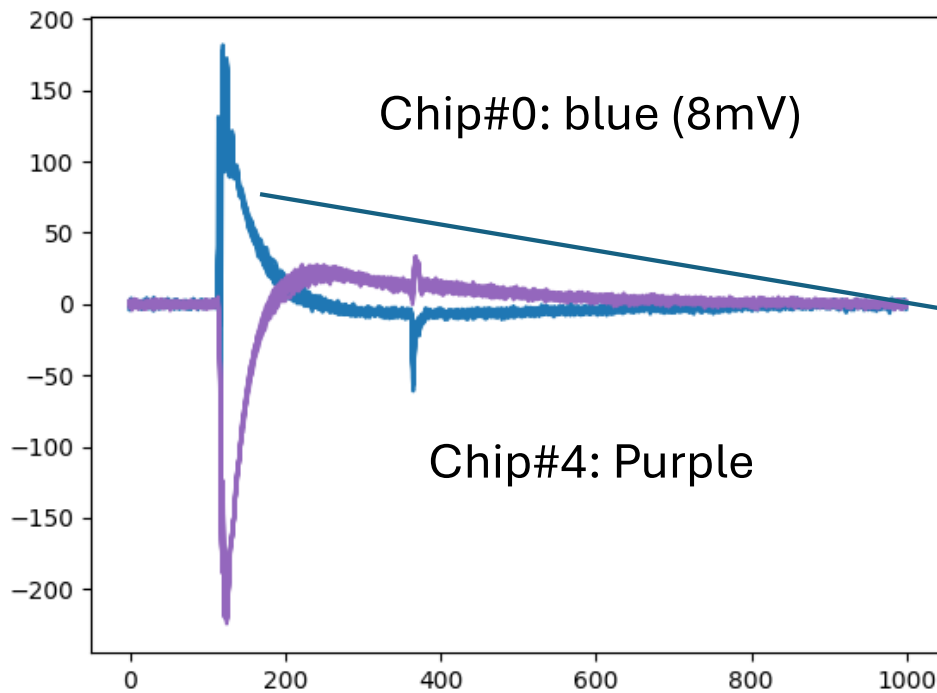
VDDA for chip#0-3: 0.1 Ohm, 1x C
VDDP for chip#0-3: 0.1 Ohm, 3x C
VDDA/VDDP (tied together) for chip#4-7: 1 Ohm, 3x C

Scope CH1(Blue): VDDA&VDDP for ch64-ch127
Scope CH3(Green): VDDP for ch0-ch63
Scope CH4(Pink): VDDA for ch0-ch63
Scope CH2(Red): CH#0

Internal calibration (SE)

- ## Chip#1,2,3,5,6,7 are pulsed at 218 fC
  - ### Chip#0CH#0 is used for analog monitoring
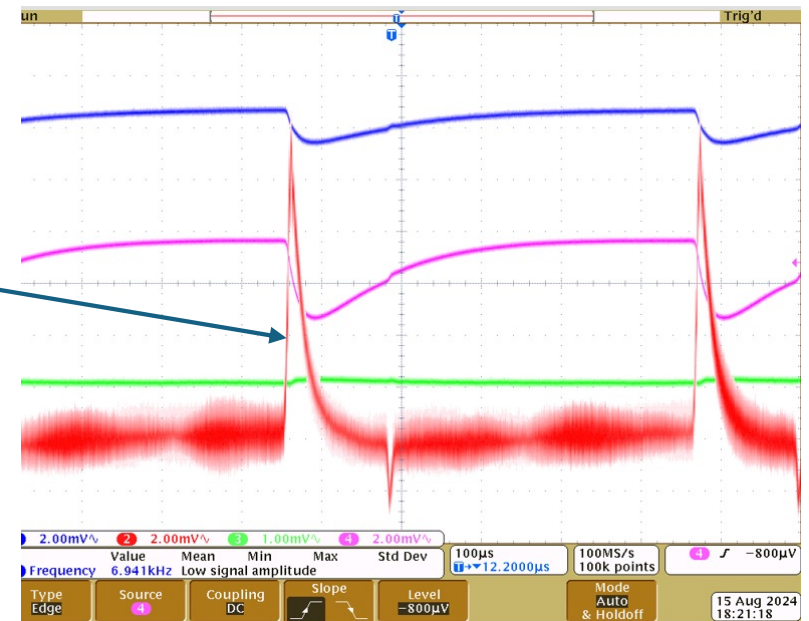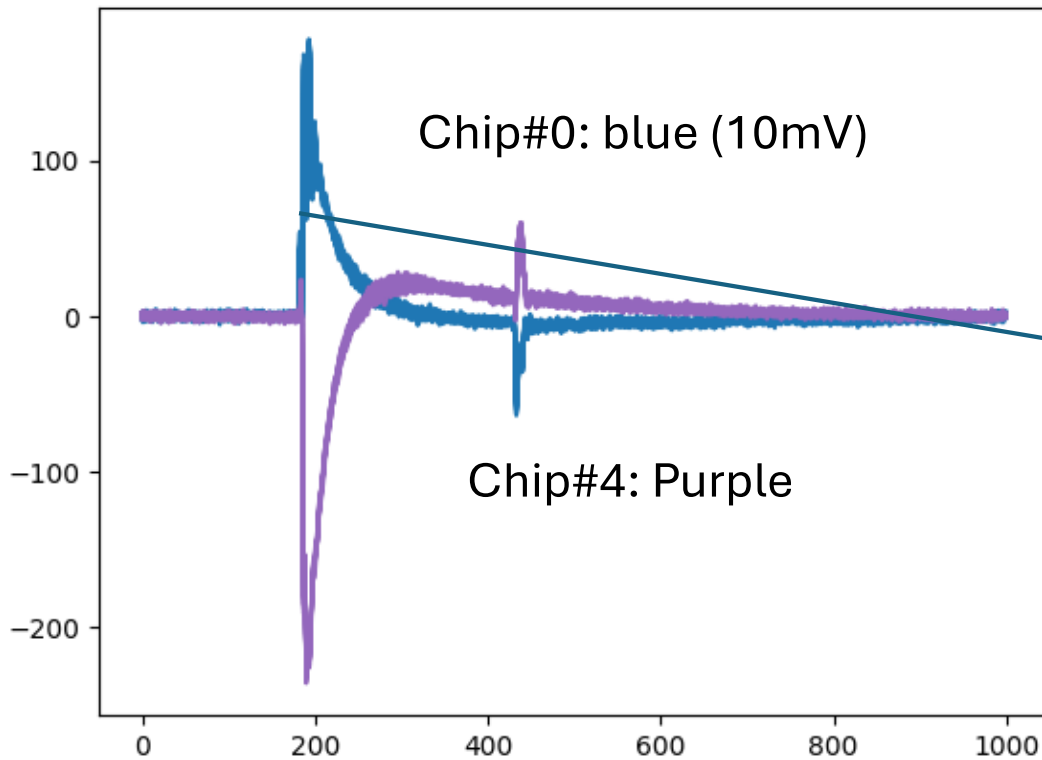

Scope CH1(Blue): VDDA&VDDP for ch64-ch127
Scope CH3(Green): VDDP for ch0-ch63
Scope CH4(Pink): VDDA for ch0-ch63
Scope CH2(Red): CH#0

Internal calibration (DIFF)

- Chip#1,2,3,5,6,7 are pulsed at 218 fC
  - Chip#0CH#0 is used for analog monitoring

Chip#0: blue (10mV)

Chip#4: Purple

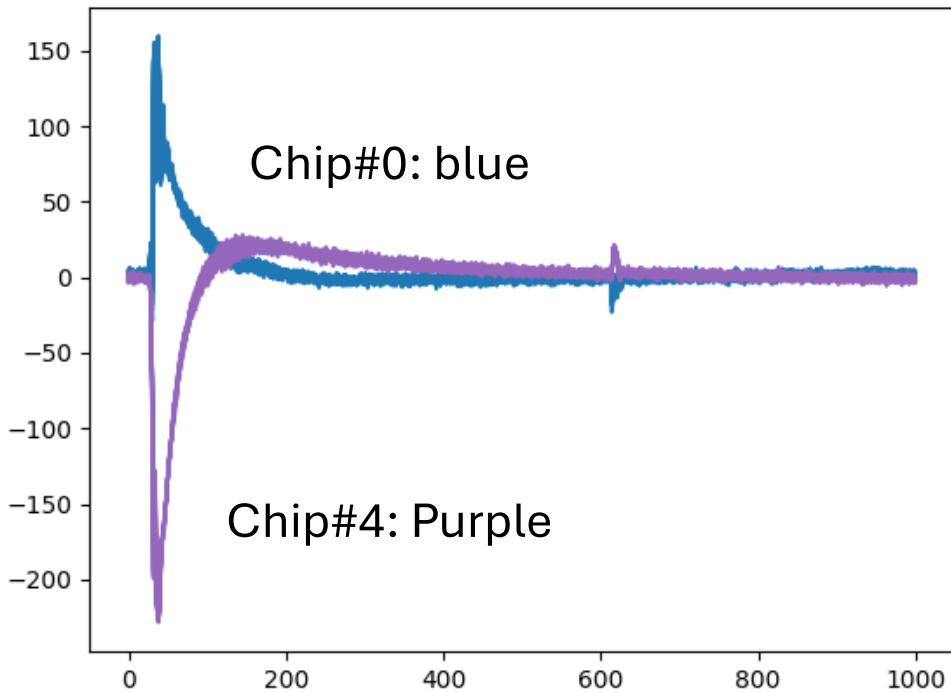Scope CH1(Blue): VDDA&VDDP for ch64-ch127
Scope CH3(Green): VDDP for ch0-ch63
Scope CH4(Pink): VDDA for ch0-ch63
Scope CH2(Red): CH#0

External Pulser from Signal Generator
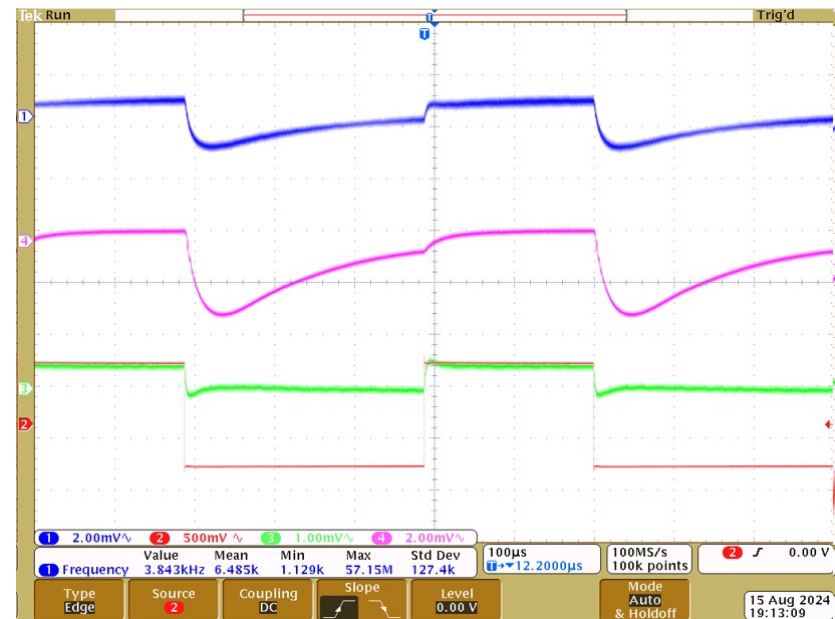
- Chip#1,2,3,5,6,7 are pulsed at 185 fC

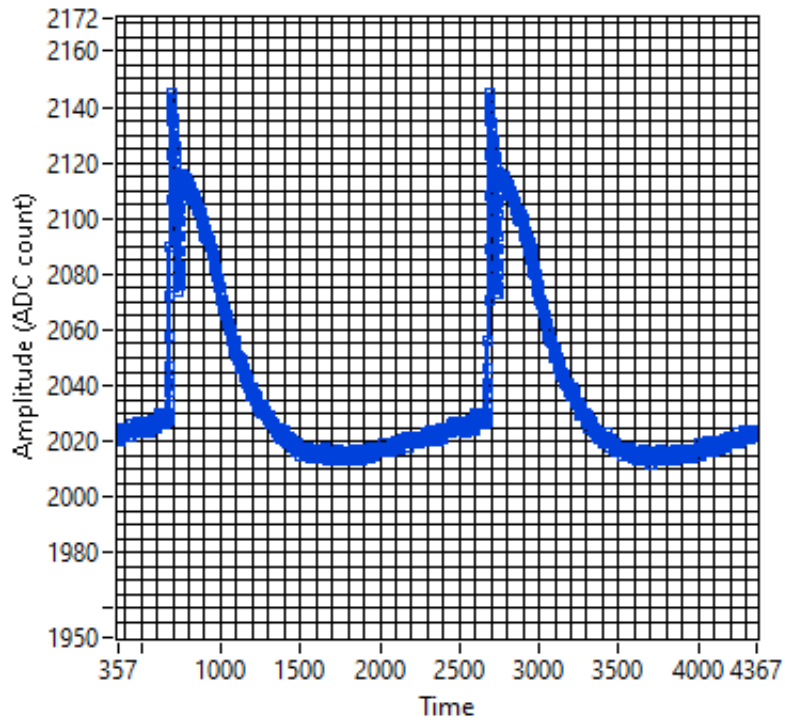VDDA for chip#0-3: 0.1 Ohm, 2x C
VDDP for chip#0-3: 0.1 Ohm, 1x C
VDDO disconnected from VDDA
re-connected to VDDP for chip#0-3
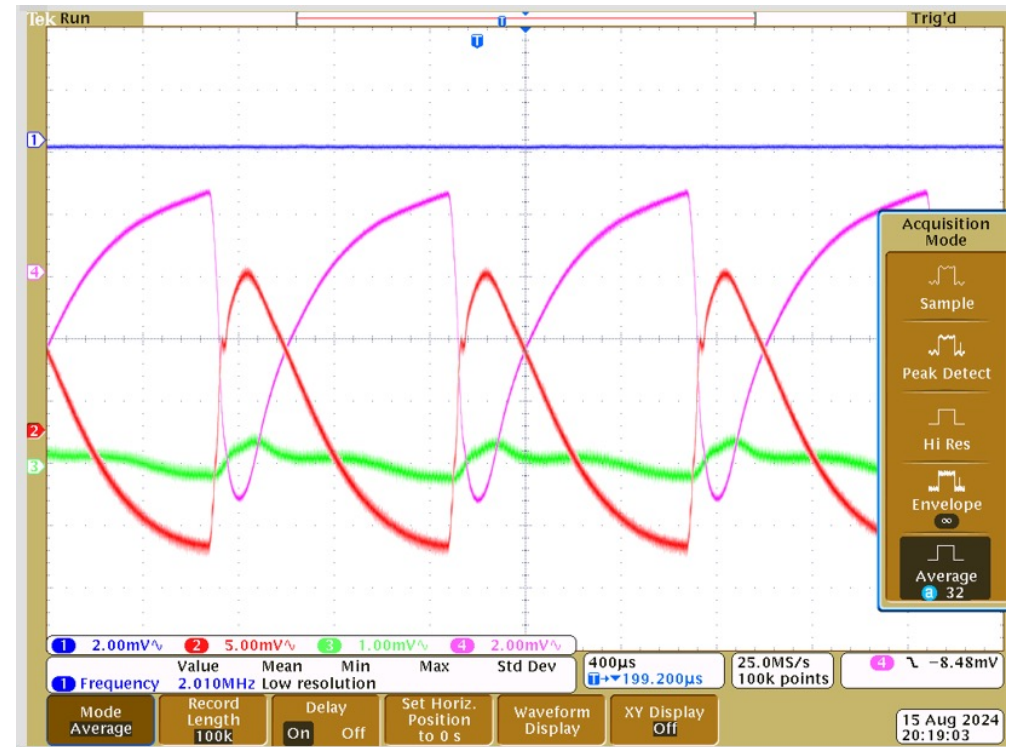
VDDA/VDDP (tie together) for chip#4-7: 0.1 Ohm, 3x C

SBND FEMB (LN2)

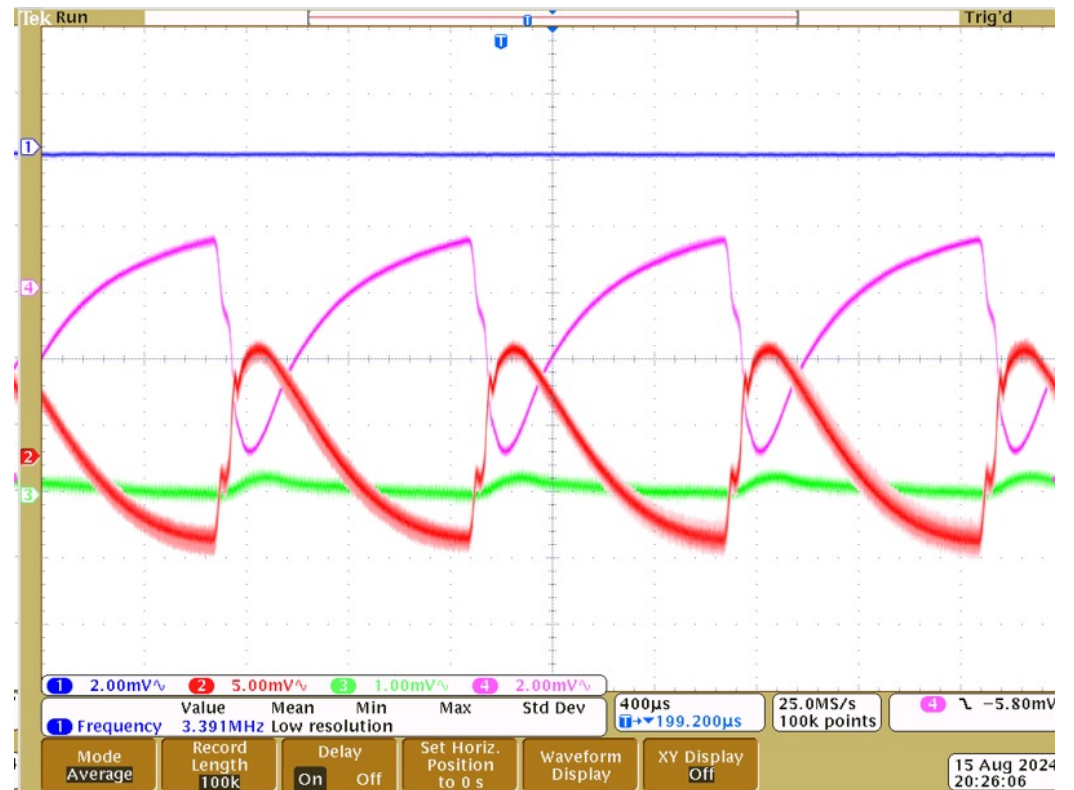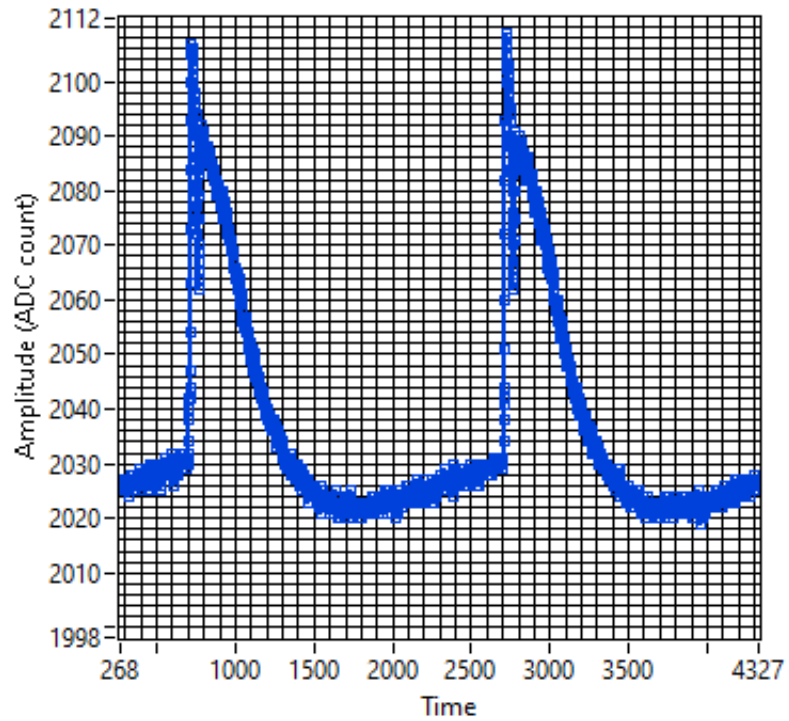- VDDP and VDDA are separated

- 3 chips are pulsed (dac = 0x3f)

SBND FEMB (LN2)

- 2 chips are pulsed (dac = 0x3f)

SBND SBND FEMB (LN2)

- 1 chip is pulsed (dac = 0x3f)