DUNE-VD PDS
Cold electronics for the cathode modules

Sept. 17th, 2024

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Motivations of the study and topics of presentation at PhSensor Mtg

Bench Tests performed at FNAL/IERCC-ColdLab in LAr and at MTS at CERN/NP in LAr

- Signal and Noise dependence from V_{bias} on SiPM (HPK) and from CE-DCEM Gain (R_{fb}) parameters: search for optimal configurations within range of requirement values
- Motivations for SiPM HPK V_{bias}^{VD} adopted so far in the VD (FD2) r/o electronic development
- Study performed shows opportunities for R_{fb} & V_{bias} combinations - w/ lower V_{bias} that preserve high SNR and large DR.
- DCDC V_{out} (in LAr) available in the range of identified V_{bias}
- Propose longevity tests (at BNL) at few different V_{bias} specific values and compare with reference HPK V_{bias}^{HD} for potential long-term degradation.

SiPMs readout performance study

Two key parameters:

Signal Noise Ratio and **Dynamic Range**

SPE signal is proportional to both SiPM bias and CE gain.
Noise is not.

Varying one or the other is not equivalent in terms of SNR.

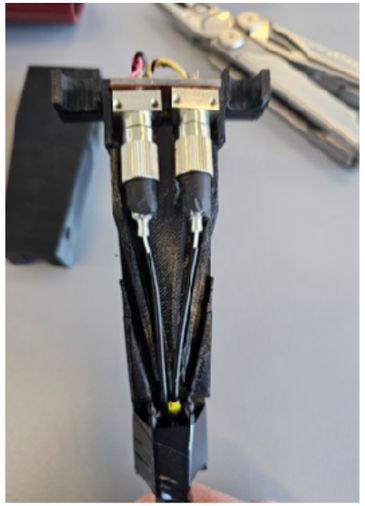
Dynamic range, which depends on CE saturation, is proportional to 1/SPE amplitude

➡ Dynamic range ~ 1/bias and 1/gain.

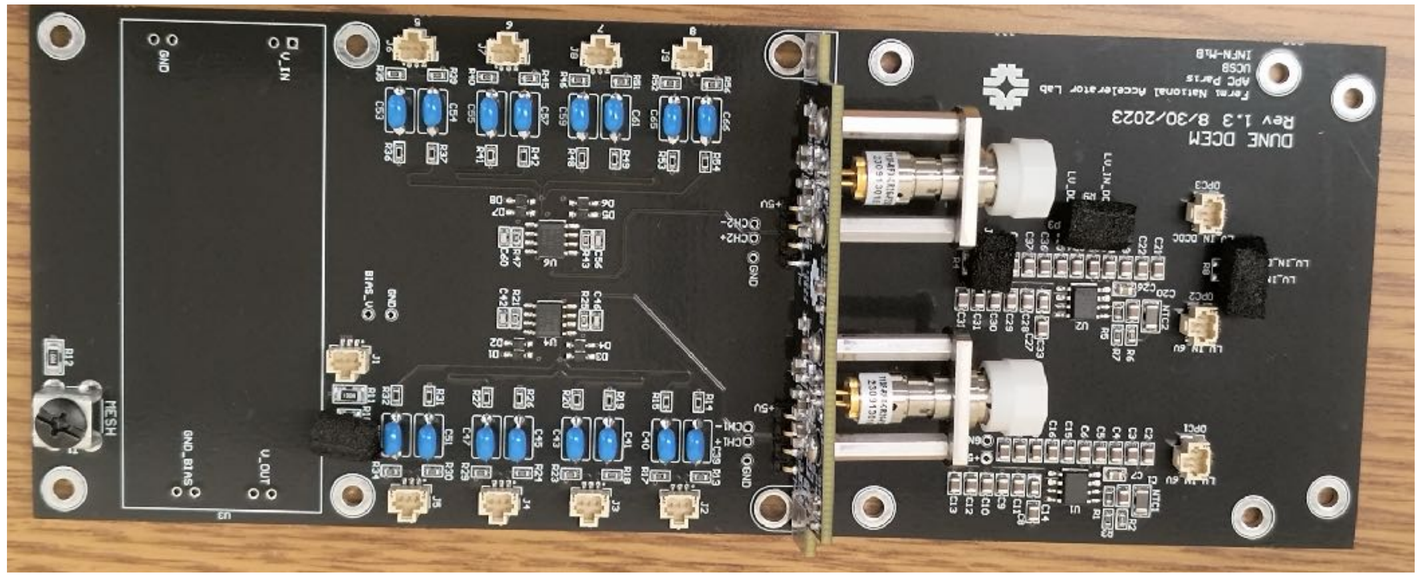
Cathode CE: DCEM 1.31

DCDC w/ and w/o shielding

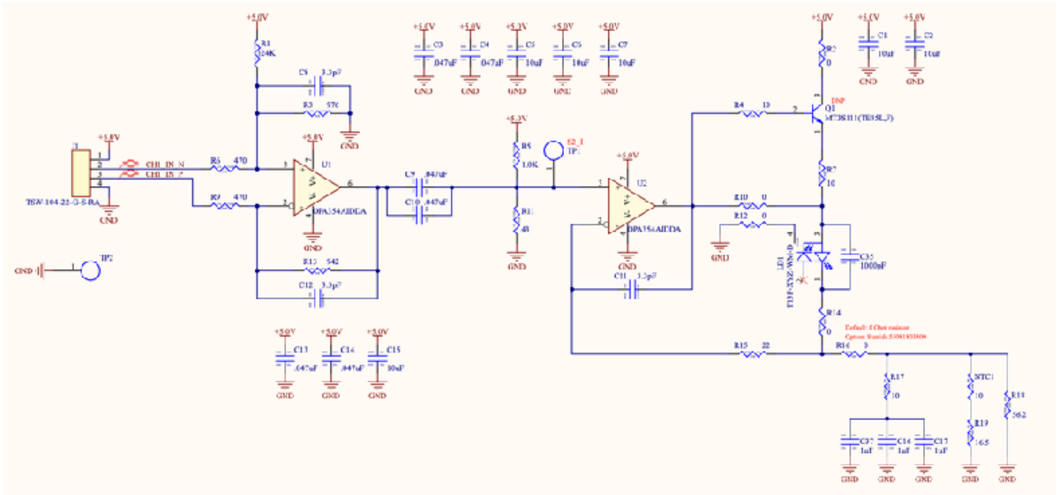
OPC + fibers



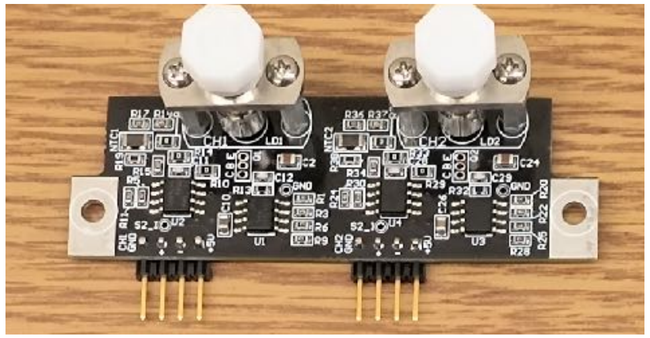
Motherboard:



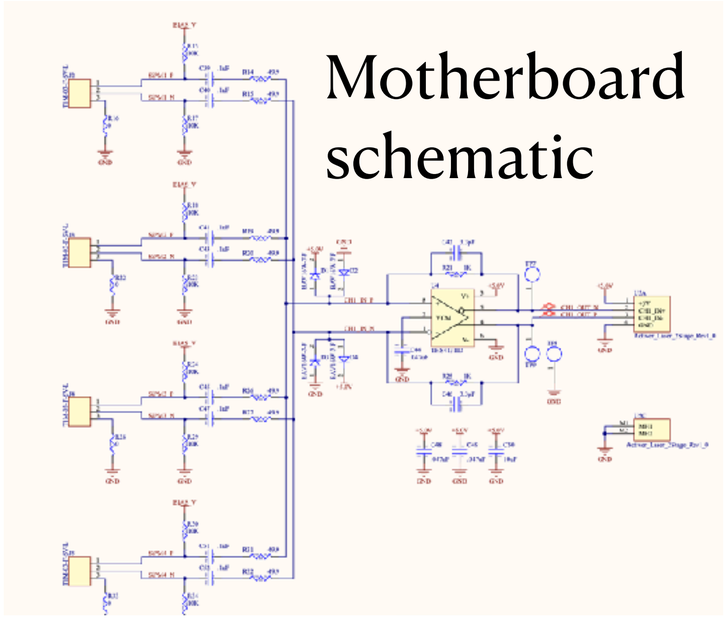
Laser daughter card schematic



Laser daughter card



Motherboard schematic



Scan in Bias Voltage and CE Gain (1st stage)

Test setup

DCEM1.3 CMOS
4 HPK flexes
Koheron+scope r/o
Bias over copper
No-DCDC

DCEM and SiPM in LAr

Gain ∝ R_{FB}

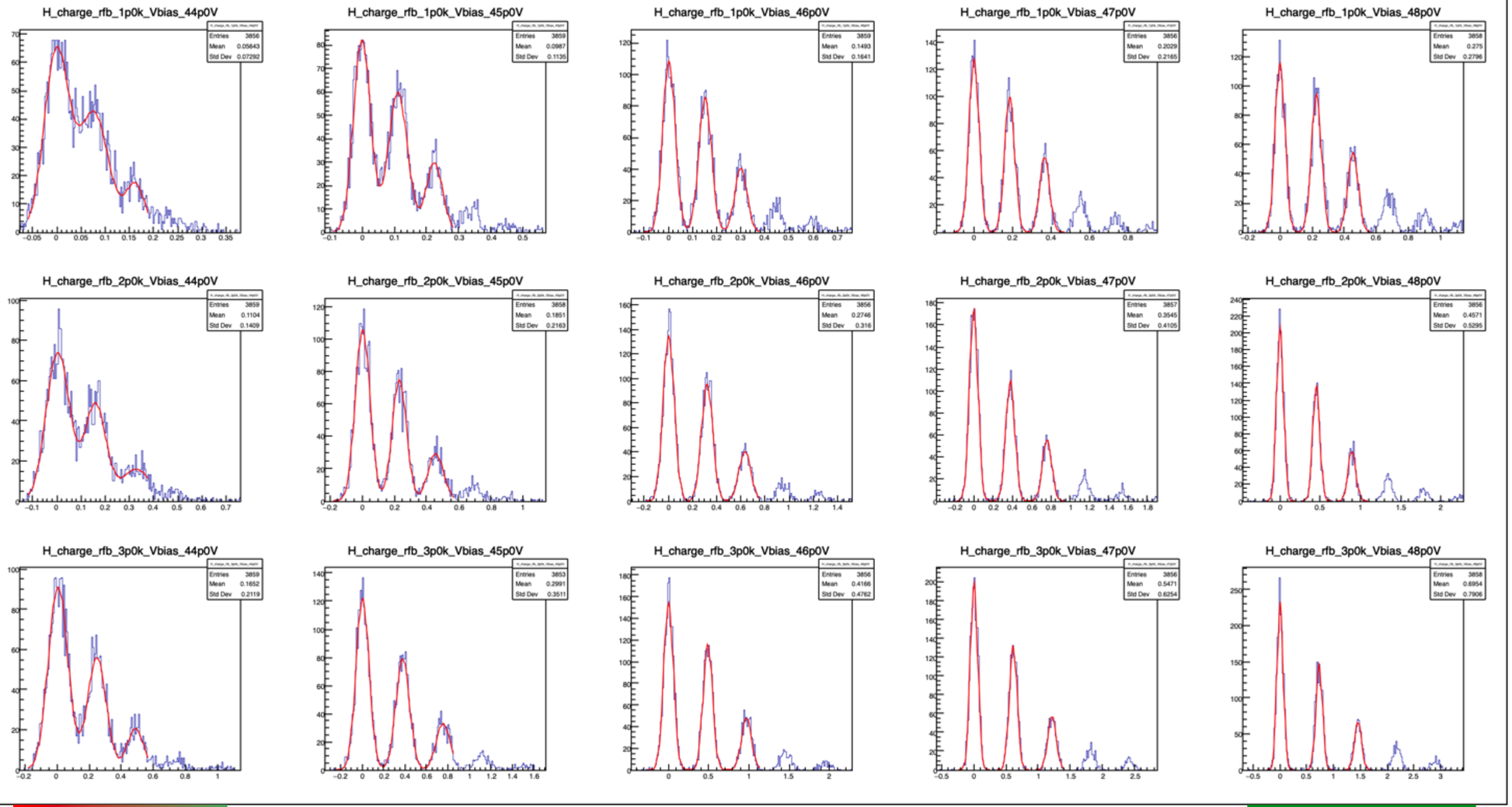
3x feedback resistor values:
1kΩ, 2kΩ, 3kΩ

5x bias voltage values:
44V, 45V, 46V, 47V, 48V

Tests with other configs. (CMOS, BiPol OpAmp) and also with FBK gives similar behavior.

Low G - Low V_{bias}

Low G - High V_{bias}



High G - Low V_{bias}

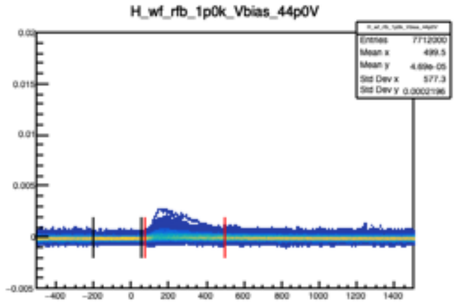
High G - HighV_{bias}

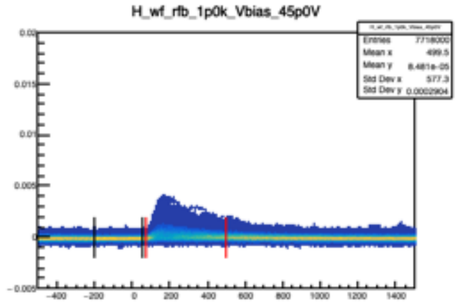
For SNR optimization **Low G - High V_{bias}** is preferred

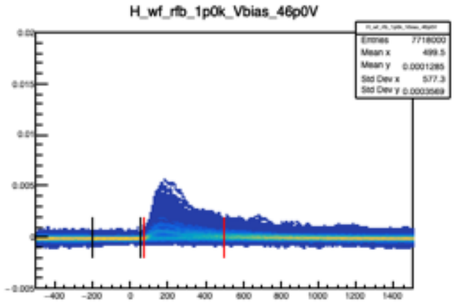
Scan in Bias Voltage and CE gain (1st stage)

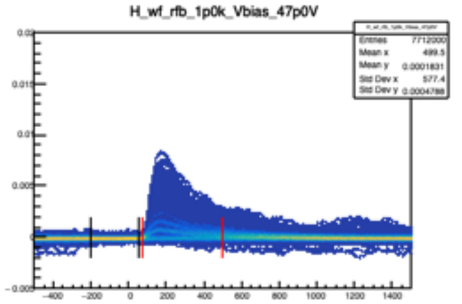
Low G - Low V_{bias}

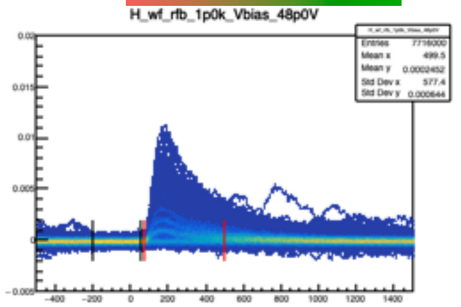
Low G - High V_{bias}

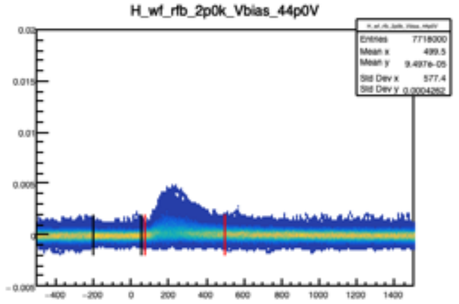


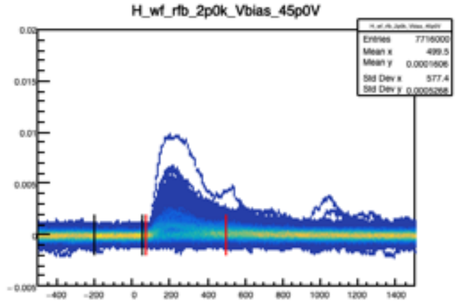


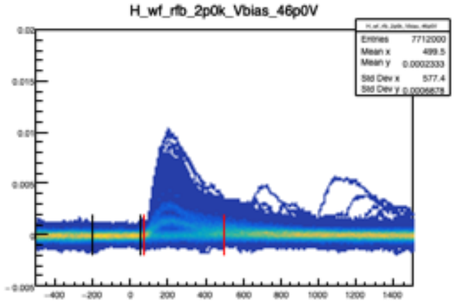


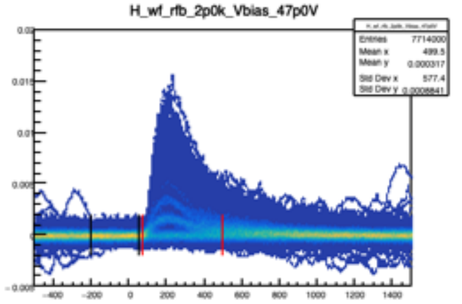


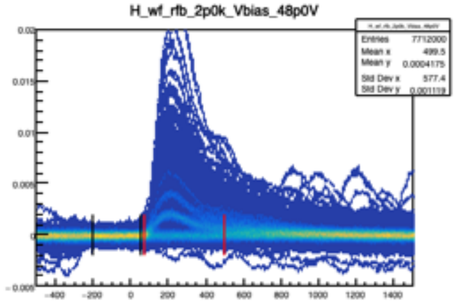


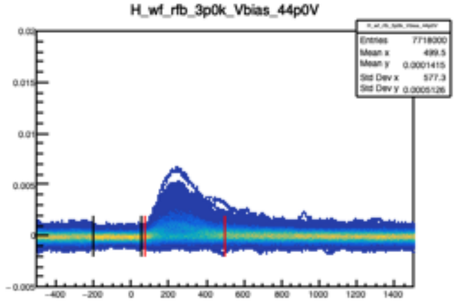


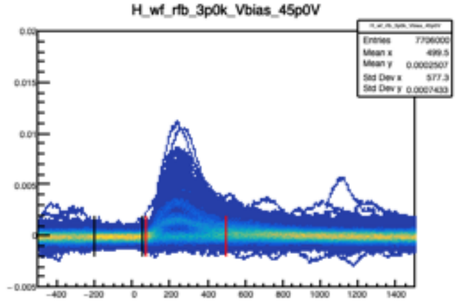


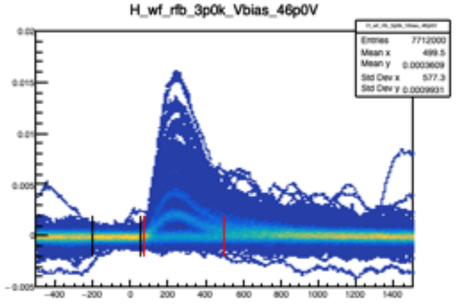


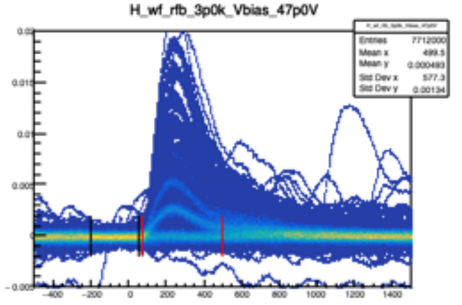


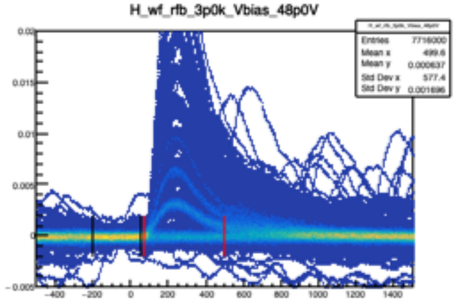












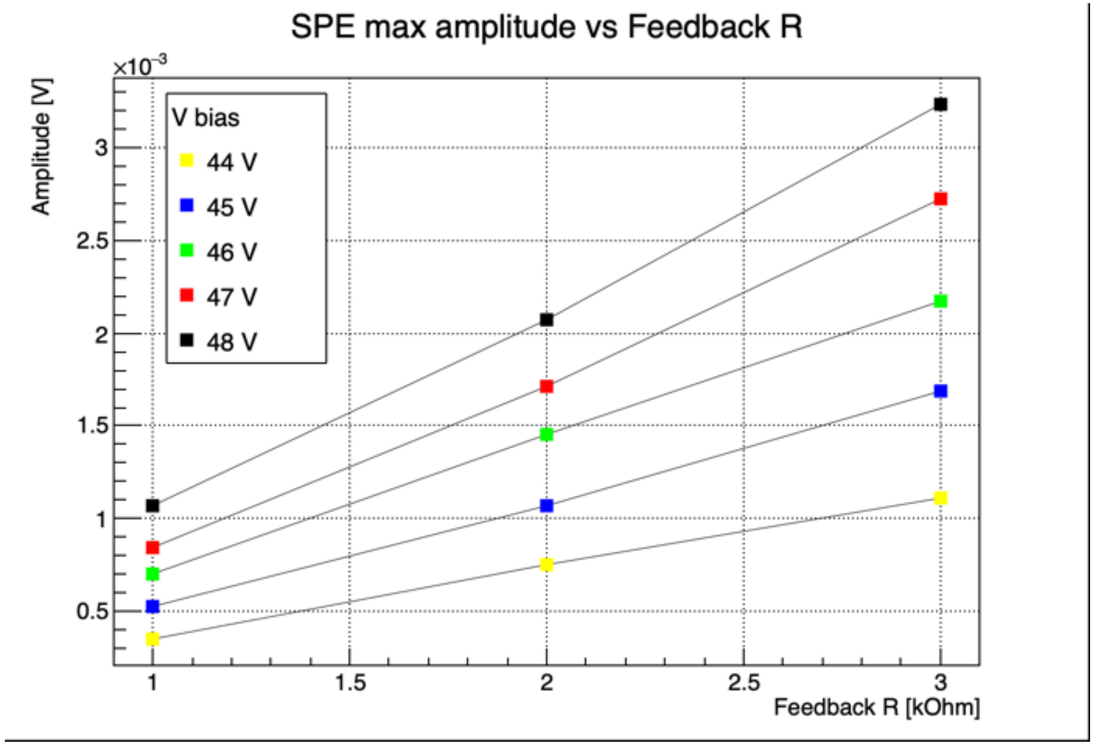
High G - Low V_{bias}

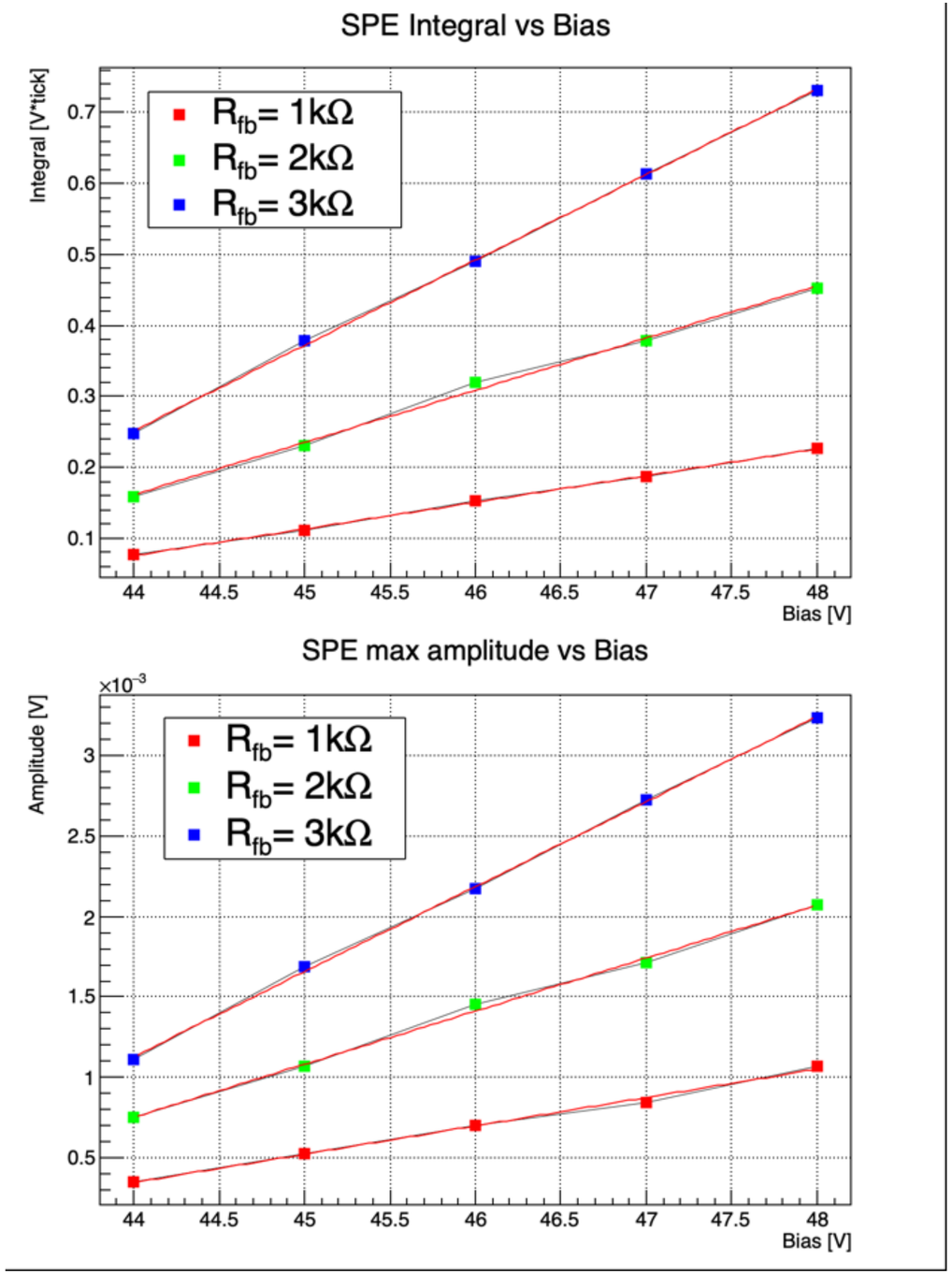
High G - HighV_{bias}

Raw data (no filtering), black window = baseline (simple average), red window = integration

SPE Signal: integral and amplitude

Both SPE integral and amplitude increase linearly with the feedback resistor values and with the over voltage values (V_{bias})

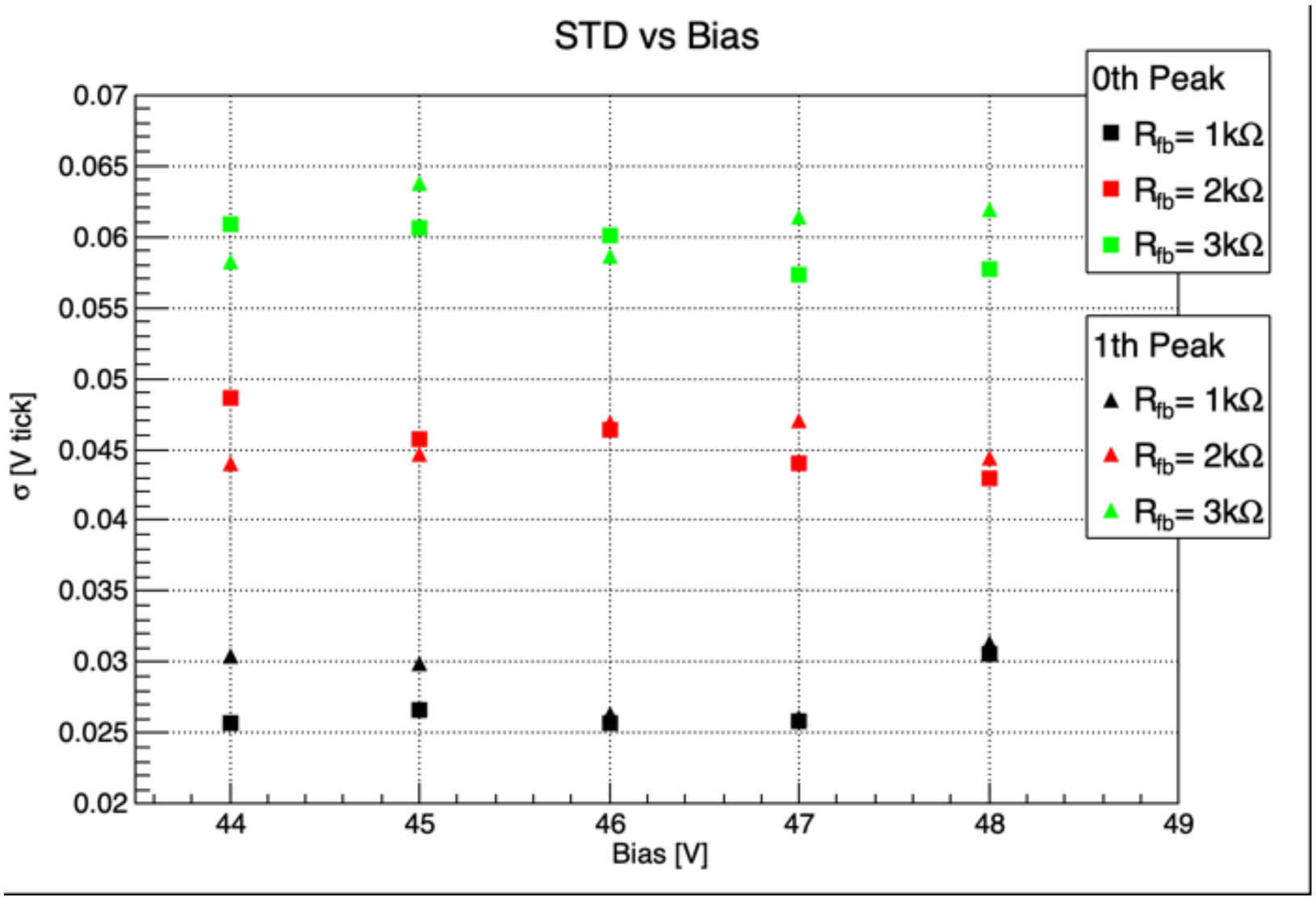




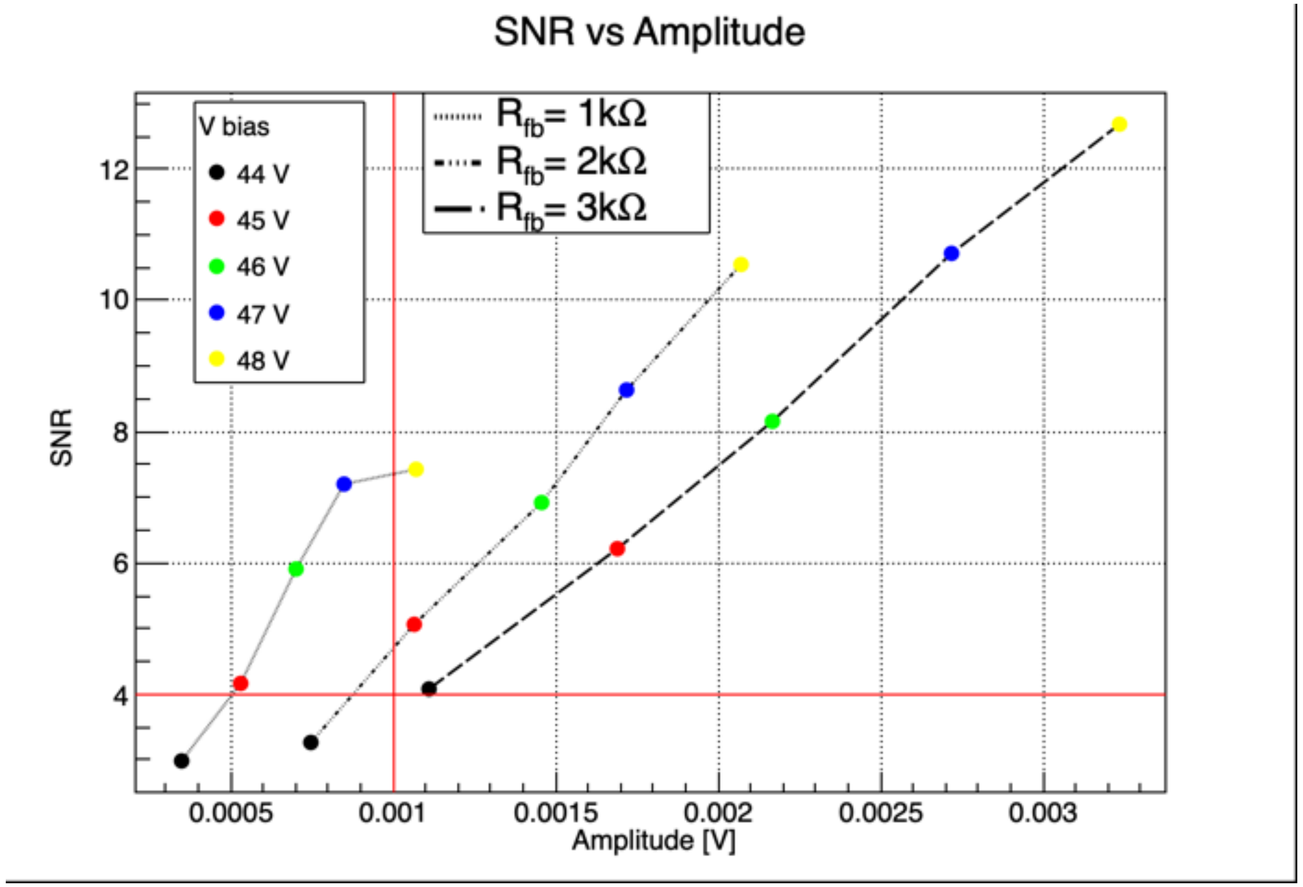
Noise

The STD of the 0th (and 1st) peak of the integral distribution:

- Is almost independent of the bias voltage
- Increase with the feedback resistor value but not linearly, maybe as square root.

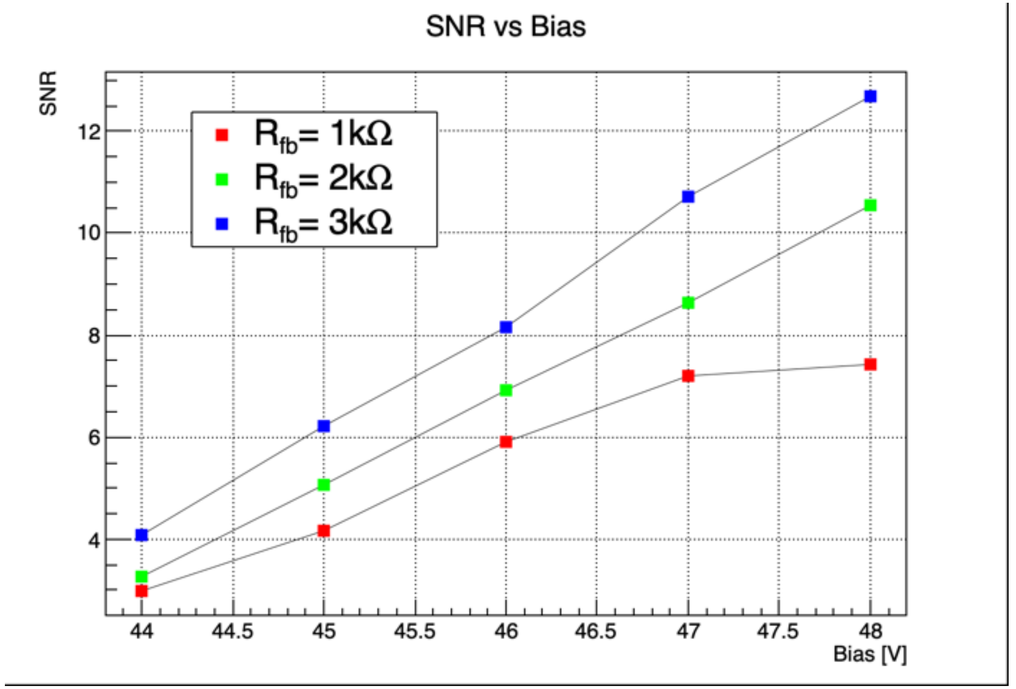


Signal Noise ratio



SNR increases with both overvoltage and feedback resistors:

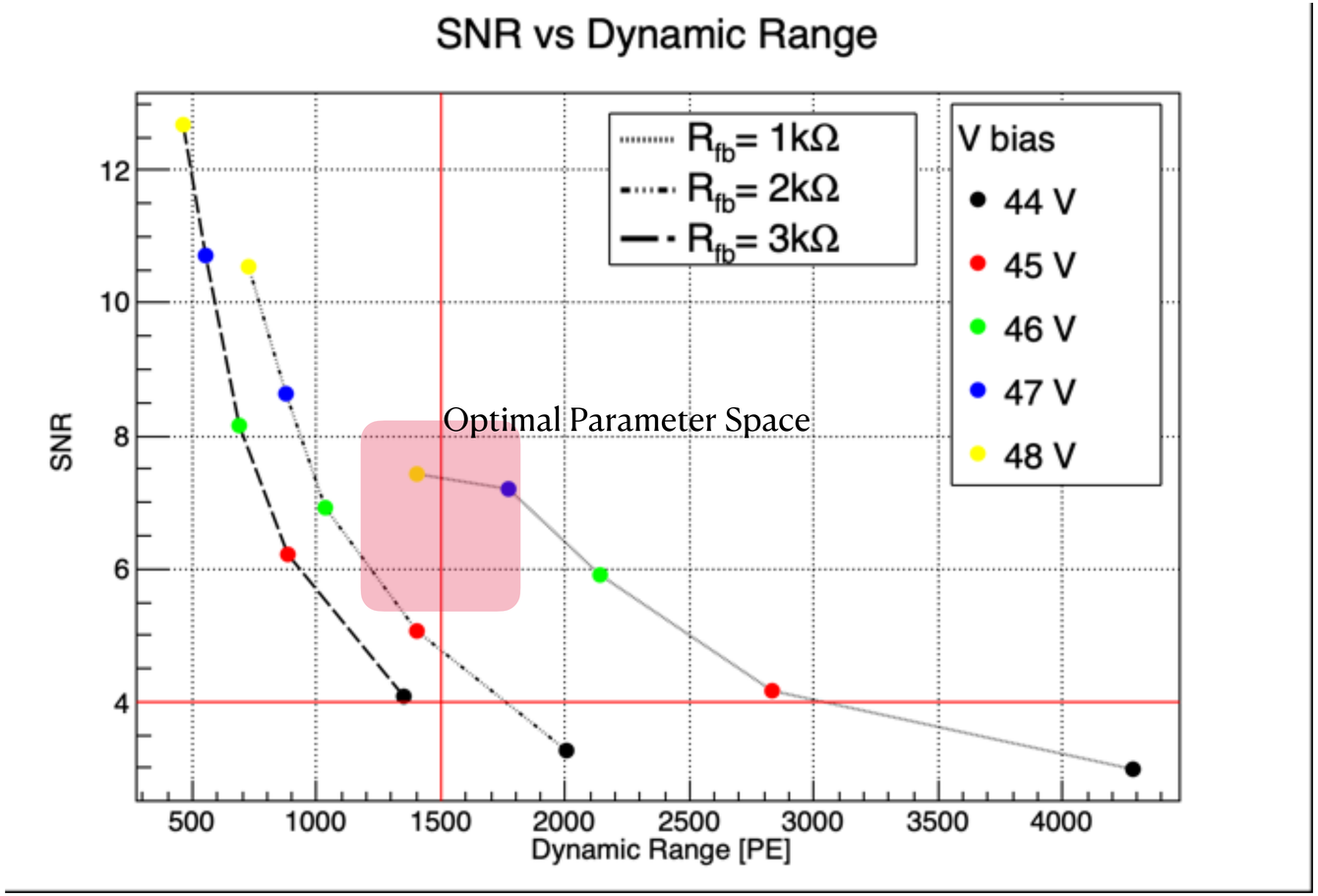
Linearly as a function of OV, much slower as a function of feedback resistors (DCEM Gain)



Signal noise ratio

- SNR increases with SPE amplitude.
- The signal can not be increased indefinitely because at its amplitude at some point limits the CE dynamic range.
- Setting a gain just above the dynamic range requirements gives the best performance in SNR.

The most efficient way to maximize the SNR is by increasing the bias voltage.



Once the bias voltage is set, a second tuning on the feedback resistor is made to adjust the SPE amplitude to be just above the dynamic range requirements.

R_{fb} & V_{bias} combinations w/ V_{bias} <47 V ($5V_{ov}$) have been found that preserve high SNR (>6) and large DR (~ 1500 PE)

SiPMs bias

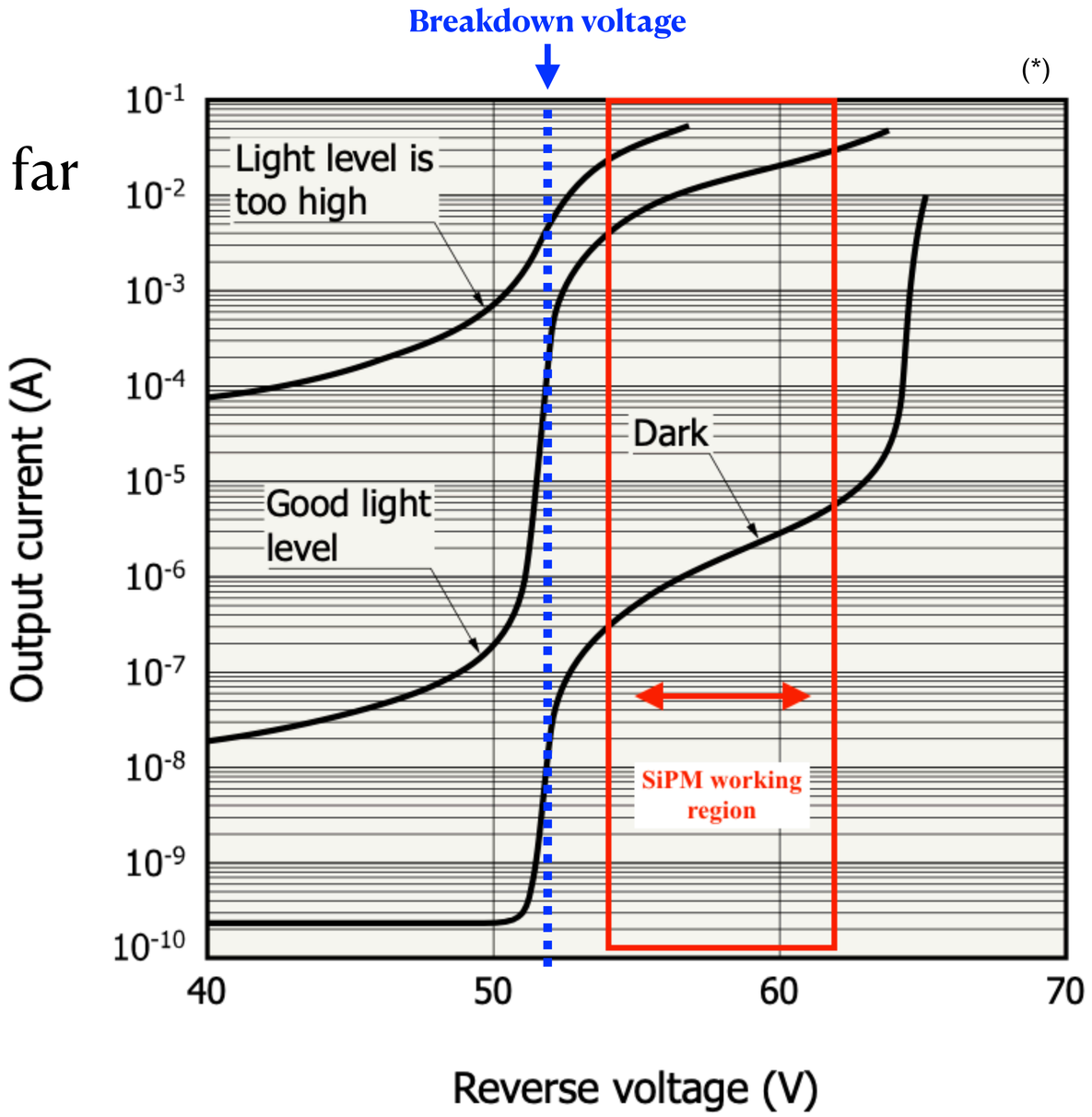
- Motivations for SiPM HPK V_{bias}^{VD} adopted so far

The choice of the SiPM bias needs to guarantee all SiPMs work in a stable regime.

Working too close to the V_{bd} transition region could result in a drop of the SiPM PDE.

Variations of the SiPM breakdown voltage can not be compensated adjusting the bias.

HPK MPPC documents indicate a working region for operating voltage where selecting optimal Vbias to match application



(*) https://www.hamamatsu.com/content/dam/hamamatsu-photonics/sites/documents/99_SALES_LIBRARY/ssd/mppc_kapd9005e.pdf

KAPDB0362EA

SiPMs bias

The current HPK SiPMs installed in Module-0 cathode modules are set at 47V which corresponds to an overvoltage of around +5V (60% PDE).

Matching max SNR (max single PE detection efficiency) & highest PDE assumed as goals of FD2 PDS application.

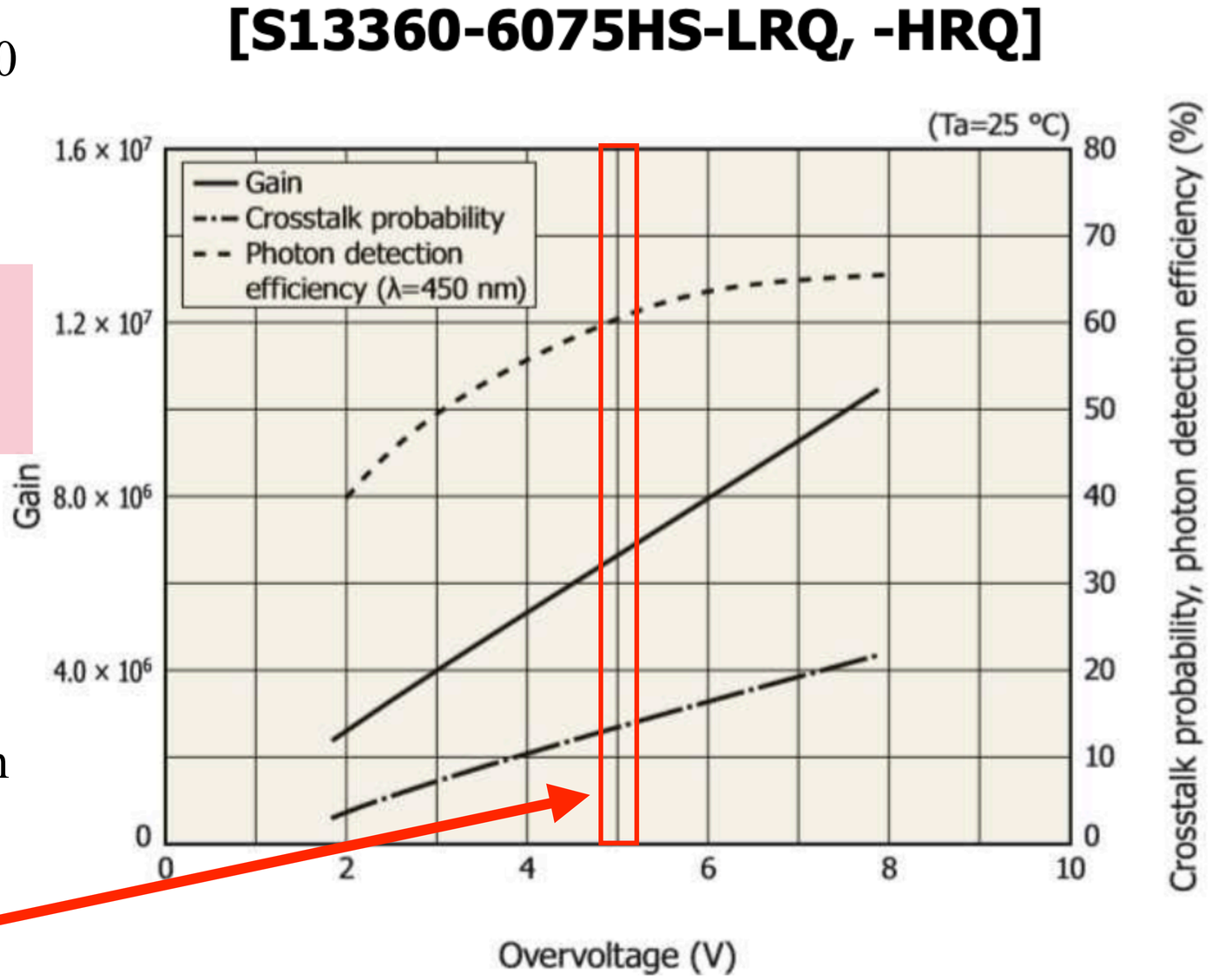
Breakdown voltage measured in LN2 for the HPK SiPM installed in Module 0 span in the range of 41.2 V to 42.2 V

[See spreadsheet]

Passing from LN2 to LAr we would expect an increase of 0.3V(?)

→ Breakdown = 42.0+/-0.5 V

→ 47V = 5 +/- 0.5 V of OV

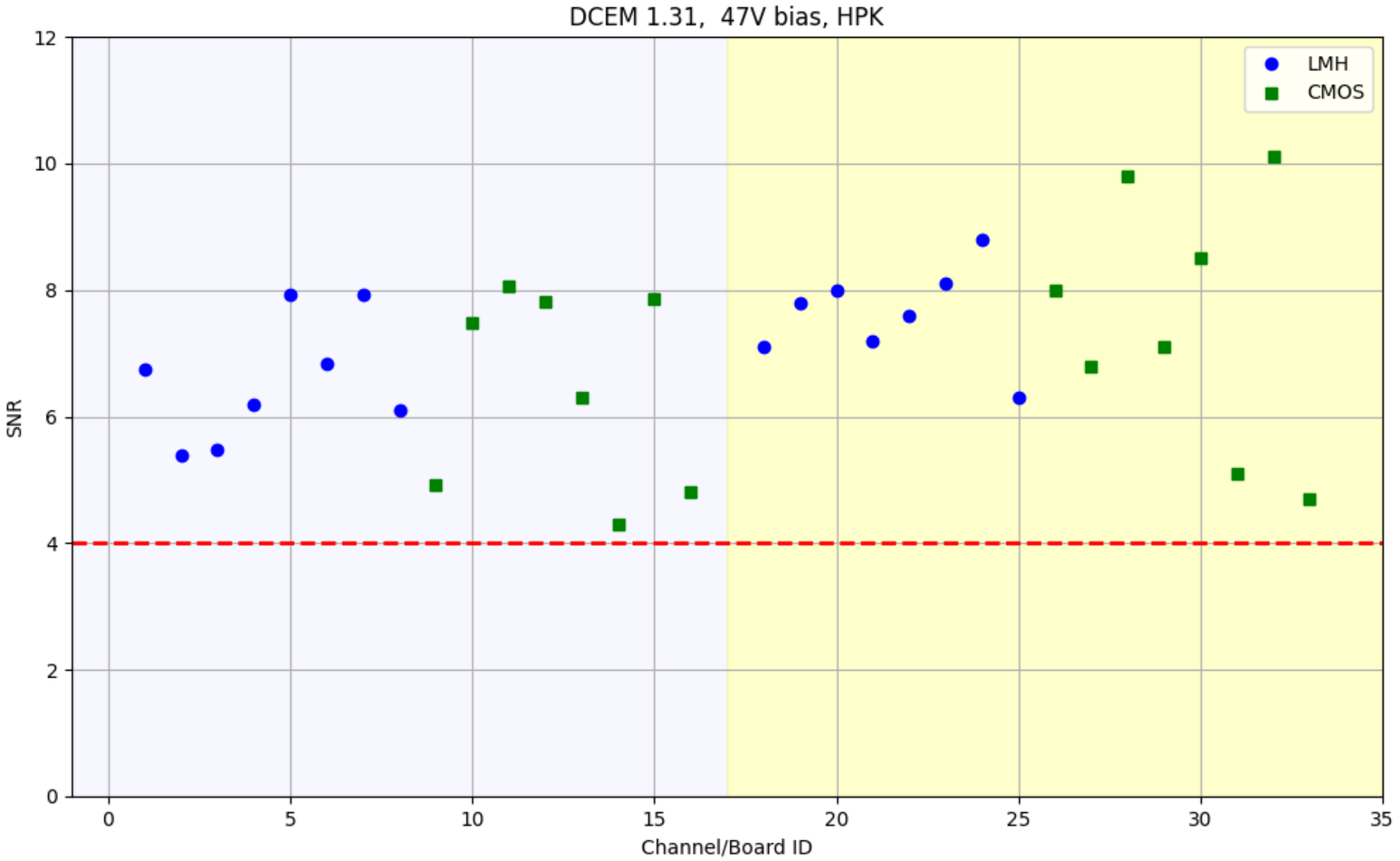


DCEM 1.31 performances summary

Module 0 summary results from 16 DCEM boards tested in LAr 4x HPK per channel, 47V bias.

Blue background:
(Boards installed in module 0)
- DCEM 1.31 LMH/CMOS
- tested at the CERN test stand
- SoF/PoF
- DCDC
- Koheron+CAEN r/o

Yellow background:
(Backup boards)
- DCEM 1.3 LMH/CMOS
- tested at Fermilab
- SoF
- PoC
- DCDC
- Koheron+oscilloscope r/o



Spread ch-to-ch of SNR due to mostly to test setup fibers readout.
The goal would be to choose Vbis and Rfb with high enough SNR (>>4 on average) to be sure all FD2 PD channels will be above requirement of SNR>4

SiPMs bias

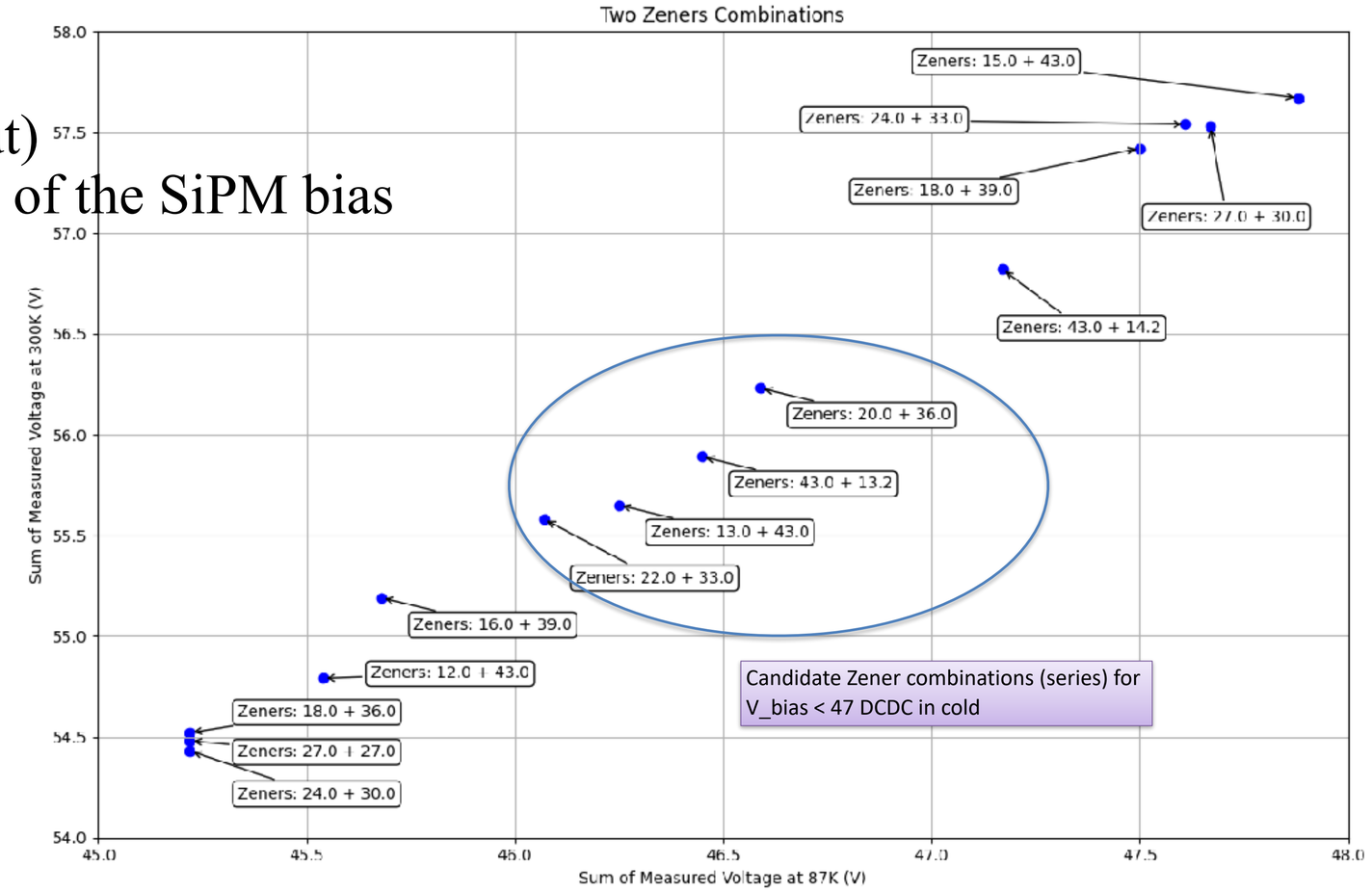
(due to used in DCDC circuit to set V_out)
the DCDC does not allow the fine-tuning of the SiPM bias

The PoF/bias system for the DUNE-VD cold electronics does not allow the tuning of the bias after installation.

- The SiPM bias is provided by the DCDC on the front-end CE.
- The DCDC bias voltage is set through Zener diodes in series.

The bias can not be set arbitrarily but only combining in series two Zener, **with finite number of available Zener diode values**

The bias voltage at room T and in LAr is strongly correlated.



The plot shows the measured bias values (warm vs cold) per each of the available Zener diodes combinations (test performed by Mike Miller measuring single Zeners)

DCDC proposed solution for Cold Box

DCDC group (Mike Miller) proposed two alternative solutions for biasing below 47V:

Nominal 13V + 43V zeners = 46.25 VDC at 87K and 55.7 VDC at 300K
Nominal 39V + 16V zeners = 45.70 VDC at 87K and 55.2 VDC at 300K

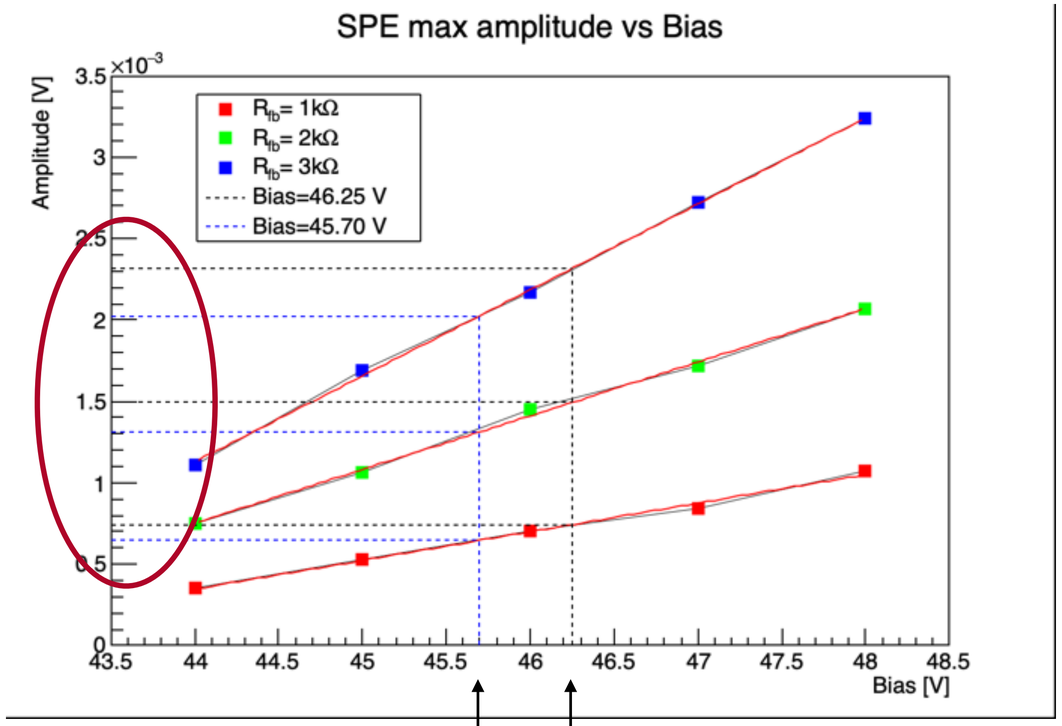
Those numbers are indicative and they need to be tested. We would expect some deviations.
The solution implemented in Module0 DCDC uses:

Nominal 27V + 30V zeners = 47.70 VDC at 87K and 57.5 VDC at 300K

With this configuration, the DCDC provides 47.0 VDC at 87K and 56.4 VDC at 300K
The tuning was made after multiple iterations probing different Zener diodes until the desired value was achieved.
Maybe not so precise since the DCDC was supposed to provide 46.8 V.

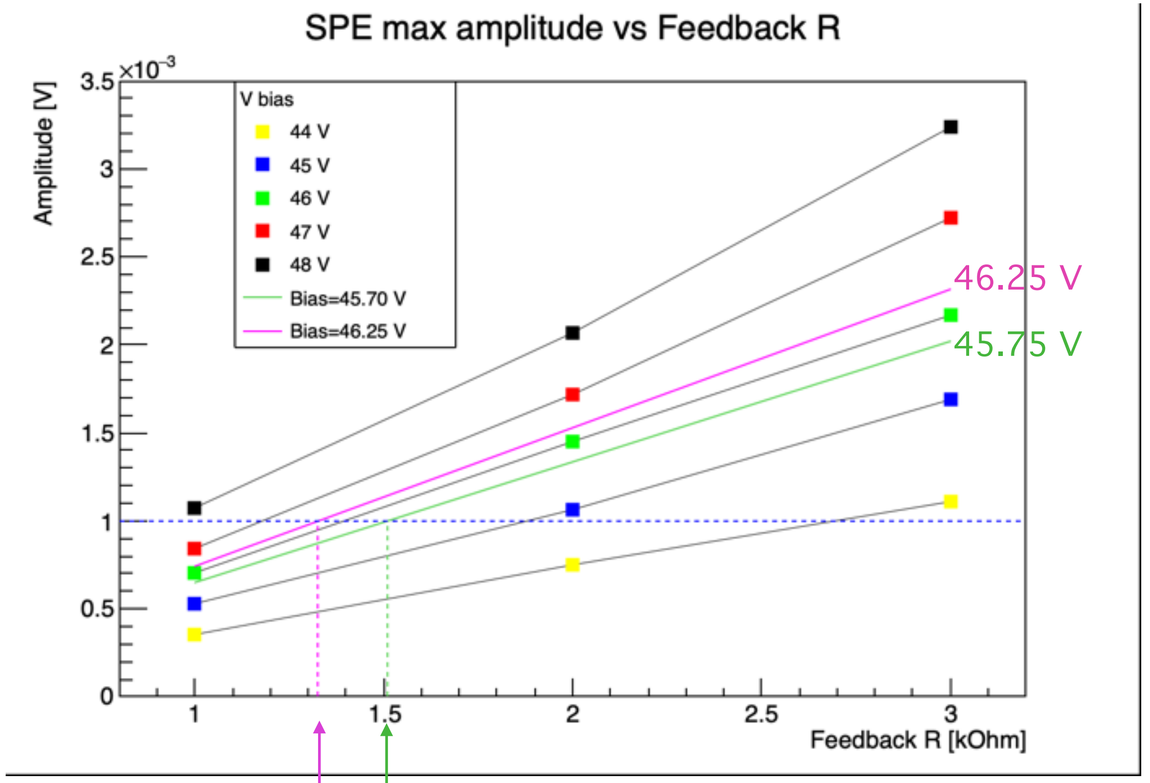
Gain Setup

Form SPE amp. vs Bias voltage plot it is possible to determine the SPE amp. for different feedback resitors



45.7V and 46.25V

Those numbers can be used to determine a suitable feedback resistor to matches the dynamic range



Ideal Feedback resistor values:
1.5 kOhm for 45.7V and
1.3 kOhm for 46.25V

DCDC proposed solution for VD-FD

Tuning the DCDC is not easy and we can not access all the values we want.

The DCDC can be tuned to an absolute value.

This could result in a limitation for the FD in matching the SiPM breakdown spread.

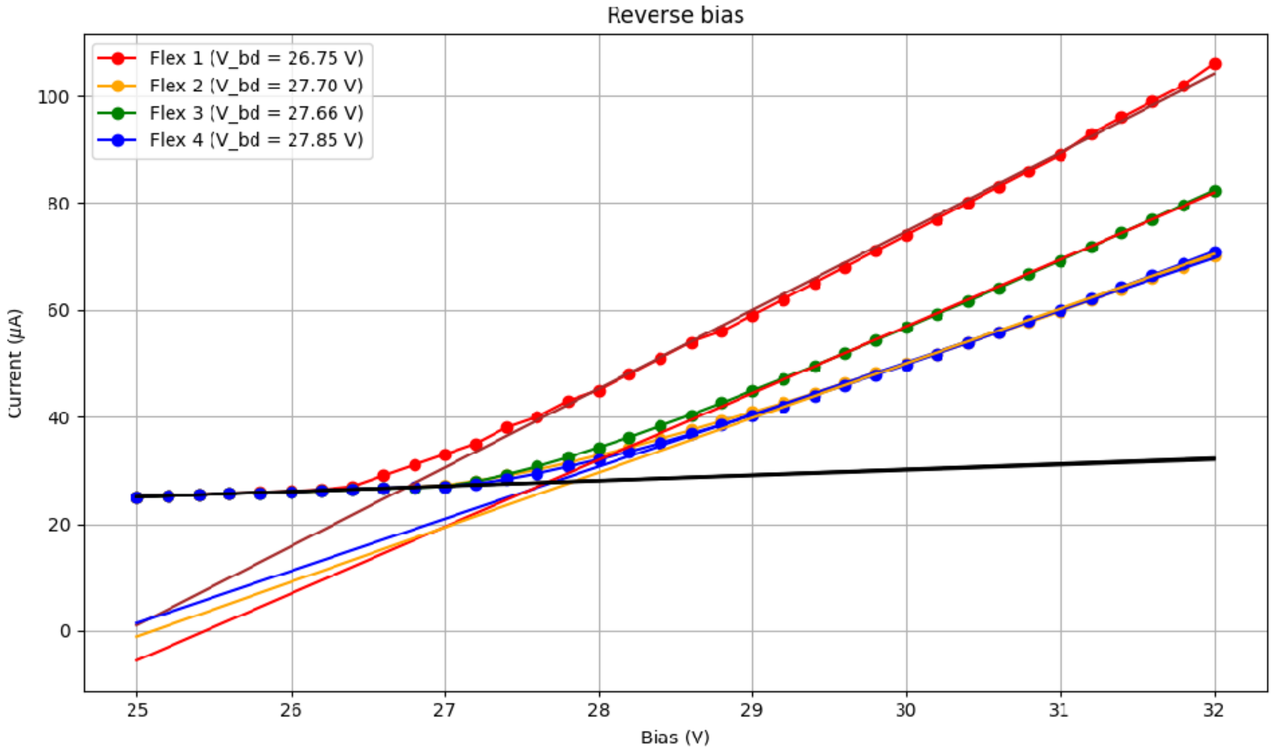
One of the proposal is to build 2 or 3 set of DCDCs tuned 0.5 V apart to reduce the spread in overvoltage.

Knowing what is the expected spread of the SiPM breakdown and in which percentage would be very helpful to consider this option.

Major problem we can see at the moment is resources to develop and work on the fine tuning of those DCDCs

Breakdown voltage spread

4x FBK flexes tested at Fermilab, one of them shows a breakdown voltage ~1V smaller than the other 3



Same HPK analysis has been made for FBK but using only 3 flexes… see other PDF document

Backup

Cross Talks overview

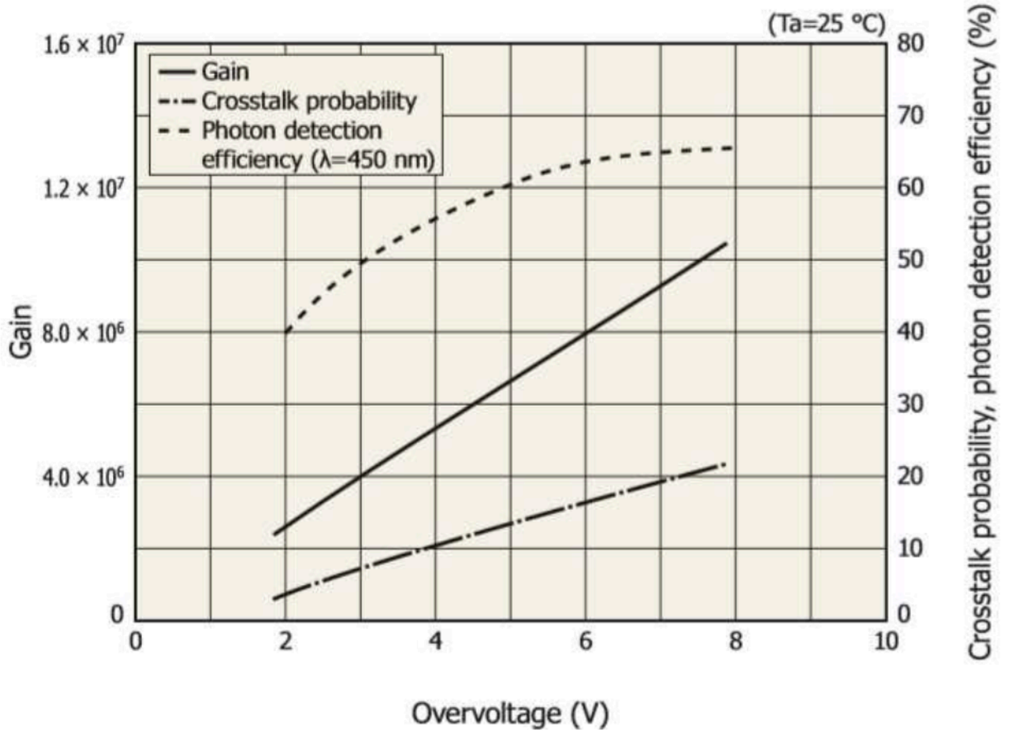
From Sergio Manthey CM slides

	FBK	Typical V_bd	~27 V @ LAr
PDE	V bias	Over Voltage	Cross Talks
50%	34.0 V	7.0 V	32.5%
45%	31.5 V	4.5 V	16.1%
40%	30.5 V	3.5 V	12.7%

From Francesco Di Capua CM slides

	FBK	Typical V_bd	~27 V @ LAr
PDE	V bias	Over Voltage	Cross Talks
50%	34.0 V	7.0 V	33%
47%(?)	33.0 V	6.0 V	25%
45%	31.5 V	4.5 V	18%

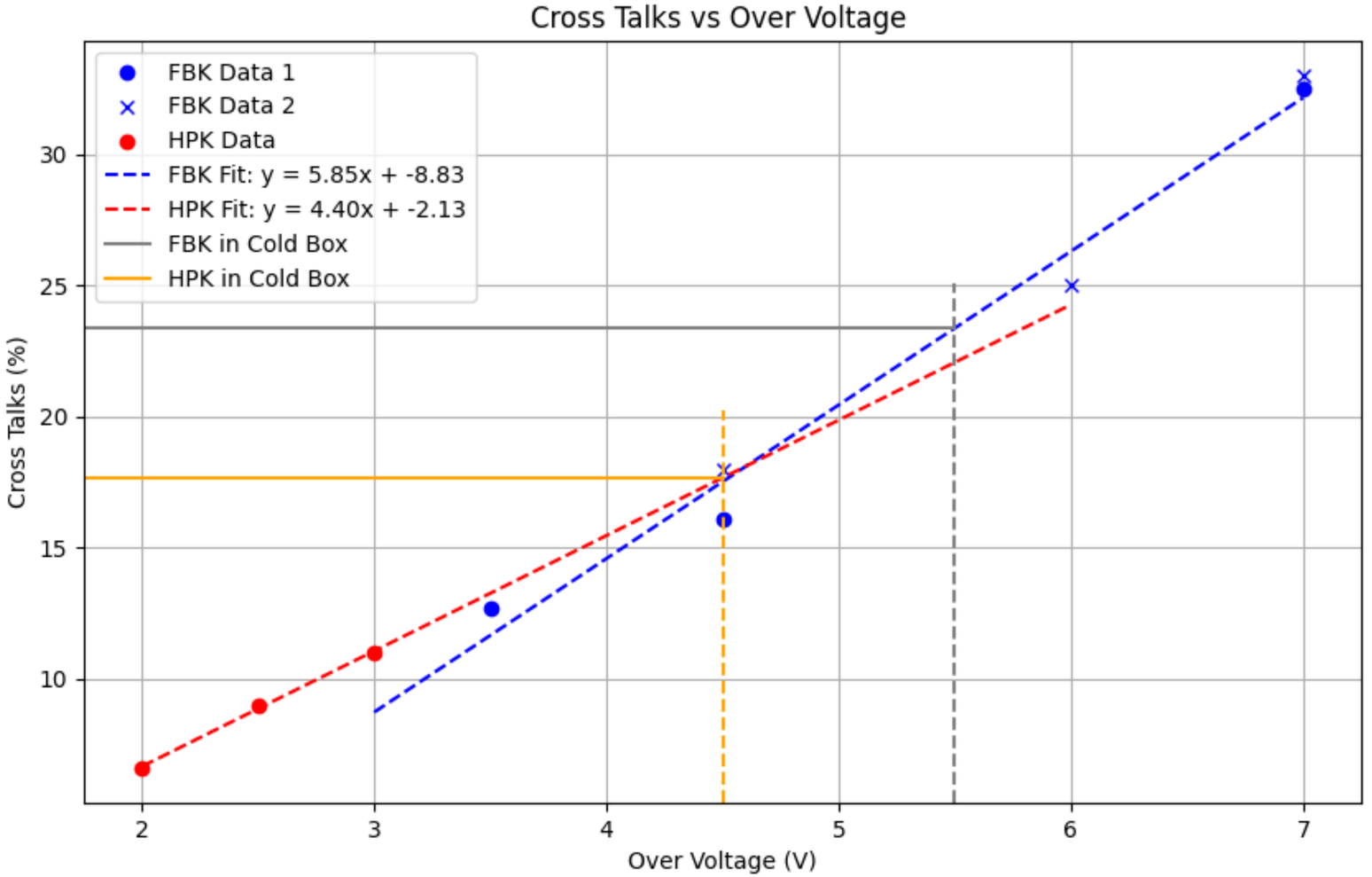
[S13360-6075HS-LRQ, -HRQ]



Form Ines

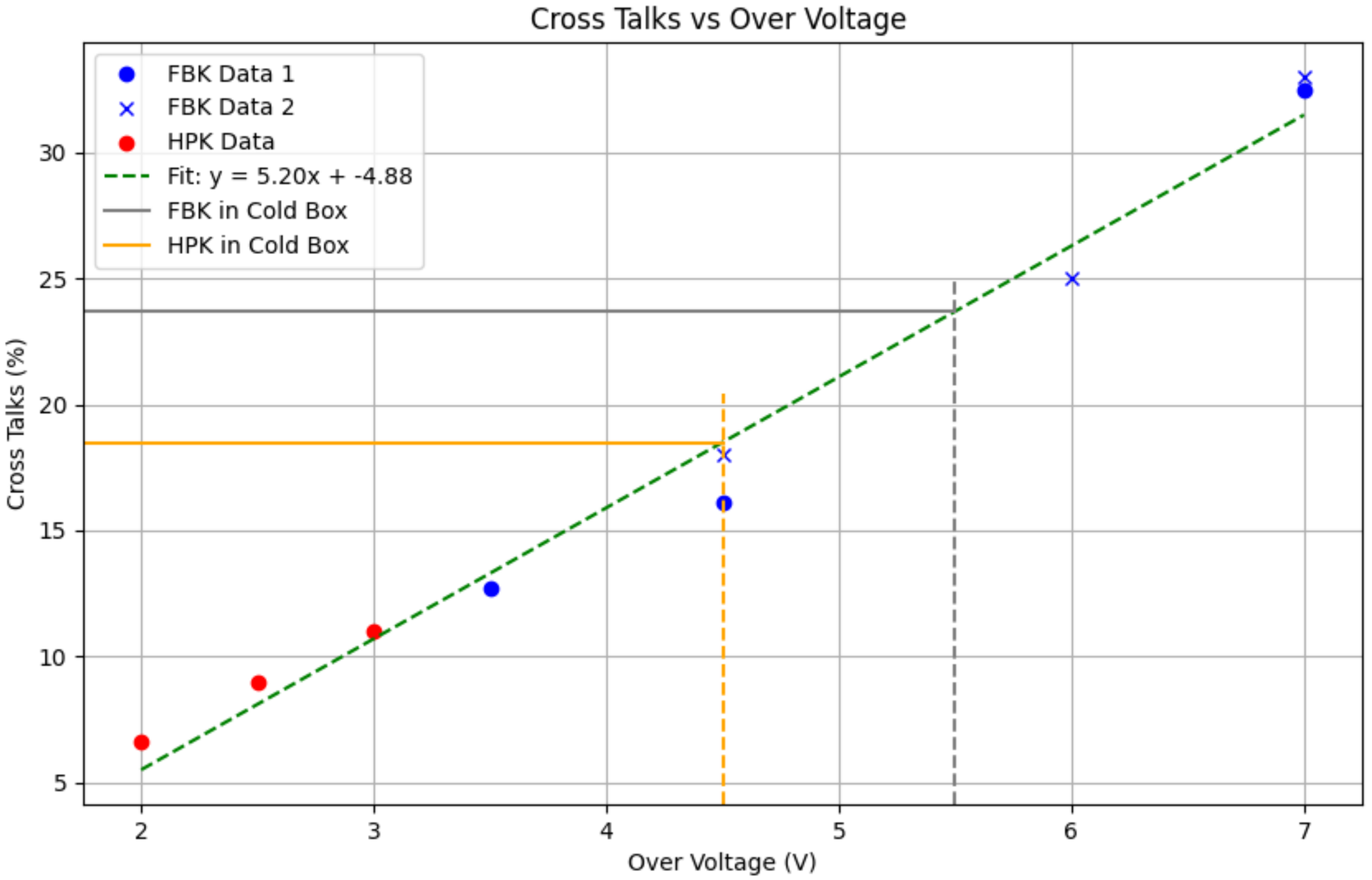
	HPK	Typical V_bd	~42 V @ LN2
PDE	V bias	Over Voltage	Cross Talks
50%	45.0 V	3.0 V	11.0%
45%	44.5 V	2.5 V	9.0%
40%	44.0 V	2.0 V	6.6%

Cross Talks vs Bias Voltage



Cross-Talks for FBK and HPK seem to have a very similar dependence from the Bias Voltage.

Cross Talks vs Bias Voltage



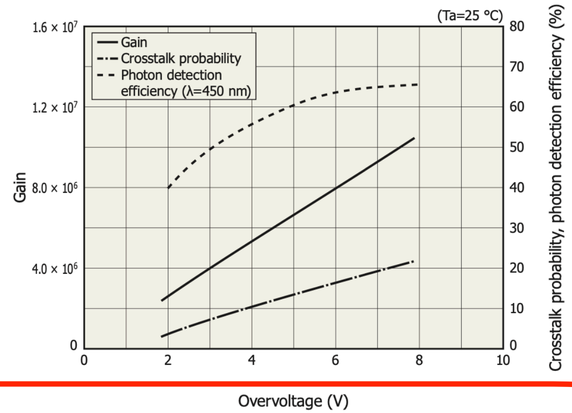
Same plot as before, but I fitted both FBK dataset and HPK dataset all together

From Hamamatsu datasheets

a high speed and low dark count are needed [Table 3-2]. The MPPC characteristics vary with the operating voltage [Table 3-3]. To deal with various applications, the MPPC operating voltage can be adjusted as desired over a wide setting range. To obtain an optimum MPPC performance, the operating voltage should be set higher in applications requiring a high gain, high photon detection efficiency, and superior time resolution, while it should be set lower in applications requiring low noise (low dark, low crosstalk, and low afterpulses).

MPPC (multi-pixel photon counter) | **S13360 series**

Pixel pitch: 75 µm



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MPPC characteristics vary with the operating voltage. Although increasing the operating voltage improves the photon detection efficiency and time resolution, it also increases the dark count and crosstalk at the same time, so an optimum operating voltage must be selected to match the application.

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NOTE: From photosensor group studies HPK shows similar or smaller crosstalks than FBK at the same overvoltage.

Module 0 backup board performances

Summary 2:

Same DCDC for [1,2, 5,6,7,8] [3, 4] have their own DCDC			Room T, no flexes connected						LAr, 4x HPK flex connecte in ch 2					
DCEM	Type	V_bias (V)	I (mA)	DCDC out (V)	DCDC LDO (V)	OpAmp LDO (V)	Offset Ch1 (mV)	Offset Ch2 (mV)	I (mA)	DCDC out (V)	DCDC LDO (V)	OpAmp LDO (V)	Offset Ch1 (mV)	Offset Ch2 (mV)
1	CMOS	5.3	124	56.3	4.99	4.99	185	195	60	47.0	5.02	5.00	135	117
2	CMOS	5.3	124	56.4	4.98	4.99	187	181	60	47.0	5.03	5.00	97	87
3	CMOS	5.3	126	56.4	4.98	5.00	205	184	60	47.0	4.93	4.95	125	83
4	CMOS	5.3	126	56.4	5.00	4.98	204	154	60	47.1	5.01	4.92	115	90
5	BiPolar	5.3	104	56.4	4.99	4.99	46	56	54	47.0	5.00	4.97	81	74
6	BiPolar	5.3	105	56.3	4.99	4.98	48	45	55	47.0	4.98	5.02	103	104
7	BiPolar	5.3	104	56.5	4.98	4.99	37	37	55	47.0	5.01	5.01	90	102
8	BiPolar	5.3	105	56.4	4.98	5.00	45	47	54	47.0	5.01	5.02	97	103

Summary 3:

4x HPK flex, LAr, DCDC		SNR		SNR (20 MhZ cut)		<SPE> ampl (mV)		Dynamic Range (Number of PE)		Undershoot (%)	
DCEM	Type	Ch1	Ch2	Ch1	Ch2	Ch1	Ch2	Ch1	Ch2	Ch1	Ch2
1	CMOS	8.0	6.8	8.1	8.3	1.1	1.2	1545	1417	1.9	1.5
2	CMOS	9.8	7.1	7.3	8.0	1.0	0.8	1600	1500	1.7	1.8
3	CMOS	8.5	5.1	9.2	5.2	1.0	1.0	1600	1600	1.8	2.1
4	CMOS	10.1	4.7	9.8	4.6	1.1	1.0	1545	1500	1.5	1.7
5	BiPolar	7.1	7.8	7.9	8.2	0.8	0.8	2000	2000	2.0	1.7
6	BiPolar	8.0	7.2	9.3	7.1	1.0	1.0	1700	1700	1.7	2.2
7	BiPolar	7.6	8.1	8.3	8.0	0.9	1.0	1889	1700	2.8	1.7
8	BiPolar	8.8	6.3	9.7	10.1	1.0	1.1	1700	1545	1.8	1.3

Module 0 installed board performances here