Precision timing ASIC

A recent real-life example:

The development of ETROC for CMS Endcap Timing Layer (ETL) using LGAD sensors

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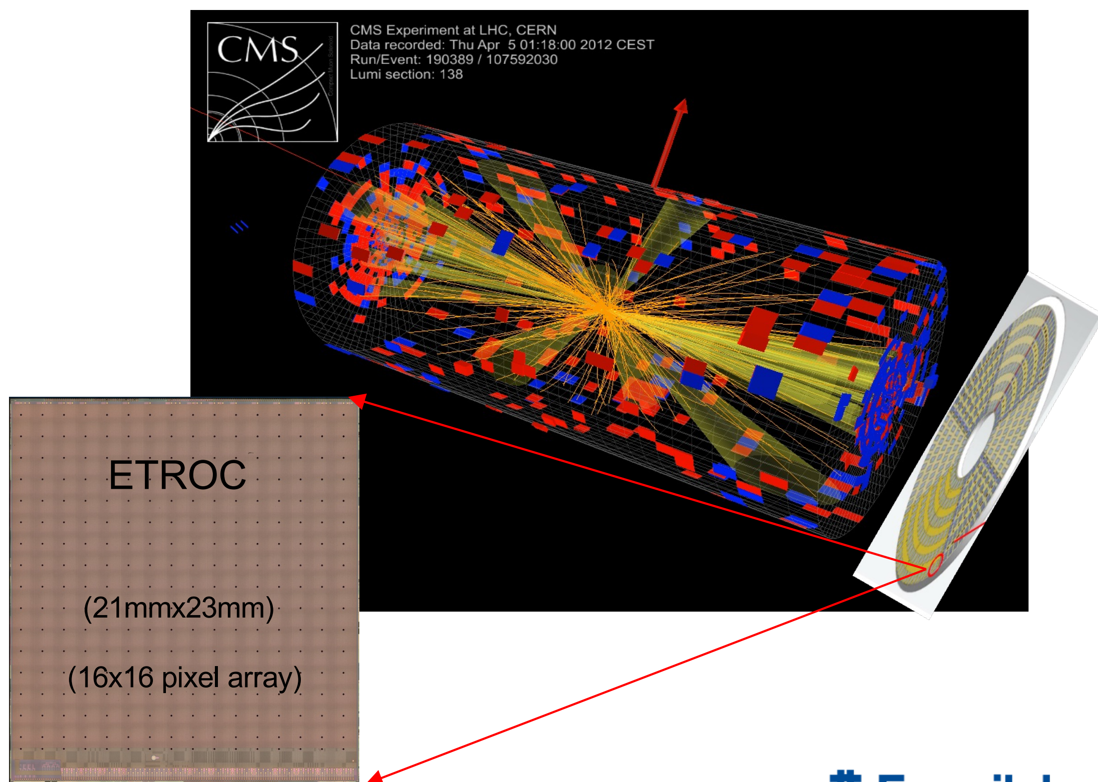
EDIT school at FNAL,
Nov 19, 2024

ASIC = “Application-specific integrated circuit”

Our design approach:
ASIC: “A System design Including a Chip”



ETROC: Endcap Timing ReadOut Chip

Outline of this lecture

- A brief history of time
  - Motivations of precision timing detector for HL-LHC and beyond
- How to approach precision timing ASIC design specifications: system considerations
- The development of ETROC: from initial prototypes to final ASIC
  - some unique challenges encountered and solutions
- What's involved in testing precision timing ASIC
  - some highlights of testing results/methods
- Future prospect with one R&D example

In this lecture, will use LGAD-based precision timing detector ASIC development as example: CMS Endcap Timing Layer (ETROC)

An old story from my graduate school days (CLEO experiment at Cornell Wilson Lab)

Long ago, a young theoretical physicist had real trouble finding a girlfriend for a *long* time. Very frustrated, he complained to Hans Bethe at Cornell, Hans's advice (with his strong German accent):

Young man, if the cross section is so low, increase the luminosity !

Rate = $\sigma \mathcal{L}$

σ - cross-section

probability that an interaction will occur

Good advice for HEP over the past four decades and beyond…

Hans Bethe: Nobel Prize in 1967 for his work on theory of stellar nucleosynthesis
"supreme problem - solver of the 20th century" -- Freeman Dyson (Princeton)

40+ years ago …

LBL-
Apri

PROCEEDINGS
OF THE
1983 DPF WORKSHOP
ON

Collider Detectors:
Present Capabilities
And
Future Possibilities

February 28 - March 4, 1983

Lawrence Berkeley Laboratory
University of California
Berkeley, California 94720

Edited By
Stewart C. Loken and Peter Nemethy

Prepared for the U.S. Department of Energy under Contract DE-AC03-76SF00098 and for the High Energy Physics Section of the National Science Foundation.

FOREWORD

The "Workshop on Collider Detectors: Present Capabilities and Future Possibilities" was sponsored by the Division of Particles and Fields of the APS and hosted by Lawrence Berkeley Laboratory. It was held at LBL from February 28th to March 4th, 1983.

The organizing committee consisted of A.K. Mann (Chairman), C. Baltay, R. Diebold, H. Gordon, D. Hartill, P. Nemethy, D. Ritson and R. Schwitters. The local organizing committee was R. Cahn, S. Loken and P. Nemethy.

The workshop focused on the problems posed by high luminosities at hadron colliders, considering luminosities on a continuous range from 10^{29} to 10^{34} cm^{-2} sec^{-1}, picking two specific center-of-mass energies, 1 TeV and 20 TeV. The participants divided into the five working groups tabulated below.

These proceedings contain three sections. Section I consists of input to the workshop, the introductory comments of the organizing committee chairman (A.K. Mann); two out of our three invited talks (W.J. Willis, M. Banner, C. Rubbia) on collider experience; finally two documents, which were invaluable in getting the workshop started, theoretical estimates of relevant cross sections (R. Cahn) and of high $P_{\perp}$ jet behavior (F. Paige).

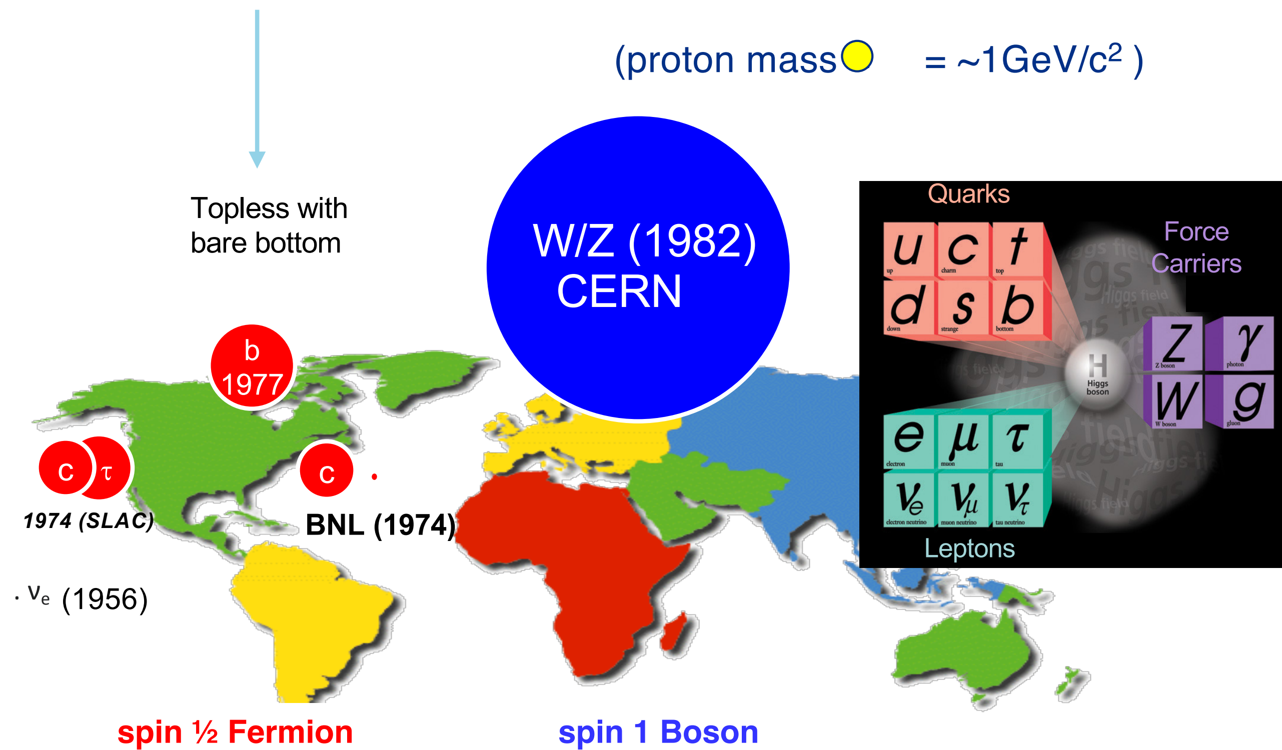
The workshop focused on the problems posed by high luminosity at hadron colliders, … from 10^{29} to 10^{34} cm^{-2} s^{-1} …1 TeV and 20 TeV energy….

vided by the Department of Energy and the National Science Foundation.

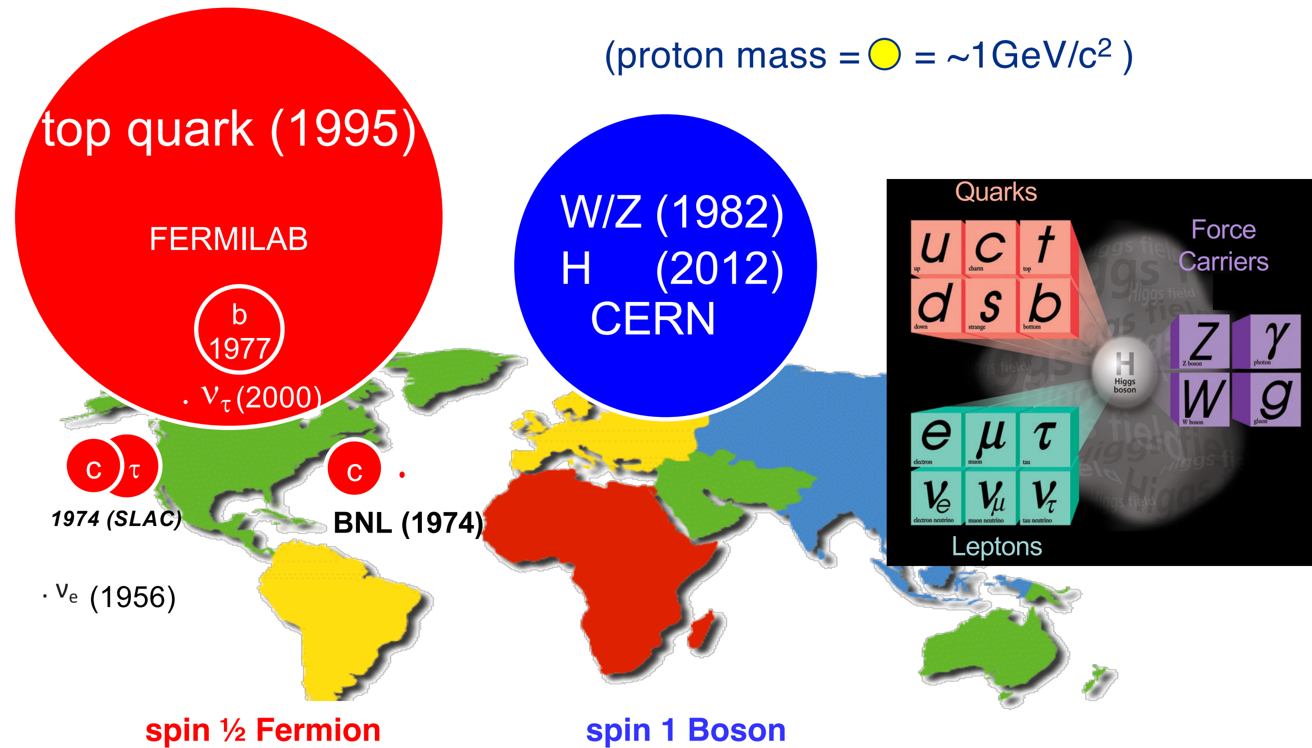
At that time, the workshop proceedings didn't mention precision position silicon tracker that later became critical to top quark discovery and Higgs discovery …

Today, we are developing precision timing silicon detector (LGAD based) for HL-LHC upgrade

Fermilab Tevatron Physics BEFORE 1990 (before sensor + ASIC):

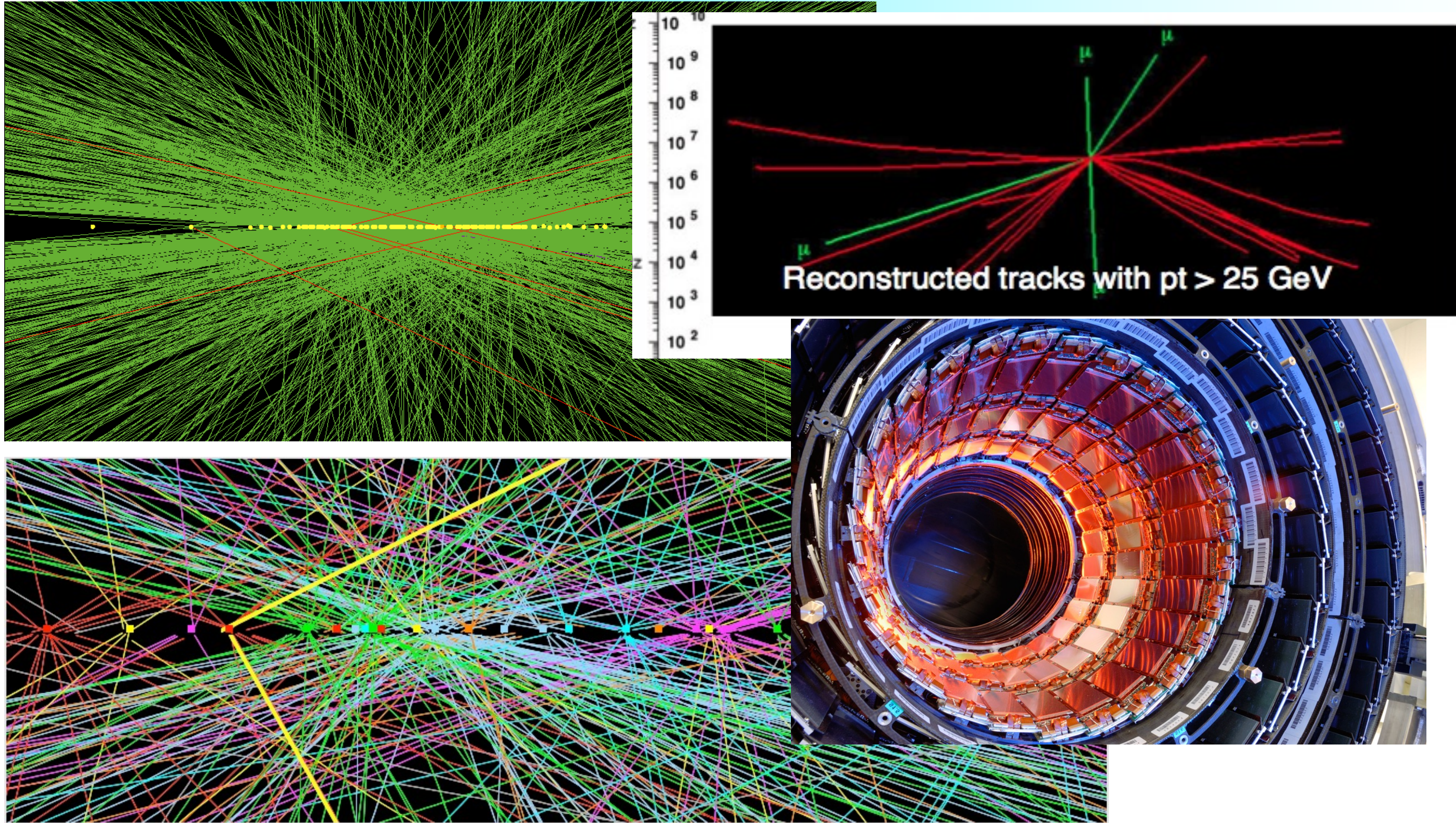


Particle Physics since 1990 (enabled by sensor + ASICs)



Historically, sensor and ASIC have played a critical role in HEP since ~1990s

Higher luminosity means higher pile-up events

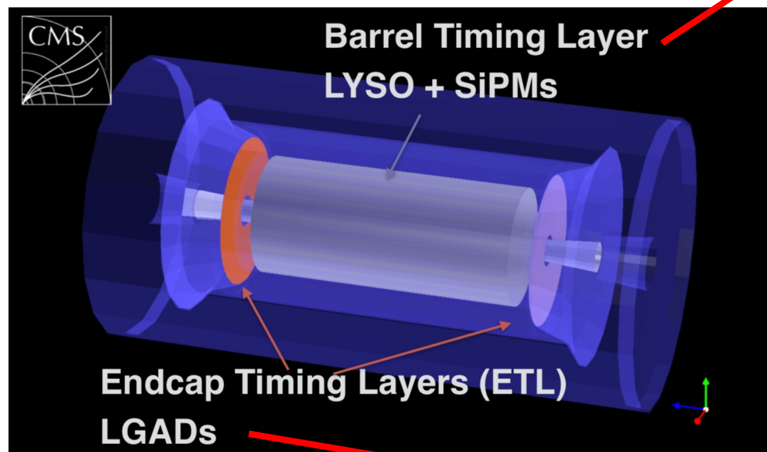


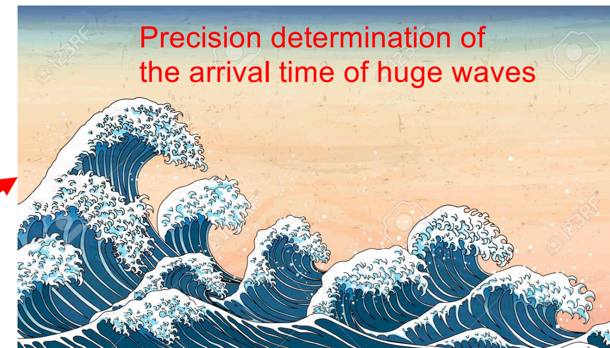
Silicon tracker with precision position information alone will not be enough to separate the pile-up events, precision timing detector can help: ***CMS Endcap Timing Layer (ETL) is designed for this purpose***

CMS new MTD (MIP Timing Detector)

CMS MTD: BTL and ETL are among the first generation precision timing detectors:

challenging front-end electronics design, tons of progress have been made over recent years



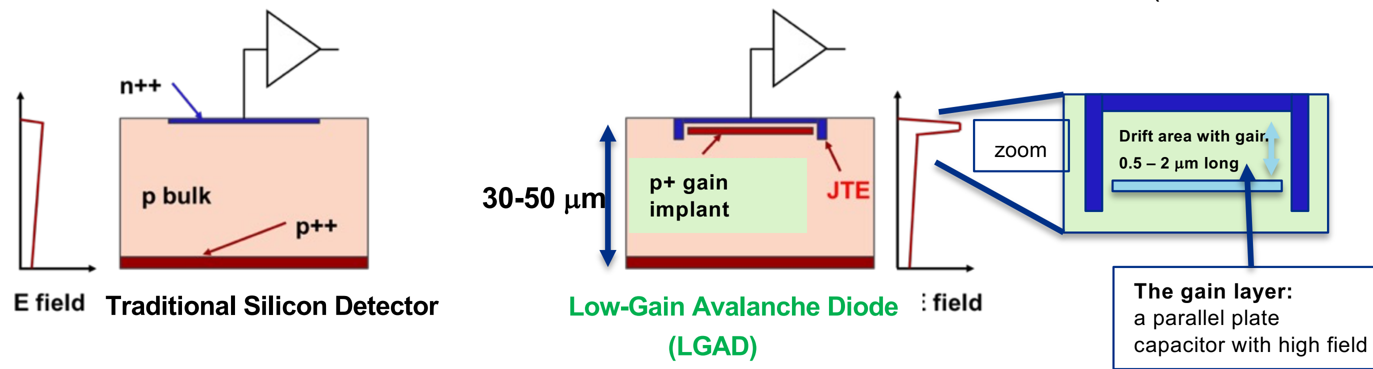


- Thin layers between tracker and calorimeters (BTL single layer, ETL double)
- with about ~ ***30-50 ps per track*** resolution

Ultra-Fast Silicon Detectors (LGAD)

FAST

A slide from Nicolo Cartiglia (CMS/ETL LGAD sensor expert)



- In UFSD, a moderately p-doped implant creates a volume of high field, where charge multiplication happens.
- The low gain allows segmenting and keeping the shot noise below the electronic noise since the leakage current is low.

Low gain is the key ingredient to excellent temporal resolution

This means low signal size → requires very low noise

Ultra Fast Silicon Detectors

UFSD are LGAD detectors optimized to achieve the best possible time resolution

Specifically:

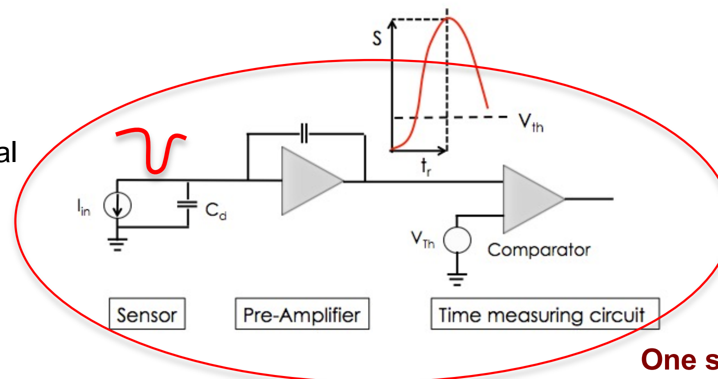
Thinner with better timing resolution

1. Thin to maximize the slew rate (dV/dt)
2. Parallel plate – like geometries (pixels..) for most uniform weighting field
3. High electric field to maximize the drift velocity
4. Highest possible resistivity to have uniform E field
5. Small size to keep the capacitance low — 1.3mm x 1.3mm at 50um thick: ~ 3-4pF
6. Small volumes to keep the leakage current low (shot noise)

One system: sensor and ASIC

A slide from Nicolo Cartiglia

- Sensors produce a current pulse
- The read-out measures the time of arrival



One single system

Sensors and read-out are two parts of a single object

Sensors and electronics succeed (or eventually fail) together

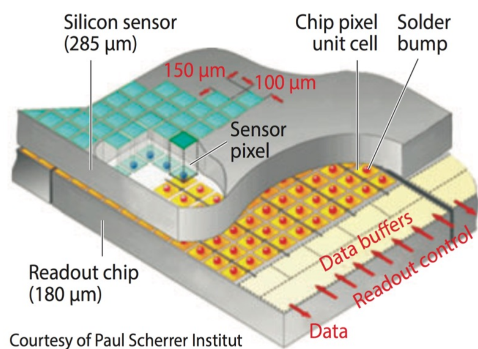
In "timing circuits" things can go wrong very rapidly (quote stolen from a chip designer)

==> This is not a simple evolution of what we know how to do.

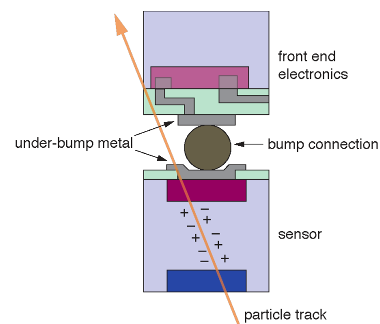
Hybrid Pixel Detectors: general concept

A slide from
Frank Hartmann

"Flip-Chip" pixel detector:
On top the Si detector, below the readout chip, bump bonds make the electrical connection for each pixel.



Detail of bump bond connection. Bottom is the detector, on top the readout chip:



L. Rossi, *Pixel Detectors Hybridisation*, Nucl. Instr. Meth. A **501**, 239 (2003)

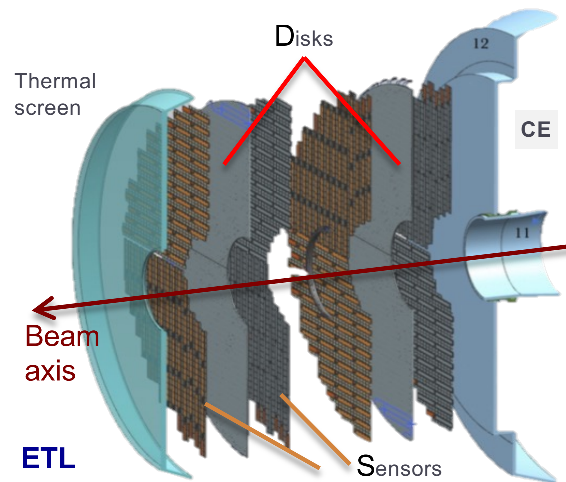
Hybrid
LGAD
detector

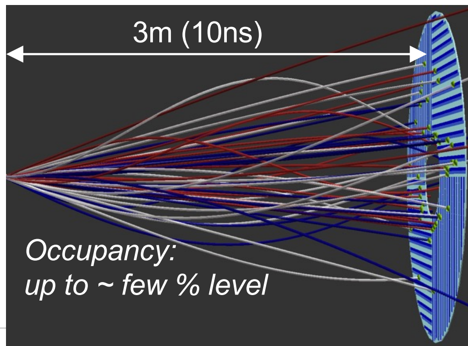
Bump bond
between:

Front-end
electronics(ASIC)
&
LGAD pixel/pad

CMS ETL precision timing *challenges*

Extract precision timing information from small LGAD signal size at high radiation dose





- Low Gain Avalanche Detectors (LGADs)
  - Basic unit:
    - 2x2 cm² LGAD bump-bonded to ETROC ASIC mounted on two sides of cooling plates
  - Two layers/disks per endcap (~2 hits per track)
  - 1.6 < |η| < 3.0, surface ~14 m²; ~9 M channels
  - Nominal fluence: ***$1.7x10^{15}$ n_{eq}/cm^2*** (@ 3000 fb^{-1})
- LGAD gain modest: 10-30
  - LGAD Landau contribution: ~ 30ps
  - Front-end contribution should be kept < 40ps
  - < 50ps per hit, or 35ps per track (with 2 hits)
- ***Extract precision timing from***

  Small LGAD signal (typical 10-20 fC)
  - ***With low power: < 4mW/channel on average***

ETROC design challenges:

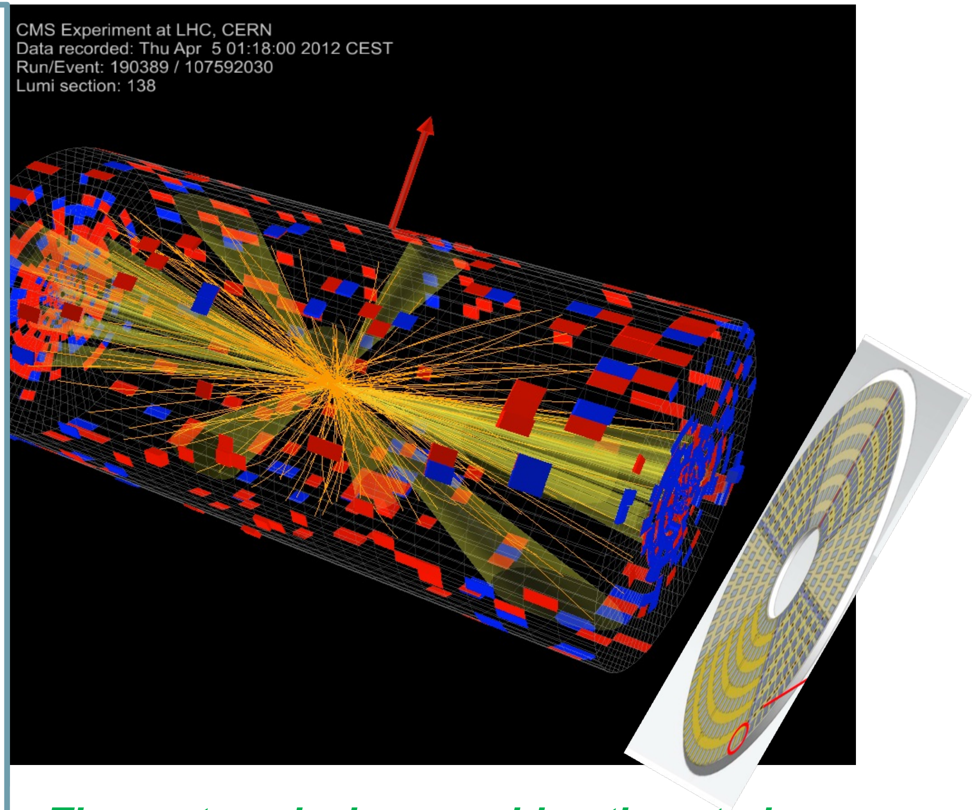
Low power and fast/precision timing, with low noise
Precision clock distribution,
Minimizing readout digital activities → low noise

Let's consider the case: CMS Endcap Timing Layer
to design a timing detector for the endcap using LGAD sensors

Some system design considerations

- Single layer vs multi-layer design
  - Single layer or more?
- Occupancy vs pixelization
  - What's pixel size should be?
- Power & cooling capacity
  - Faster timing → higher power
- Clock distribution
  - from system to lowest level
- Front-end design optimization strategy
  - How to optimize at design stage

….



The system design consideration study initially done around summer of 2018

Let's consider the case: CMS Endcap Timing Layer
to design a timing detector for the endcap using LGAD sensors

Some system design considerations

- Single layer vs multi-layer design
  - Single layer or more?

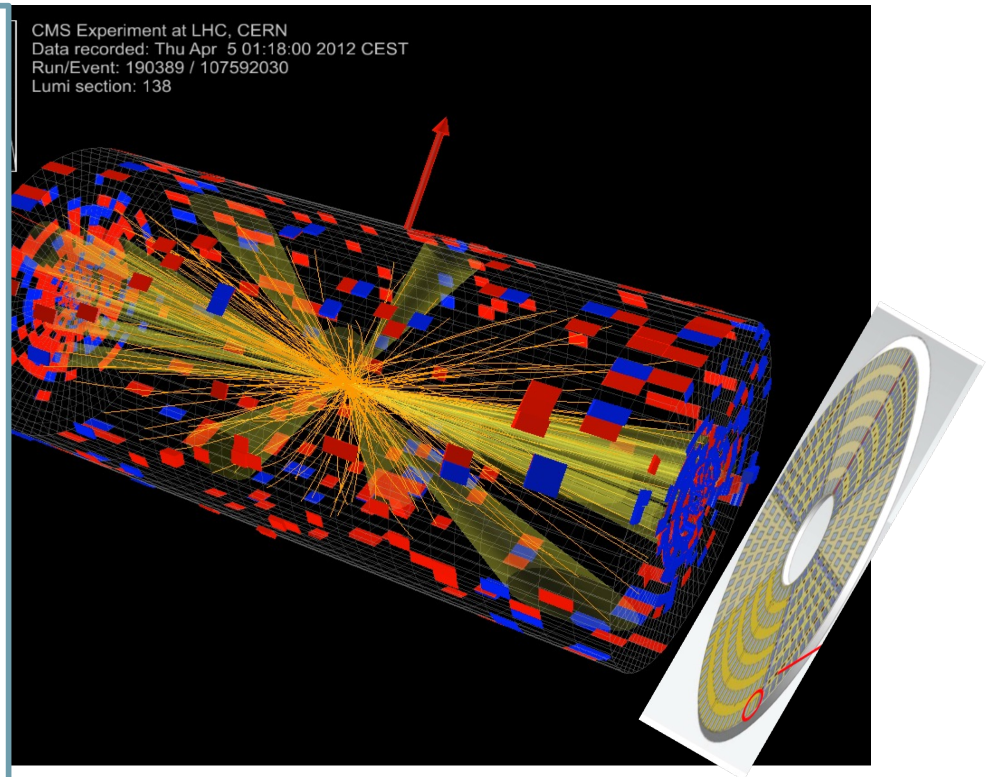
The ETL design goal is to achieve timing resolution of
~35 ps per track (~60 ps @ end of life)

1) If single layer:

the LGAD contribution is already at 30-40ps level, leaving not much room for ASIC to contribute:
would require almost ideal ASIC

2) If ***double layer:***
only 50ps per hit is required
(50/sqrt (2) = ~35ps)

ASIC design spec is much relaxed this way



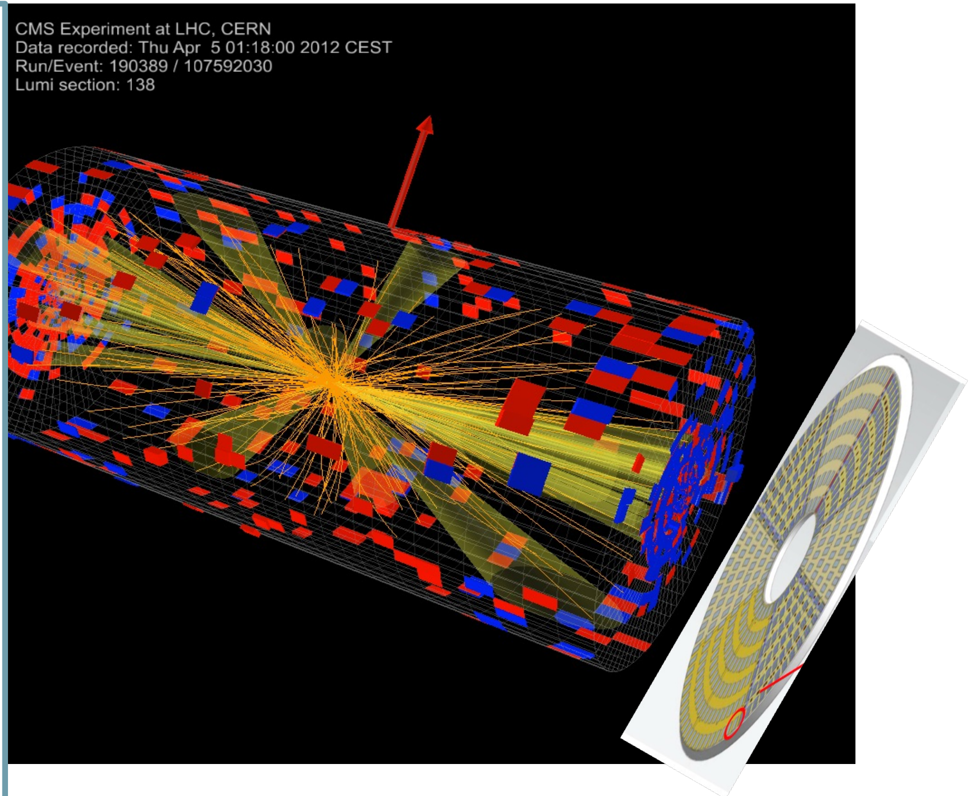
Let's consider the case: CMS Endcap Timing Layer to design a timing detector for the endcap using LGAD sensors

Some system design considerations

- Occupancy vs pixelization vs power vs footprint
  - What pixel size should be?

Would like to keep pixel level occupancy at few %, and also smaller pixel size → smaller input capacitance for preamplifier

After much design considerations, the size of pixel chosen to be 1.3 mm x 1.3mm (~3.4 pF).



Let's consider the case: CMS Endcap Timing Layer
to design a timing detector for the endcap using LGAD sensors

Some system design considerations

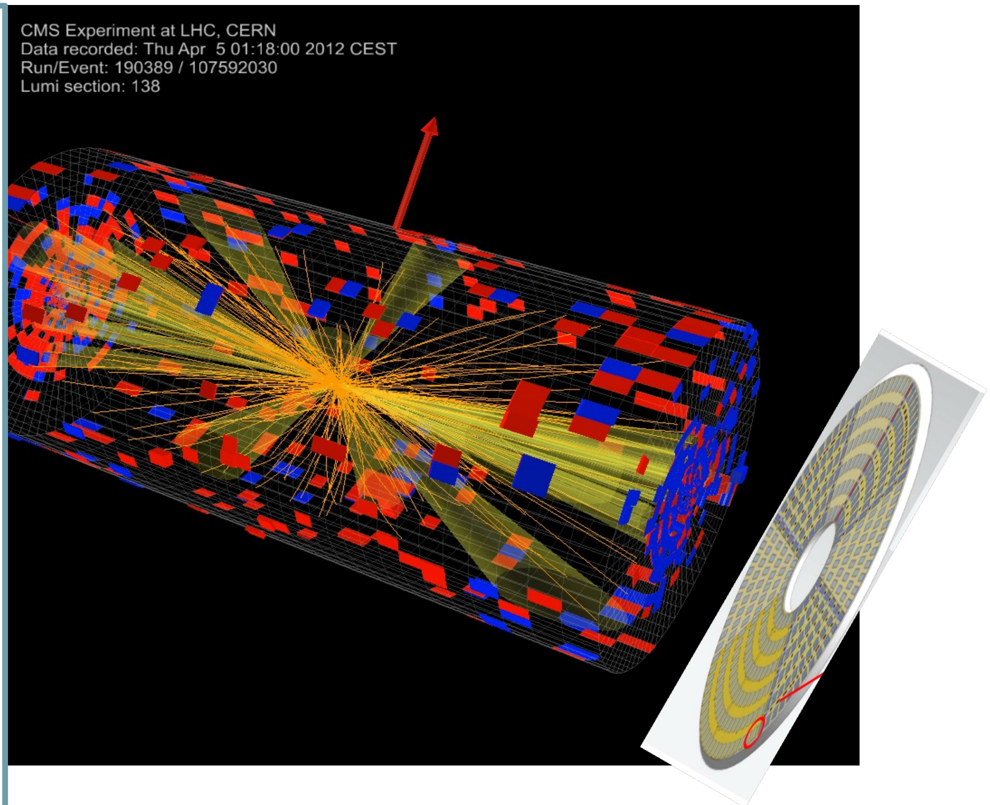
- Power & cooling capacity
  - Faster timing → higher power

At system level, power & cooling capacity is limited, proper specification is crucial to the ASIC design, and require plenty of safety margin

This also means that the ASIC design has to be optimized for low power consumption:

The system design requires that
the specification of ASIC power: < 1W/chip
This means: ~2-3mW per pixel

Will come back to this point later



Let's consider the case: CMS Endcap Timing Layer
to design a timing detector for the endcap using LGAD sensors

Some system design considerations

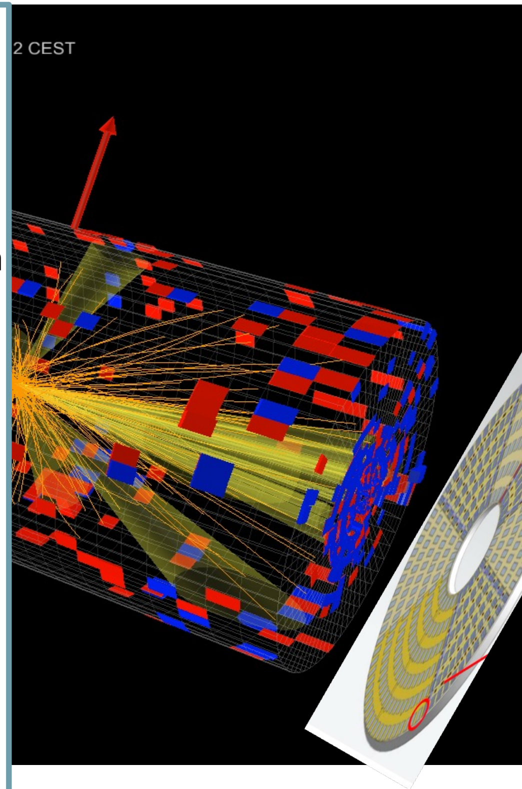
- Clock distribution
  - from system to lowest level

The jitter contribution from clock distribution has to be kept below 15ps at system level

This is new challenge
to HEP detector system design.

For ETROC, the goal is to keep internal clock distribution jitter below 10ps

Will come back to this later



Other system design considerations:

Design for Testability:

How to test at chip level, at system level, during production QA/QC, during detector installation and commissioning?

Design for monitoring/calibration/operation

How to monitor and calibrate during detector operation?
How to make it easier?

ETROC design are based
on past three decades of operational
experiences with actual detectors/ASICs:
such as Babar/CDF/CMS…

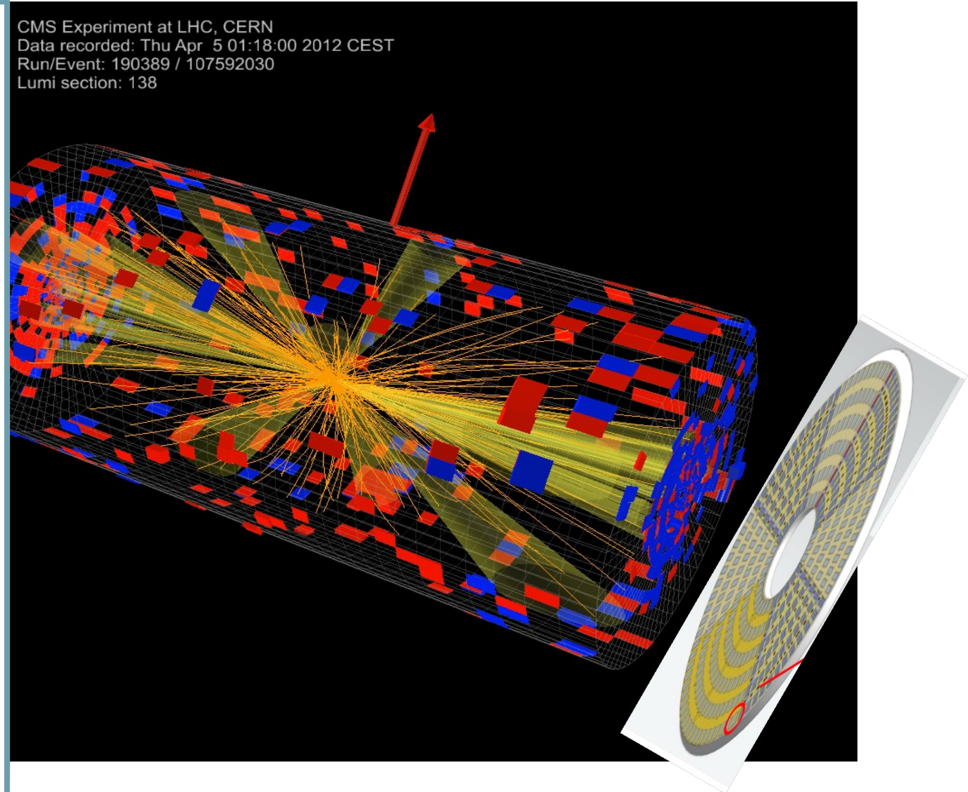
Let's consider the case: CMS Endcap Timing Layer
to design a timing detector for the endcap using LGAD sensors

Some system design considerations

- Front-end design optimization strategy
  - How to optimize at design stage

With the system design in mind, the front-end of the ASIC design can be optimized.

Proper System Design is the Key to the success of any challenging ASIC project



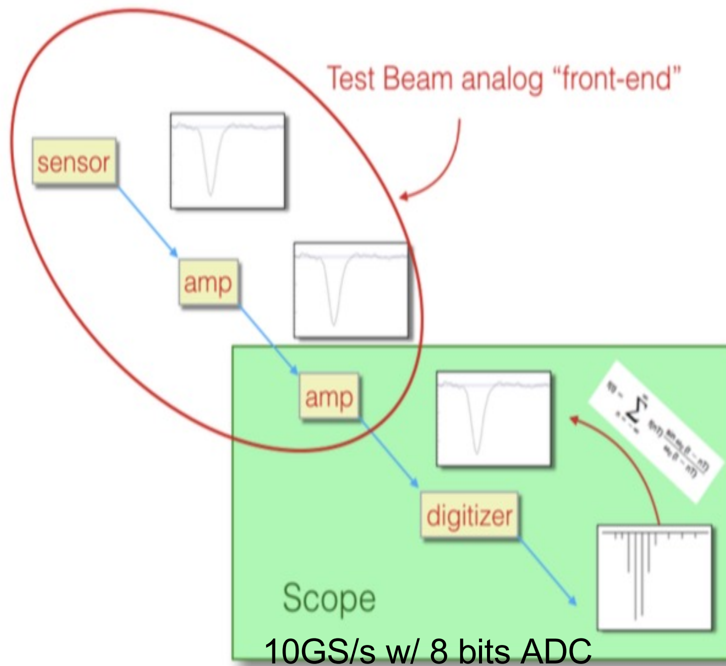
Methodology to approach the front-end design

- A three pronged approach is taken to consider the ASIC and the sensor together from the start to ***optimize the front-end design for LGAD behavior at end of operations*** (low signal size etc)
  1. Use the ***LGAD beam test data*** as input , to study different timing algorithms
     - *Leading Edge with Time Over Threshold (TOA/TOT)*
     - Constant Fraction Discrimination (CFD)
  2. Use ***LGAD simulation as input***, ***simulating different front-end design concepts***
  3. Simulate and optimize the expected performance of the actual ASIC implementation ***with post-layout simulation, using LGAD simulation as input***

The three-pronged design approach has been highly effective

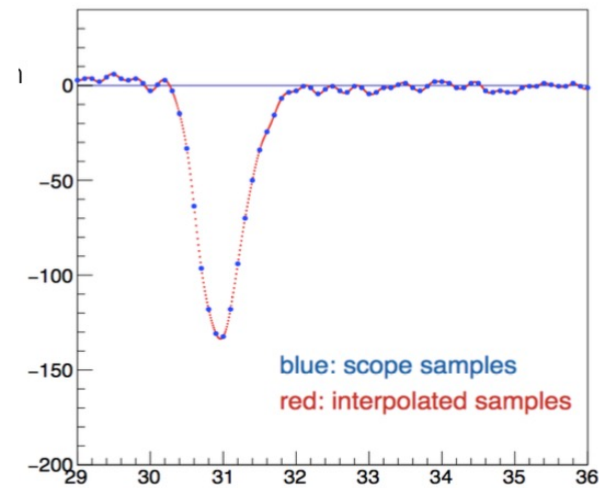
Fermilab

Waveform analysis: LGAD Test beam data



10GS/s w/ 8 bits ADC

Fermilab test beam data for LGAD: to guide the design of the front-end using sampled waveforms recorded with scope.



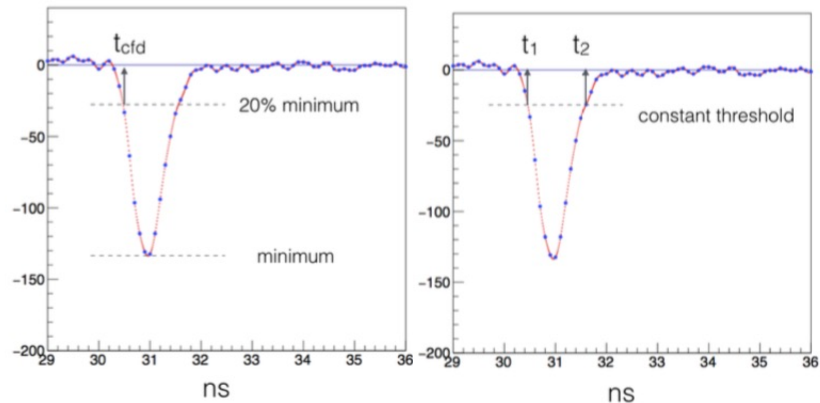
The functional interpolated signal is used to simulate the discriminator response and study timing algorithms

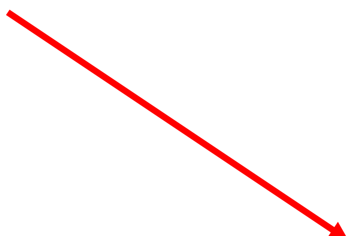
Use LGAD Test beam data: CFD vs LE/TOT

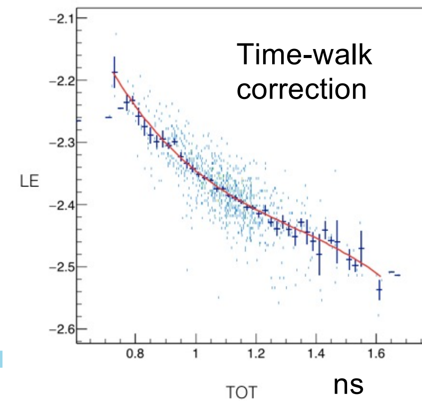
CONSTANT FRACTION VS. LEADING EDGE

Careful study has shown that there is no obvious advantage of using CFD over LE+TOT.

Given that CFD implementation is more involved, the LE+TOT approach is chosen



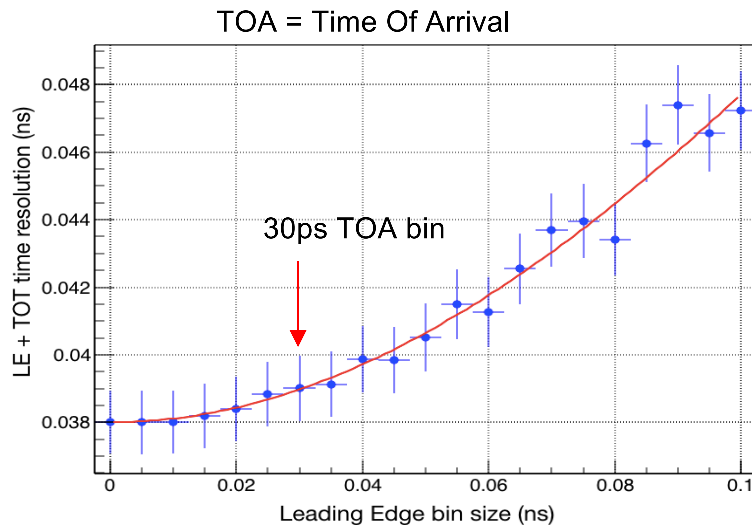


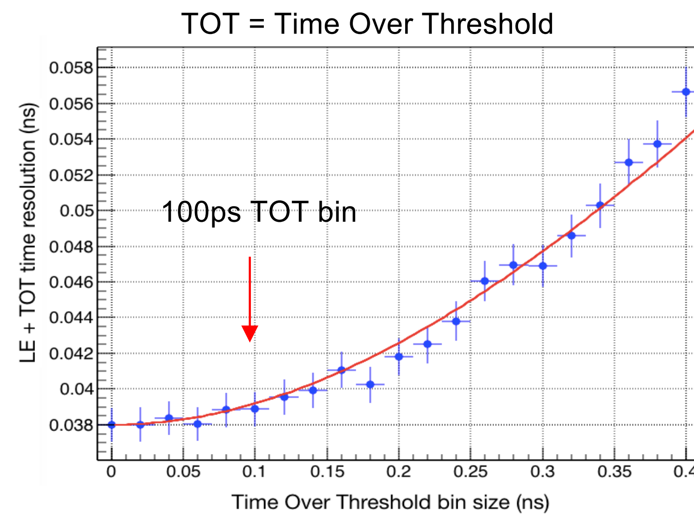


sensor type	CFD	LE+TOT
FBK W6 pre-irradiated	28 ps	30 ps
FBK W6 8.0×10^{14} n/cm^2	30 ps	32 ps
FBK W6 1.5×10^{15} n/cm^2	42 ps	40 ps

Use LGAD Test beam data: TOA/TOT bin

what is the coarsest quantization without affecting the final time resolution of the LE+TOT?





A quantization bin size of up to ~30ps for LE (TOA) and ~100ps for TOT are good enough

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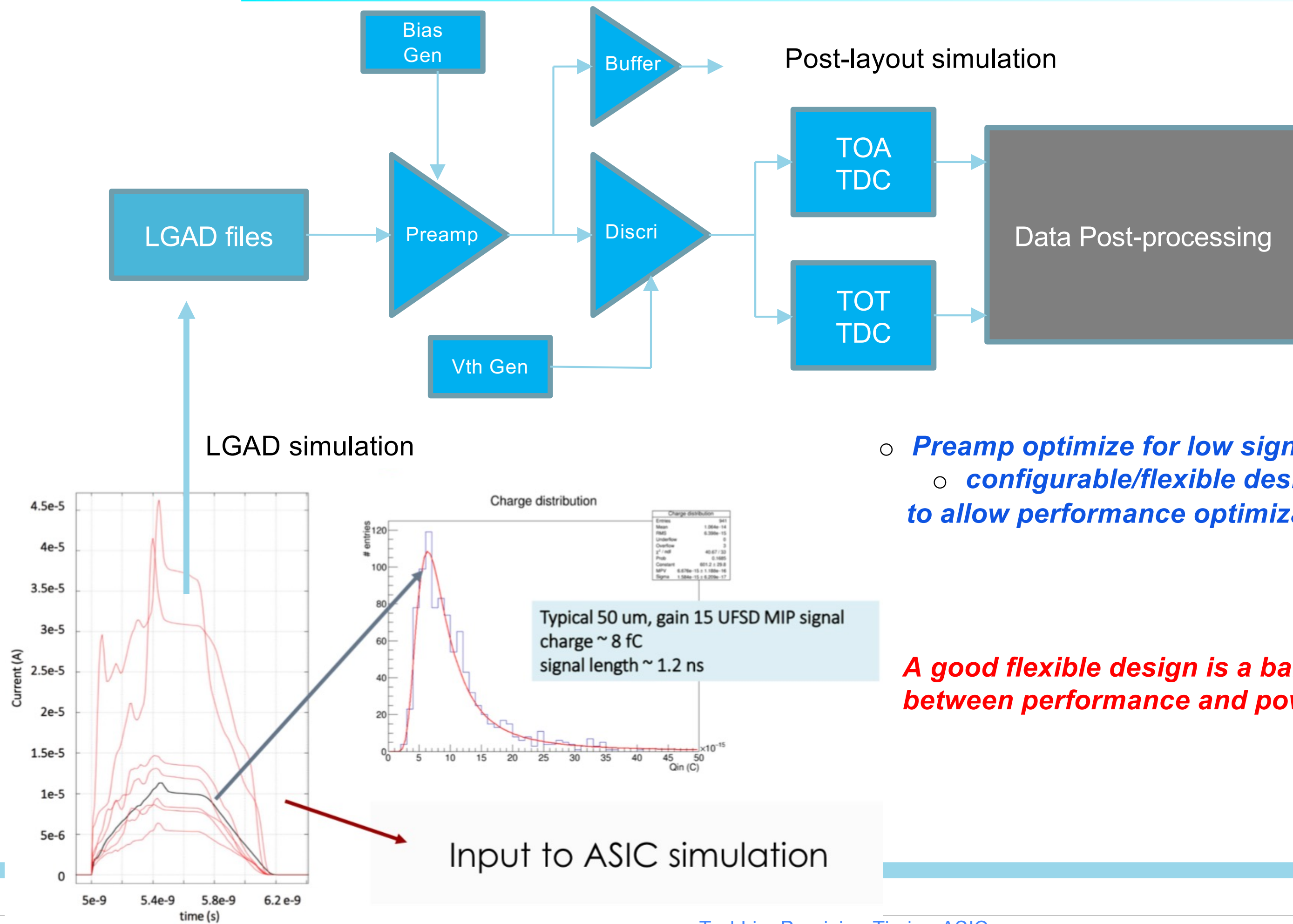
Optimizing the front-end design



- *Preamp optimize for low signal size*
  - *configurable/flexible design*

to allow performance optimization

A good flexible design is a balance between performance and power.

New ETROC TDC Design

For details: see TDC paper
https://ieeexplore.ieee.org/document/9446843

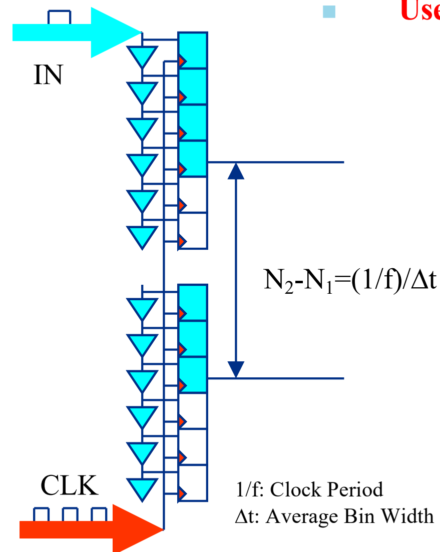
- TDC requirements
  - TOA bin < ~30ps, TOT bin < ~100ps ***(achieved: ~18 ps TOA bin, ~36ps TOT bin)***
  - Lower power highly desirable
    - ***ETROC TDC design goal: < 0.2mW per pixel (achieved 0.1mW)***
- ETROC TDC design optimized for low power
  - A simple delay line without the need for DLL's to control individual delay cells, with a cyclic structure to reduce the number of delay cells, to measure TOA & TOT at the same time
- ***In-situ delay cell self-calibration technique***
  - For each hit, will use two consecutive rising clock edges to record two time stamps, with a time difference of the known 320 MHz clock period: 3.125ns
  - Important to reach the required precision using a tapped delay line with uncontrolled delay cells (thus lower power)

This simple new TDC design choice was a bold move, many experts were very skeptical initially (developed in 2019, very first version works well and no modification needed)

ETROC TDC Self-Calibration: Twice-Recording Method

Double Time Stamping: very simple and effective

- **Each hit registered twice at two consecutive clock edges**
- **Use known clock period for "on the fly" self-calibration of delay line**



The two measurements can be used:

- to calibrate the delay.
- to reduce digitization errors.

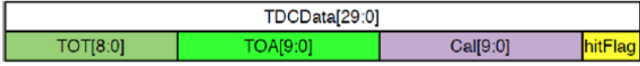
CAL = N2 – N1
TOA bin = 3.125ns / CAL
(this is the bin calibration for every hit)

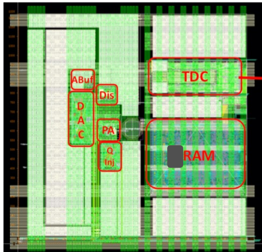
Animation by Jin-yuan Wu (FNAL EE Engineer)

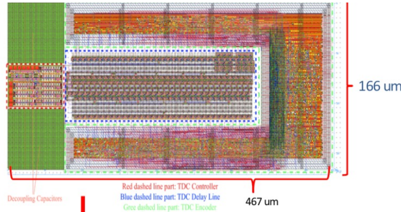
ETROC TDC

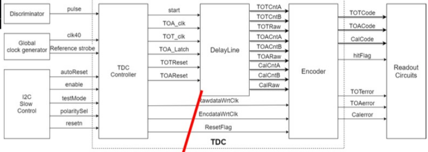
1984 IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 68, NO. 8, AUGUST 2021

A Low-Power Time-to-Digital Converter for the CMS Endcap Timing Layer (ETL) Upgrade









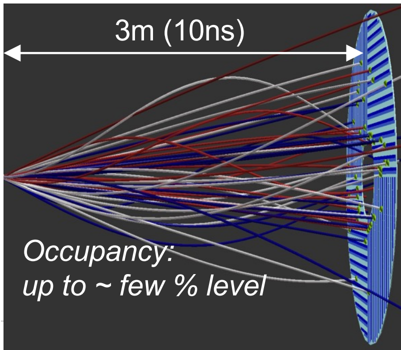
hitFlag: discriminator is fired or not

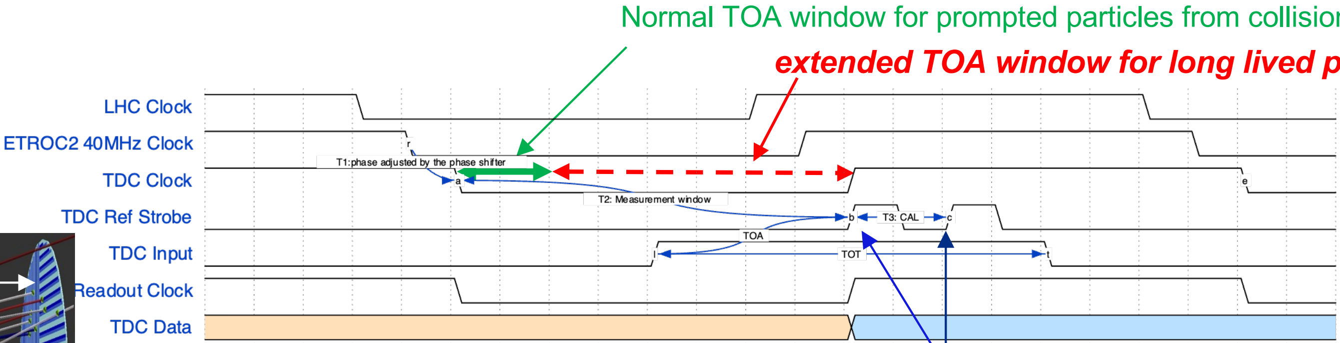
- bin= T3/Cal_code
- TOA=12.5 - bin*TOA_code

T3 is programable with 3.125 ns by default.

Normal TOA window for prompted particles from collisions

extended TOA window for long lived particles





Double time-stamps for self-calibration "on the fly", to calibrate TDC bin size in real time for every hit (very important feature of this TDC design)

https://ieeexplore.ieee.org/document/9446843

Less sensitive to temperature changes, IR drops, radiation etc…

Design considerations for precision timing detector

- System power and cooling constraint and how it influences ASIC design
- Design methodology to optimize front-end from system point of view
- Single layer detector vs multi-layer (ETL design: 1 layer → 2 layer)
- TDC design choice: very low power required → new design
- Precision clock distribution considerations: from system to detector, to chip, to pixel and to each TDC delay unit (using H-tree approach)
- Design to enhance physics reach:
  - such as detection/trigger for long live particles, with wide TDC window
- Design for testability, monitoring and calibration considerations:
  - Internal charge injection, pattern generator within each pixel
  - Internal automatic threshold calibration (noise width) within each pixel
  - Internal waveform sampler (one per chip)
  - FPGA emulator
- ***…***

Proper System Design is the Key to the success of any challenging ASIC project

A good design is a compromise between system design and ASIC design

Our approach: "ASIC == A System design Including a Chip"

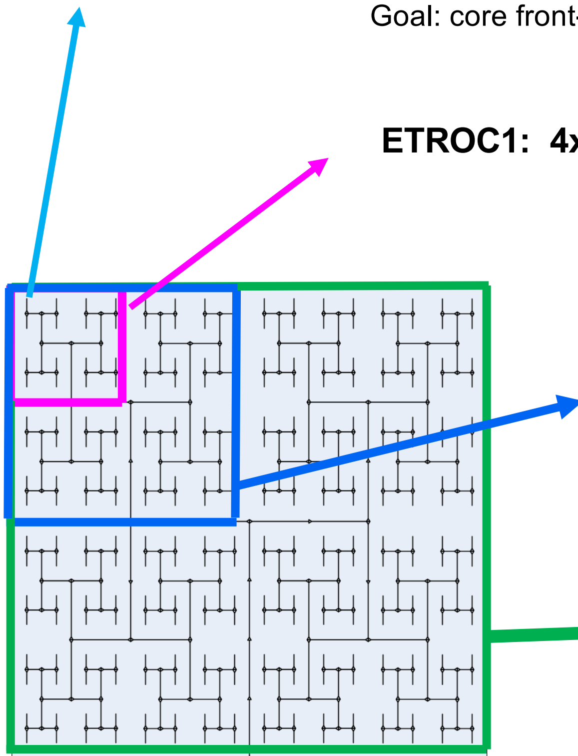
ETROC Development: ***divide & conquer***

ETROC0: 1x1 pixel channel with preamp + discriminator (submitted Dec 2018)

Goal: core front-end analog performance

ETROC1: 4x4 clock tree, preamp + discriminator + TDC (submitted Aug 2019)

Goal: full chain front-end with TDC, 4x4 clock tree
This is the first full chain precision timing prototype



ETROC2: 8x8, *full functionality*, and ¼ clock tree (Q1 2021)

Goal: supporting circuitries, 8x8 clock tree
PLL, phase shifter, fast/slow control, I/O, L1 buffer…

ETROC3: 16x16 (full size): (Q1 2022)

Goal: full size with full clock tree

16 x 16 clock H-Tree

A series of increasingly complex prototype chips: ETROC0 through ETROC3.

ETROC development history (started in June 2018)

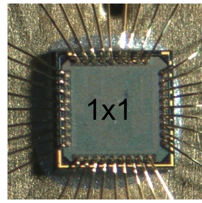
- June-Aug 2018: initial design study
- ETROC0 (front-end design: preamp and discriminator) started in Sept 2018 and submitted Dec 2018
  - First version works well, achieved ~30ps in beam test and passed 100MRad TID
    - Directly used in ETROC1 and ETROC2 without modifications
- ETROC conceptual design (CMS MTD TDR) submitted summer 2019
- ETROC1(4x4) submitted Aug 2019, with brand new low power TDC and 4x4 clock H-tree
  - First version works well without sensor, TDC has ~6ps resolution
  - LGAD-ETROC1 encountered 40MHz digital noise, still observed ~40ps time resolution in beam
    - *Provided the most important guidance for ETROC2 design: to* ***minimize the 40MHz digital noise***
  - Front-end and new TDC are directly used in ETROC2 without modifications
- ETROC2 (8x8 → 16x16) development started in 2020: ***skipped 8x8 stage, went to 16x16 full size/functionality***
  - March 2020: first ETROC waveform sampler submitted and works well
  - May 2020: ETROC PLL chip submitted and works well (collaboration with lpGBT team)
  - July 2020: ETROC I2C chip submitted and works well
  - Sept 2020: ETROC rad-hard waveform sampler submitted and works well
  - Feb 2022: first ETROC2 emulator ready for system development
  - Sept 2022: ***ETROC2 (full size/functionality) design ready, submission in Oct. 2022***
    - ***All critical analog building blocks have been tested in testing chips***
    - ***The digital building blocks have been emulated in FPGA and tested with the downstream readout***
- ETROC3: aim for submission in 2024 (intended as the final version)
  - Turns out ETROC2 works so well, plan to skip ETROC3

ETROC Early Prototyping Phase

Sept 2018 — Dec 2018 — May 2019 — Aug 2019 — March 2020 — May 2020 — July 2021 — Sept 2021 …

Project started

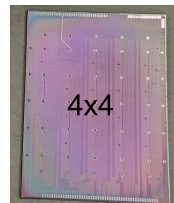
ETROC0 submitted



Preamp + discriminator

ETROC1 submitted

Covid

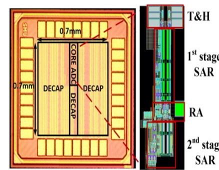


Preamp + discriminator + TDC
4x4 H-tree clock distribution

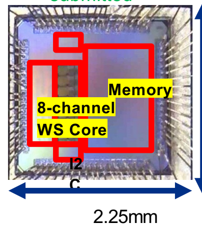
ETROC2: 8x8 → 16x16

Decision to go for full size full functionality ETROC2,
Delay submission and add few test chips …

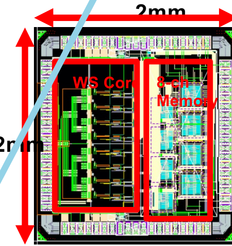
Single channel ADC submitted



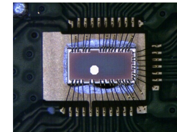
8-channel ADC Waveform Sampler (WS1) submitted



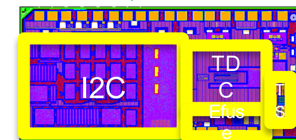
Rad-hard version of Waveform Sampler (WS2) submitted



ETROC-PLL mini ASIC submitted



I2C Test chip submitted



Total of 7 small chips, all successful

All analog blocks have been silicon proven in test chips;
ETROC2 FPGA emulator: has verified digital readout and system interfaces

ETROC2 was submitted (Oct 21, 2022), testing started in later April 2023

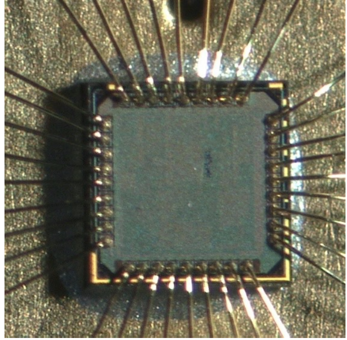
Design team: FNAL/SMU/LBNL/UCSB
Testing team: FNAL/SMU/UIC/UCSB/Lisbon/IFCA/KUL with students from KSU/KU

Most recent ETROC1 paper: https://doi.org/10.1088/1748-0221/19/09/p09019
ETROC2 paper(s) draft in progress

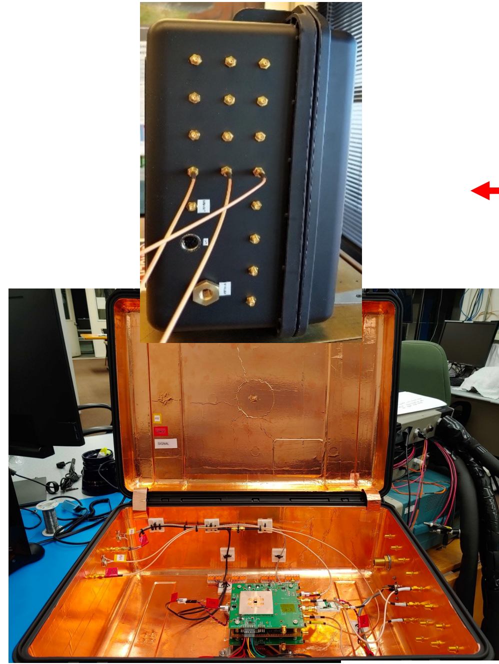
ETROC0 Beam Telescope (with 3 ETROC0 boards) without temp control

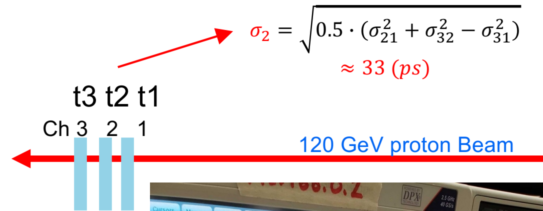
Jan-Feb 2020

Simple "suitcase" setup in parasitic mode running at FNAL Mtest



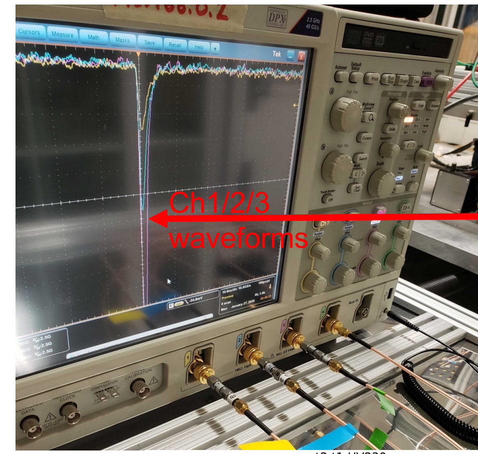
The same preamp + discriminator design is used in ETROC2, without modification





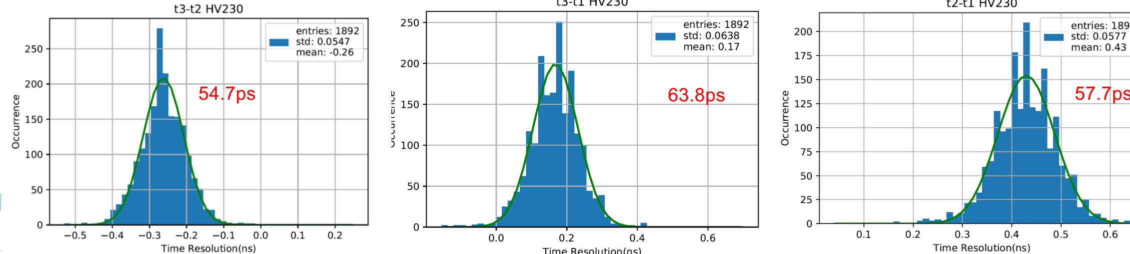
At Room Temperature, without temp control

(~29ps at -20C)



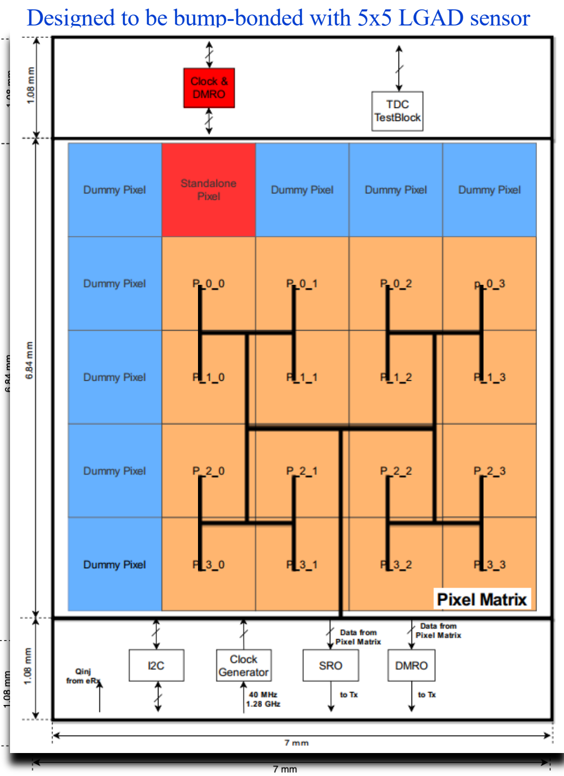
used HPK split 3 (2x2 sensors)

Preamp waveform recorded, offline waveform analysis to determine time resolution



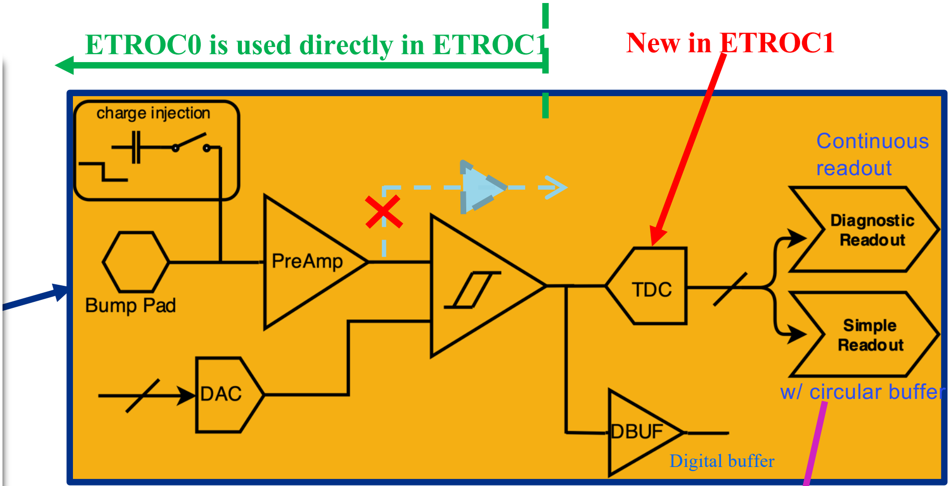
ETROC1: 4x4 pixel array under H-tree clock distribution

Designed to be bump-bonded with 5x5 LGAD sensor



ETROC0 is used directly in ETROC1

New in ETROC1



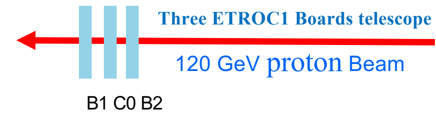
In 4x4 array, the Simple Readout is always enabled;

In Standalone pixel, the Simple Readout block is fully disabled;

Most testing done using continuous Diagnostic Readout mode (for one selected pixel)

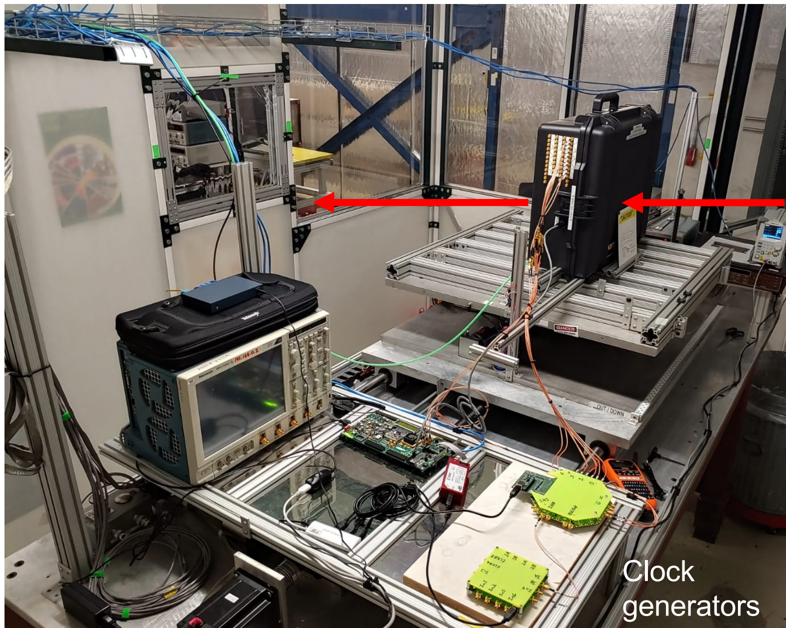
The 4x4 H-tree is designed in such a way to be able to scale up to 16x16 (for ETROC2)

ETROC1 Beam Telescope @ FTBF

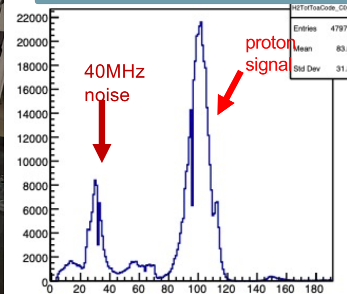


B1 C0 B2

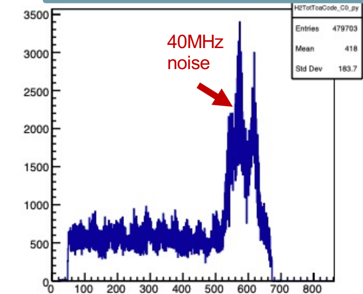
Telescope DAQ:
Triggered on B1
offline confirmed with B2
C0 is Device Under Test



C0 TOT code @HV = 238V



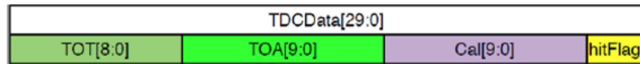
C0 TOA code @HV = 238V

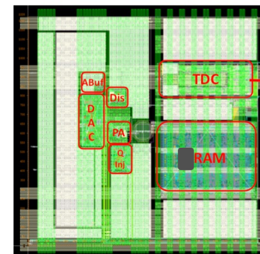


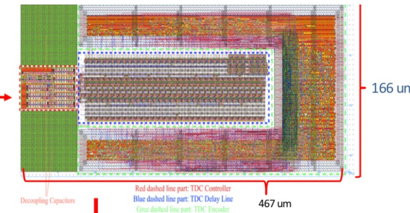
Tevatron machine clock 53MHz
ETROC clock 40MHz

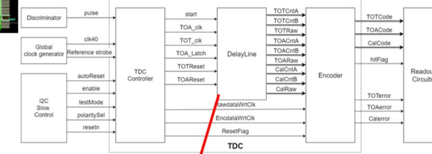
Beam TOA (time of arrival) is flat, and 40MHz noise is not.

TDC operation





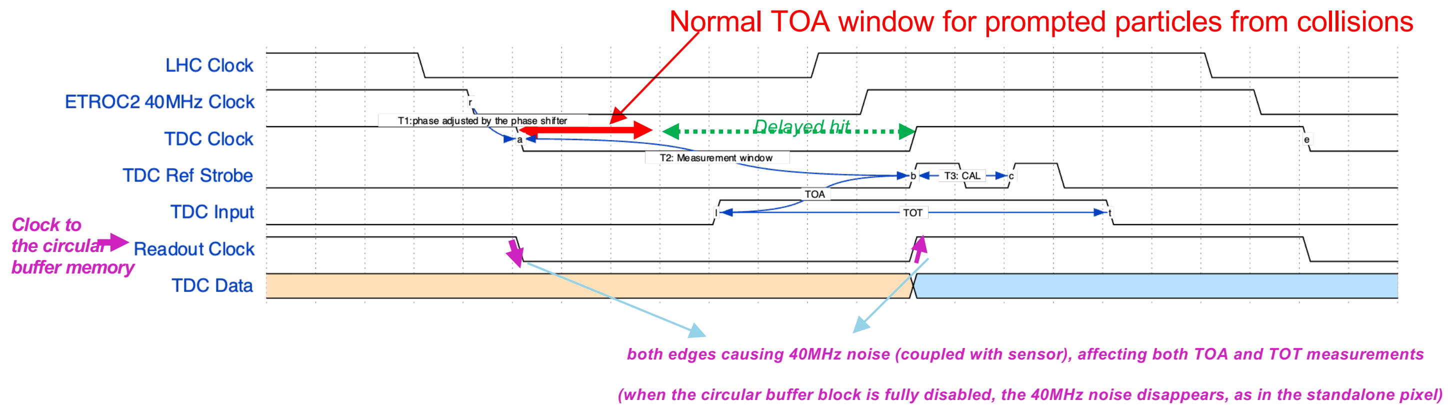




hitFlag: a discriminator is detected in a BX or not

- bin= T3/Cal_code
- TOA=12.5 - bin*TOA_code
- TOT=(TOT_code*2 – floor(TOT_code/32))*bin

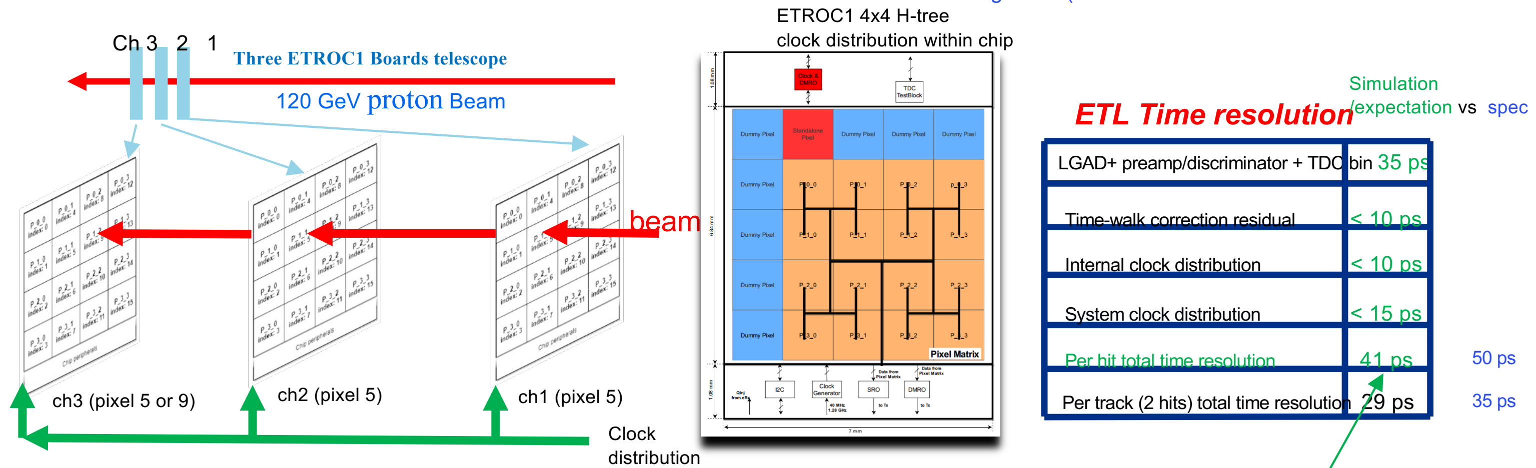
T3 is programable with, 3.125 ns by default.



For beam test, use the TOA and TOT window to stay away from the 40MHz noise

ETROC1 Test Beam results

- Testing team (UIC/SMU/FNAL + students from KSU/KNU/CNU)

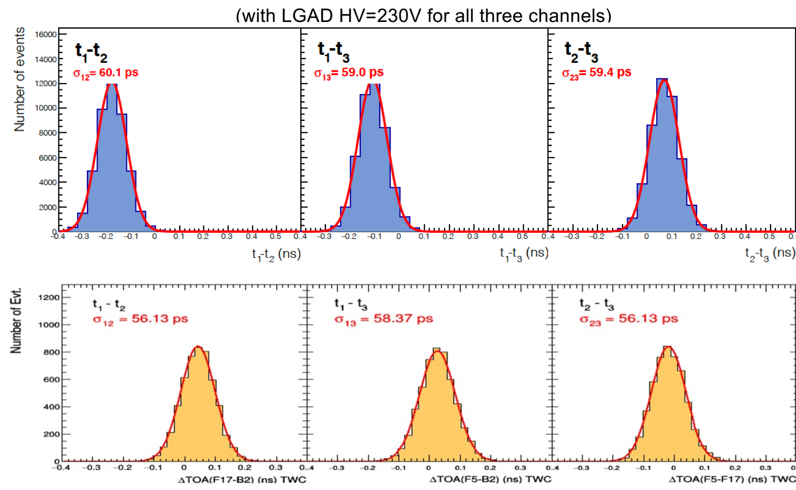


ETL Time resolution

	Simulation /expectation	spec
LGAD+ preamp/discriminator + TDC bin	35 ps	
Time-walk correction residual	< 10 ps	
Internal clock distribution	< 10 ps	
System clock distribution	< 15 ps	
Per hit total time resolution	41 ps	50 ps
Per track (2 hits) total time resolution	29 ps	35 ps

The measured time resolution includes all four contributions in the table

(with LGAD HV=230V for all three channels)



Single-hit timing resolution (ps) with TWC:

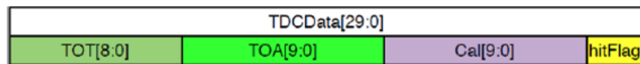
$$\sigma_i = \sqrt{0.5 \cdot (\sigma_{ij}^2 + \sigma_{ik}^2 - \sigma_{jk}^2)}$$

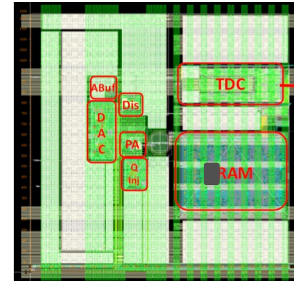
σ_1 σ_2 σ_3 ~ 42.0/42.7/41.3 ps (2021 beam test)

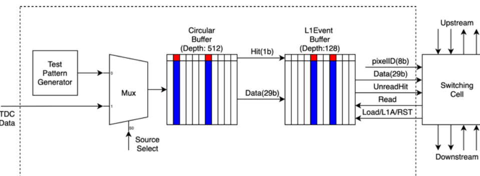
~ 41.3/38.0/41.3 ps (2022 beam test)

Fermilab

ETROC2 pixel readout design: minimize the 40MHz noise

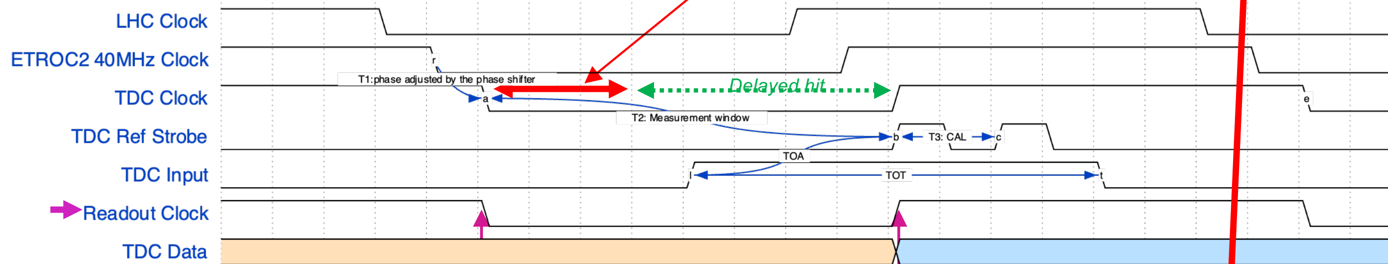






T3 is programable with 3.125 ns by default.

Normal TOA window for prompted particles from collisions



Minimizing the clocking activity (on average) to reduce the 40MHz noise: clock gating and address gating
pixel readout power consumption is x10 lower than that of ETROC1 (per pixel)

Main lesson learned from ETROC1 for ETROC2

- Main lesson learned from ETROC1
  - ***40MHz clocking activity of circular buffer memory causes noise*** through coupling with sensor
    - Bare ETROC1 (without senor) does not have this issue
    - Standalone pixel (with sensor bump bonded) does not have this issue (no circular buffer memory)
    - With somewhat higher threshold (to avoid the noise), and proper TOA/TOT windows,
      good time resolution has been obtained from test beam data for the 4x4 array pixels (~40 ps).
      - ***This agrees with expectation/simulation***
- ETROC2 design to address the 40 MHz noise issue: ***minimize it at its source***
  - *Circular buffer memory clock (and address line) gated based on hit*, only on for valid TDC hit
  - ETROC2 pixel readout power consumption is optimized to be x10 lower than that of ETROC1
  - The clocks are offset to avoid "marching in sync" (clock tree shielded)
  - *Shielding layer at the top* of ETROC2 (from sensor)
  - *Separated 40MHz clock for readout* (vs TDC clock) with adjustable phase\
  - …

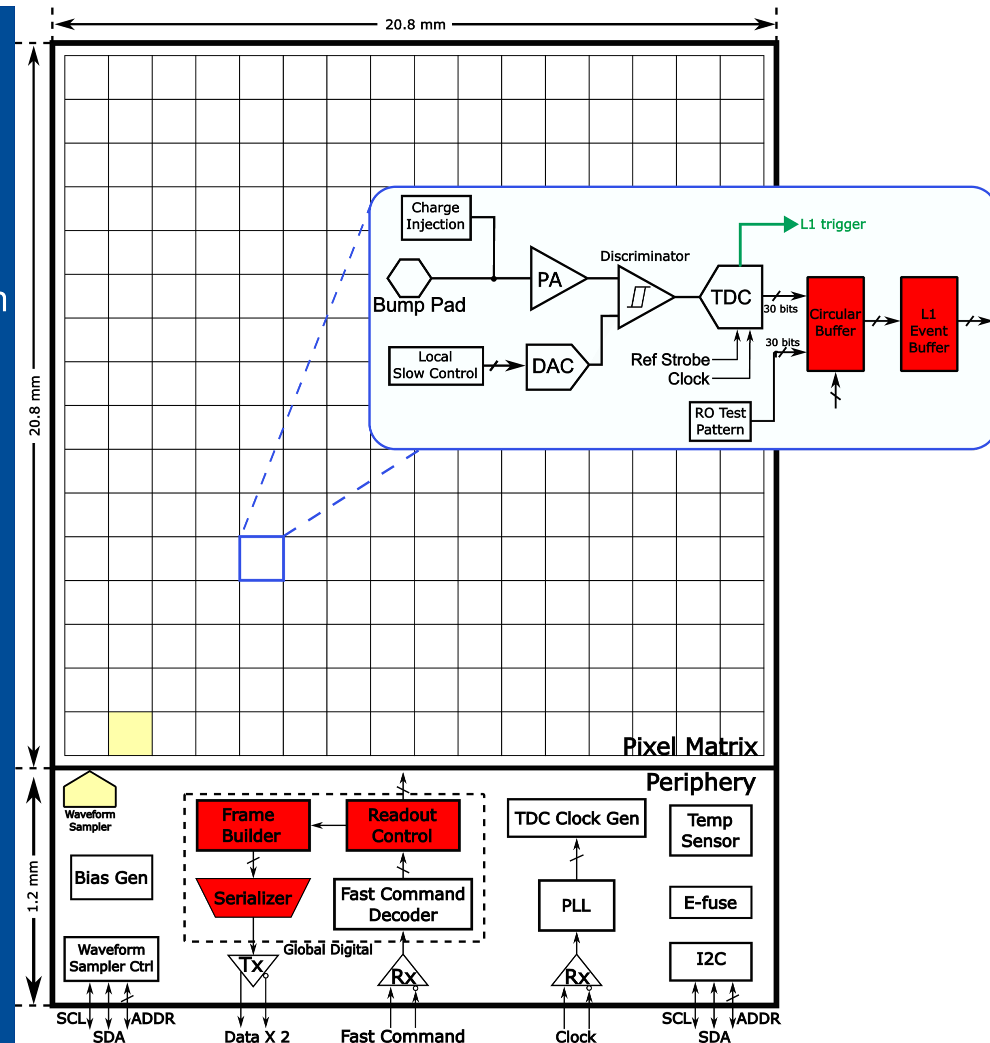
Bottom line:

ETROC2 front-end and TDC are the same as in ETROC1 (excellent performance)
ETROC2 have brand new readout design optimized to minimize the 40MHz noise
ETROC2 16x16 clock H-tree is scaled up from ETROC1 4x4 H-tree (excellent performance)

ETROC2 overall design

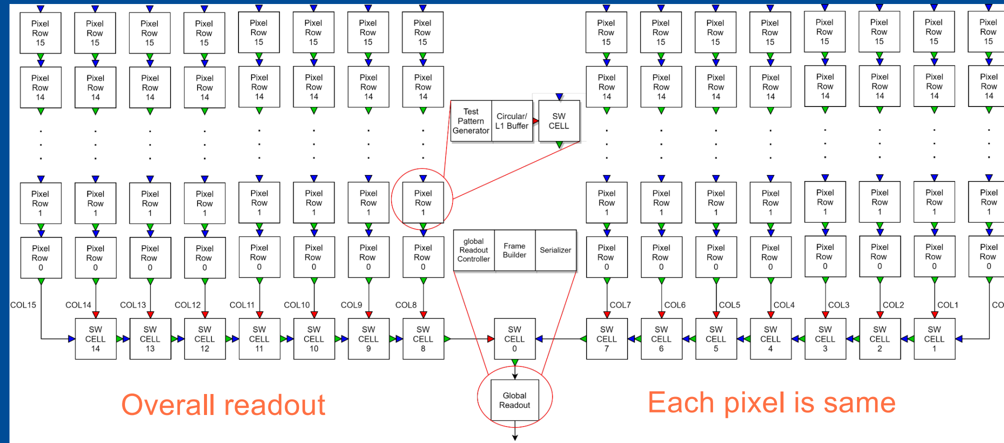
- Measuring TOA, timing walk correction with TOT
  - Front-end: PA + Discriminator + TDC
  - L1 trigger-driven readout with zero suppression
  - L1A-driven readout with zero suppression
  - A coarse map of hits for L1 trigger, monitoring or luminosity
- Interface: 40 MHz clock, I2C, fast control, serial data output at 320/640/1280 Mbps
- Fast waveform sampling for one pixel
- TSMC 65 nm CMOS process
- Power: **1 Watt/chip** @ 1.2V
- 100 MRad TID tolerance, **SEE protection**

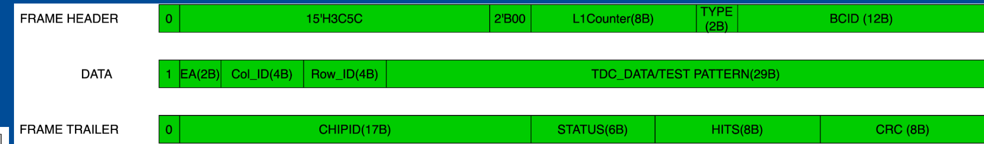
ETROC2 is the first full-size prototype, with full functionalities, designed as if it is the final design.



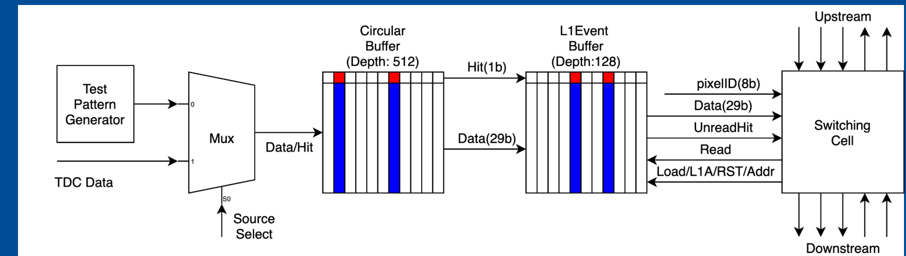
Fermilab

ETROC Readout design

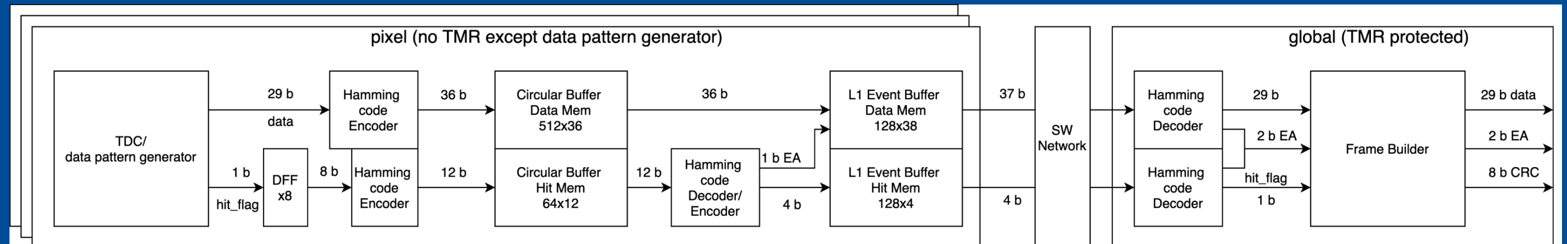




ETROC data Frame

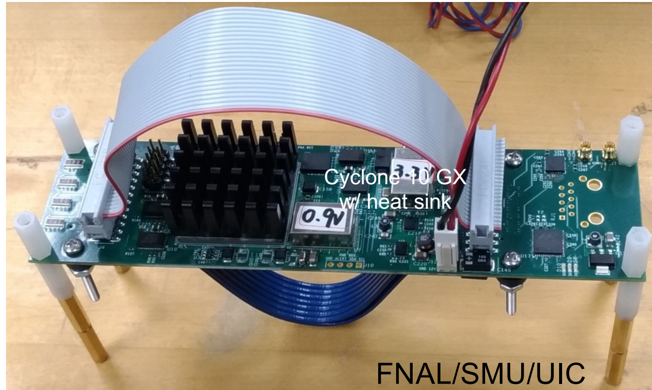


Pixel readout



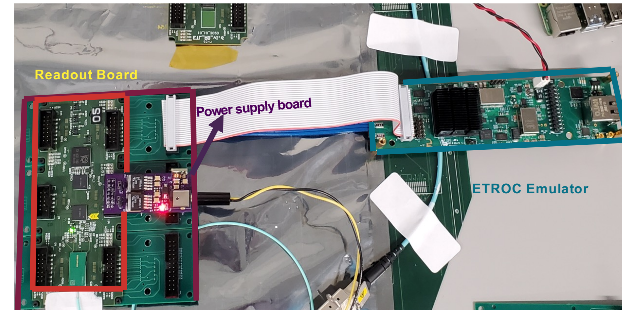
- All readout control signals are coordinated within the global readout, which is TMR protected.
- TDC data is read out through a switching network to the global readout; No TMR needed in the pixel readout.
- TDC data is protected by error correction using Hamming code from CB to the frame builder.

ETROC2 emulator testing with the Readout Board prototype
→ to verify ETROC design with system before submission of ETROC2 design



The emulator has been successfully tested with the Readout board

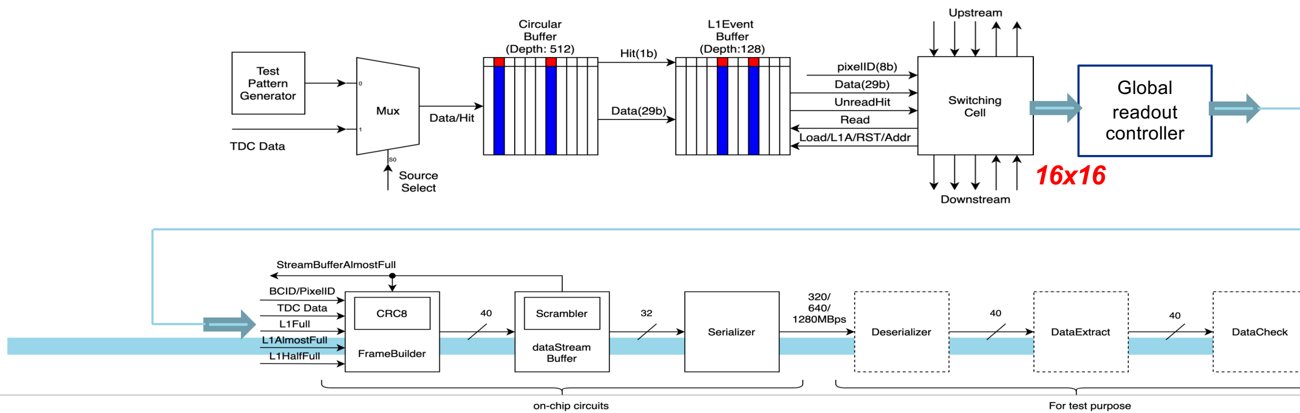
ETROC2 emulator was used at FNAL/BU/CERN/RICE

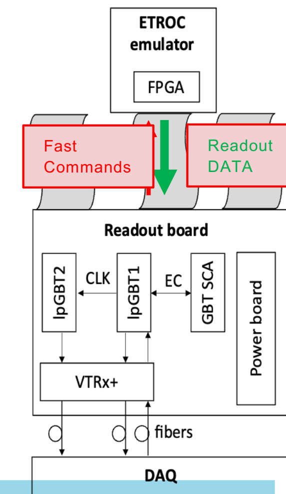


System level testing setup at BU

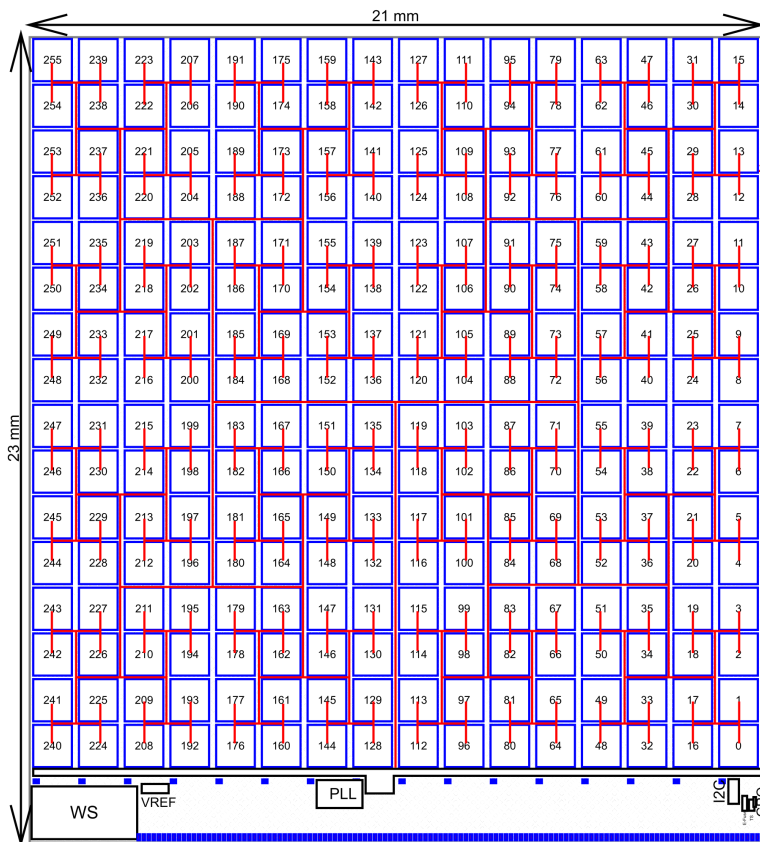
The ETROC2 FPGA emulator has been very useful during the design stage

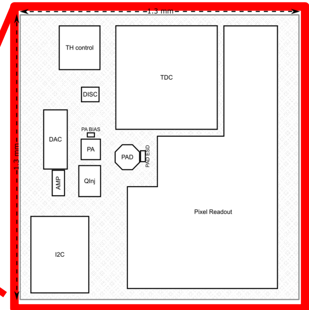
The ETROC2 emulator can emulate the entire ETROC2 digital processing chain using internal test patterns





ETROC2 design with H-tree clock distribution

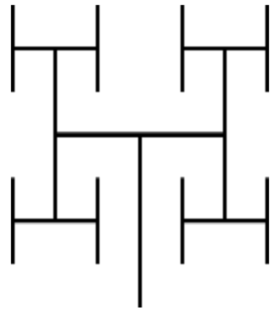




Charge injection/DAC
Preamp,
Discriminator
TDC

All tested in ETROC0/1, and reused in ETROC2

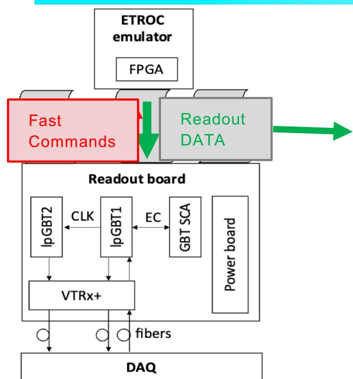
- PLL
  - PLL is based on lpGBT and validated with PLL test chip (+SEU)
- H-tree distribution tested in ETROC1
- I2C
  - I2C design validated with I2C test chip, including SEU
- TS (Temp Sensor)
  - TS validated with I2C test chip
- Efuse
  - Efuse validated with I2C test chip
- VREF
  - VREF validated with I2C test chip
- GRO
  - Reusing the GRO in ETROC1
- Tx and Rx
  - Validated in ETROC1
- WS (Waveform Sampler)
  - tested and works well
- In-pixel threshold calibration
  - tested with ETROC0 via FPGA emulator



H-tree clock distribution tested in ETROC1

All critical analog building blocks have been silicon proven, mostly tested for irradiation except TDC (design followed rad-hard practice from lpGBT), and the digital building blocks have been emulated in FPGA and tested with the downstream readout board with backend before submission

ETROC2 data output frame



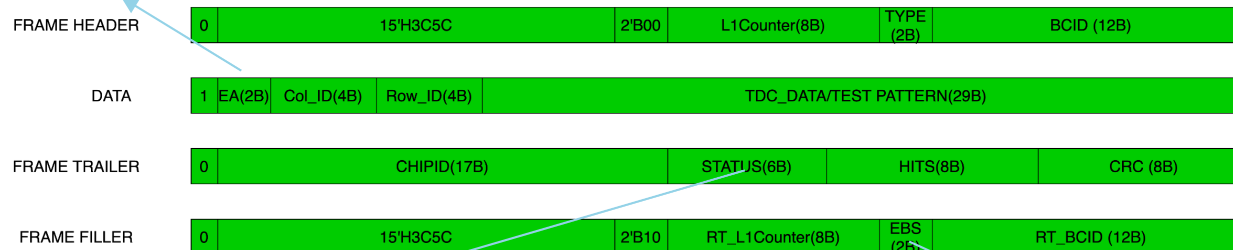
- Composes of a header, variable hit words, and a trailer.
- When there is no L1A, a filler is sent.
- Each header, data words, trailer, or filler has 40 bits.

Emulator data has been correctly received by readout board (v1) and properly unpacked for all 16x16 pixel arrays.

This was done before ETROC2 submission.

Type		meaning
0	0	regular data
0	1	random test pattern
1	0	counter test pattern
1	1	reserved

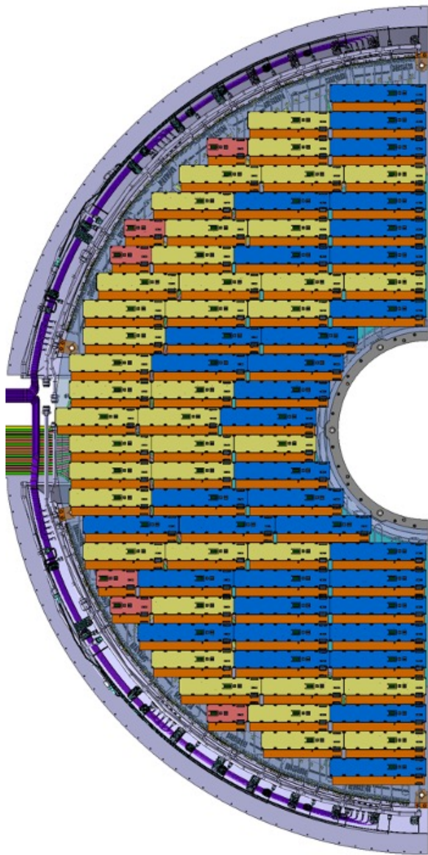
EA		meaning
0	0	no error
0	1	single bit error, but corrected
1	0	two or more bit error and no correction
1	1	Reserved

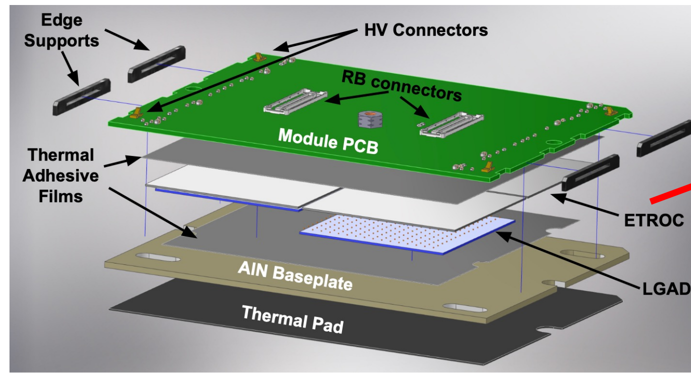


Status						meaning
					X	The L1 event buffer is full, and events may be lost
				X		The L1 Event buffer is almost full (# of hits in the buffer >= 96). The threshold can be user defined.
			X			L1 Event buffer half full (# of hits in the buffer is >= 64)
		X				single bit error occurs, but is corrected in least one pixel (OR EA[0] of all hit pixles)
	x					2 or more bits error occurs and is not corrected in least one pixel (OR EA[0] of all hit pixles)
x						reserved

EBS		meaning (2 MSB of the number of hits left in the event buffer)
0	0	Hits in the L1 event buffer is less than 32
0	1	Hits in the L1 event buffer is from 32 to 63
1	0	Hits in the L1 event buffer is from 64 to 95
1	1	Hits in the L1 event buffer is larger than 96

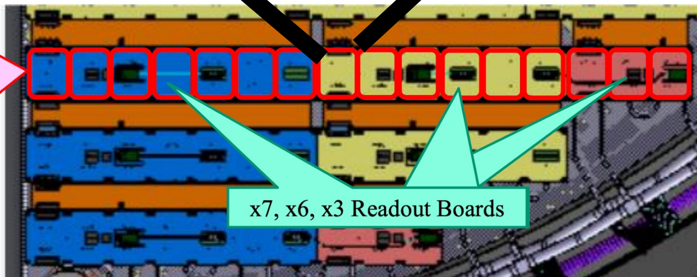
ETL Front-end readout Electronics



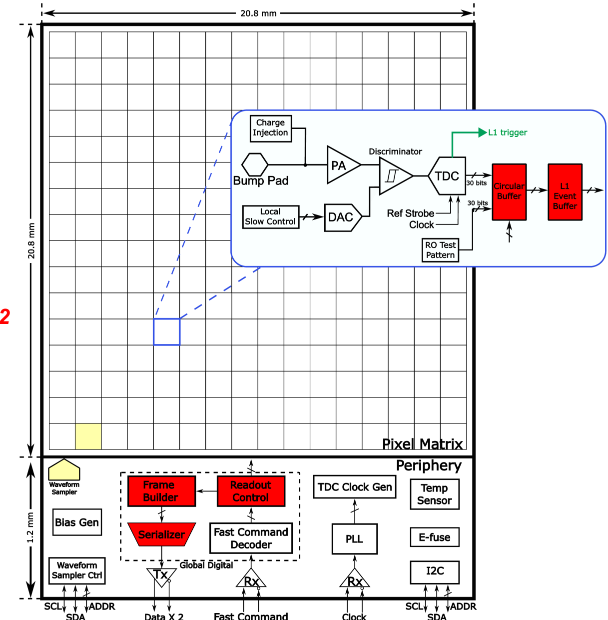


Module

Detector Modules under RBs



ETROC2



All designs have been mature enough to allow us to finalize ETROC2 design

All early prototypes have been mature enough to test the system interfaces with ETROC2 chips
(ETROC2 emulator has helped a lot)

Fermilab

ETROC2 layout (submitted on Oct 21, 2022)

Designed during COVID lockdown, all work done remotely

21 mm x 23mm in size (65nm)

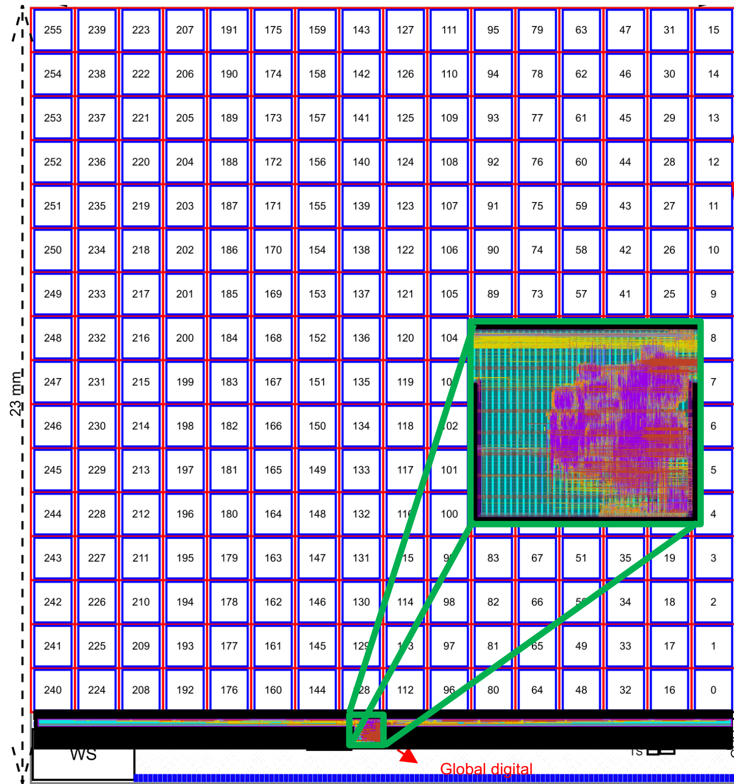
ETROC:
Precision determination of the arrival time of small water drop ripples

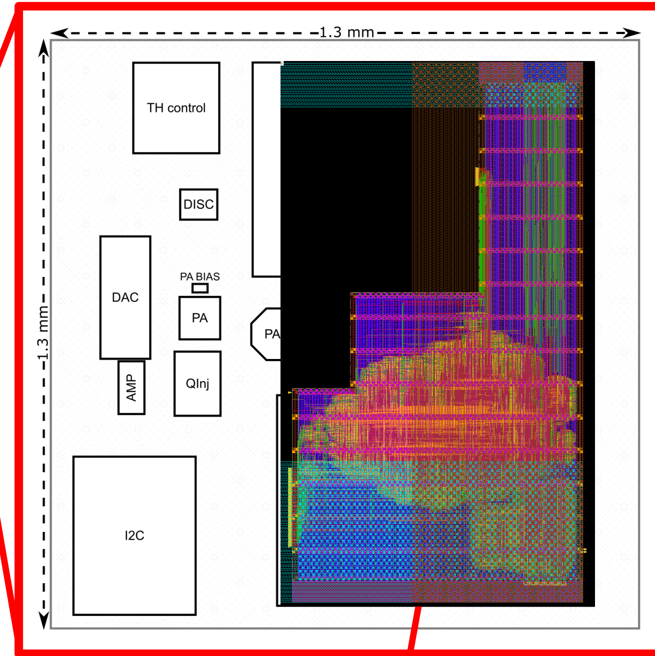
Low noise is the key
Low power is a must
Robust against TID & SEU
….

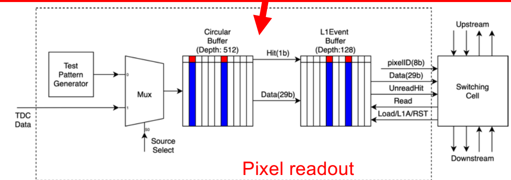
ETROC2 is the first full-size full functionality prototype

ETROC2 pixel and global readout blocks

Major milestone: All building blocks have been integrated together and verified preliminary full-chip DRC and LVS clean (except waveform sampler, being integrated now)



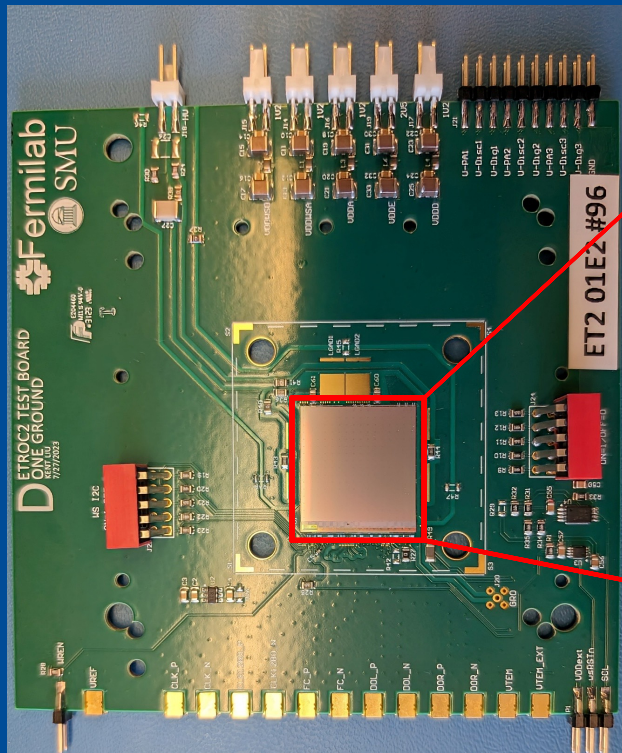


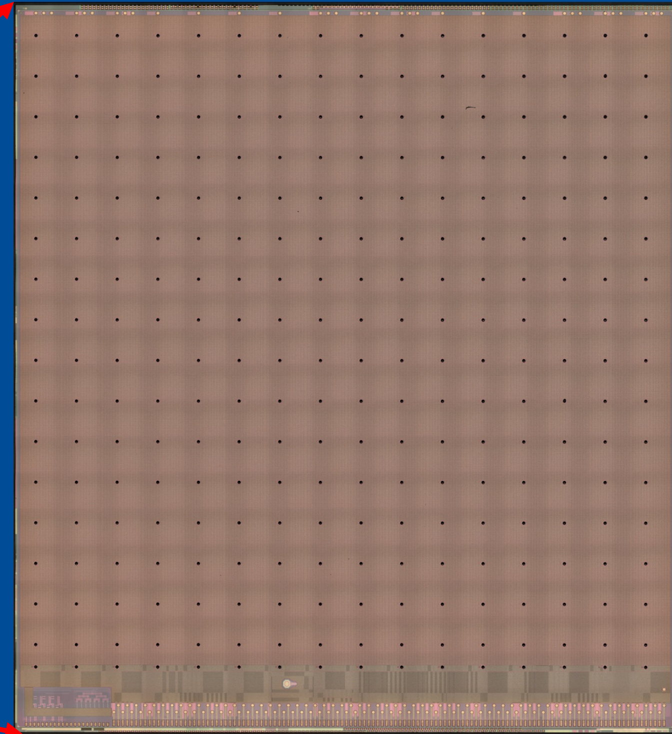


Some of ETROC2 key features: from user point of view

- **Each pixel has a low power high performance TDC, automatically *self-calibrated* for every hit recorded**
  - **Important for precision timing performance and uniformity across 16x16 array**
  - **Has large TOA window (effectively up to 11.4ns), can detect long lived or late arriving particles**
  - Paper: https://ieeexplore.ieee.org/document/9446843
- ***Each pixel has auto-threshold scan capability to quickly determine preAmp baseline and noise width***
  - ***User-friendly, save a lot time for manual calibration during detector operation***
  - Paper: https://iopscience.iop.org/article/10.1088/1748-0221/16/09/T09006
- ***Flexible readout design***
  - user-defined window for TOA, TOT and CAL to filter/suppress hits before readout for each pixel
  - user adjustable TOA measurement window (up to 12.5ns, 11.4ns effective)
  - each pixel can be enabled or disabled for DAQ readout
  - Two outputs for readout, each user configurable for 320/640/1280Mbps bandwidth
- ***L1 Trigger path (for monitoring, luminosity measurements or L1 trigger)***
  - a coarse map (user defined) hits continuously sent out every BC (on the same fiber as DAQ readout)
  - user-defined window for TOA, TOT and CAL for triggered hit, ***can trigger on long lived or delayed particles***
- ***On-chip 2.56 GSPS Waveform Sampler***
  - record waveform for one pixel up to 16 BC (400 ns), start/stop controlled via fast command, readout via I2C
  - power-down when not used, intend for monitoring purpose during detector operation
  - ***ETL has ~ 30k ETROC chips: this means 30k oscilloscope channels available***
  - Paper: IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Volume: 30, Issue: 2, Feb. 2022) Page(s): 123 – 133
- **Charge injection and self-test pattern generator, on-chip PLL (lpGBT), temp sensor, efuse etc**

ETROC2 chip and test board





ETROC2 Testing Road Map

Blue: done
Green: on going
Red: not yet

ETROC2 chips received in late April 2023

ETROC2 chip level testing

- Bare ETROC2 testing
  - Single pixel scan
    - Torture testing
      - ***Wafer probing yield study***
      - ***Temp vs Voltage vs TID to scan operation phase space***
    - TID
    - ***SEU***
- Sensor + ETROC2 testing
  - 2x2 LGAD + ETROC2 wire bonded (prepare for →)
    - ***Charge Injection noise study***
    - **laser**
    - beam
    - cosmic
  - 16x16 LGAD + ETROC2 bump bonded (start testing the first chip in Sept)
    - ***Charge Injection noise study***
    - laser
    - ***beam***
    - **cosmic**

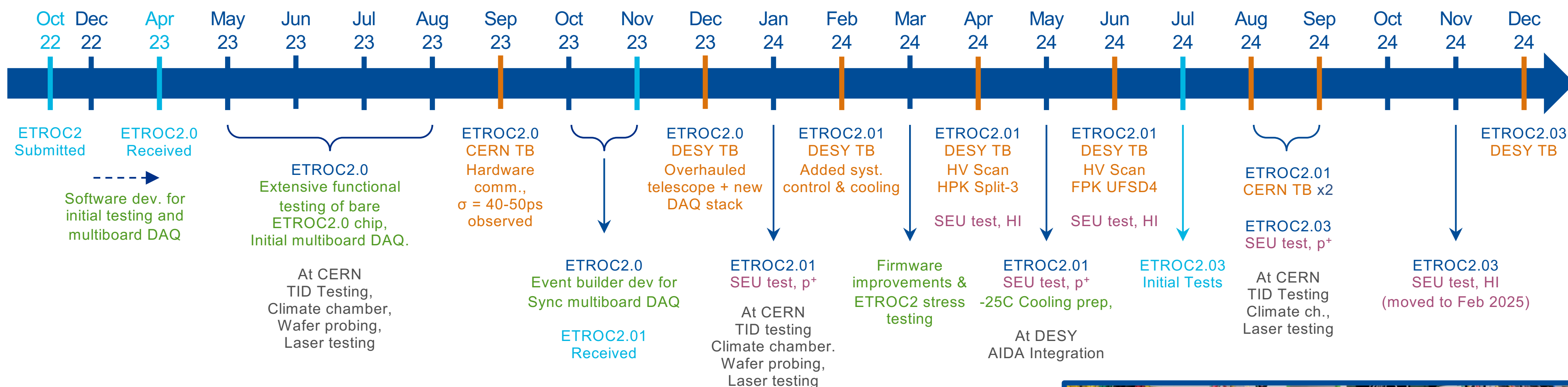
System level testing

- With Bare ETROC2
- With sensors

First round of testing completed for ETROC2.00 and 2.01

ETROC2.00/2.01 have been extensively tested, ETROC2.03 is being tested as if it is the final version

ETROC2 Test Schedule



ETROC2.00 and 2.01 have been extensively tested over the past year
ETROC2.03 testing on going, so far so good (all fixes confirmed successful)

To be done:
testing in cold, with irradiated sensors
Improve SEU test setup for one more round of testing
Improve bump bonding yield

Only a few highlights of the test results in this talk

Bump bonded ETROC2 performance with charge injection

ETL spec is < 50 ps per hit:

LGAD contribution: ~30ps

ASIC contribution:

30ps line

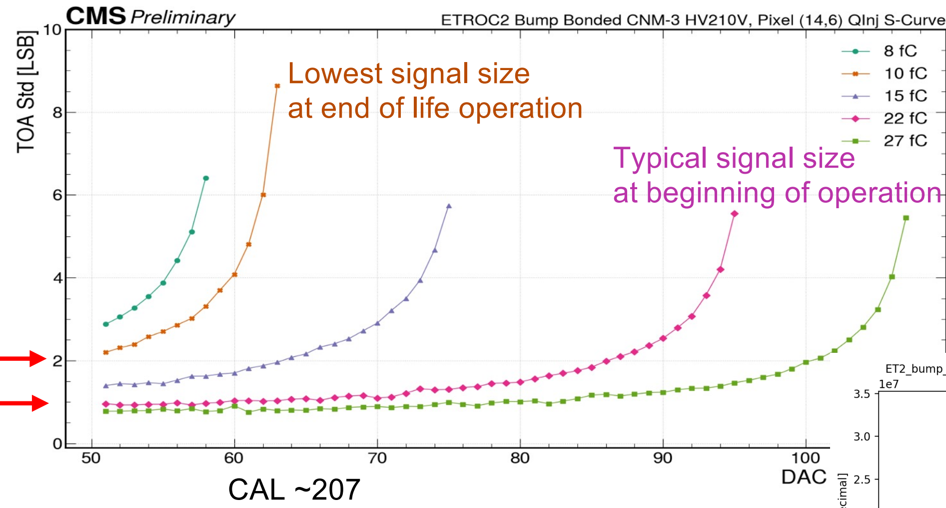
15ps line

From charge injection results, the expected performance with sensor (roughly):

LGAD+ preamp/discriminator + TDC	34 / 42 ps
Time-walk correction residual	< 10 ps
Internal clock distribution	< 10 ps
System clock distribution	< 15 ps
Per hit total time resolution	39 / 47 ps
Per track (2 hits) total time resolution	28 / 33 ps

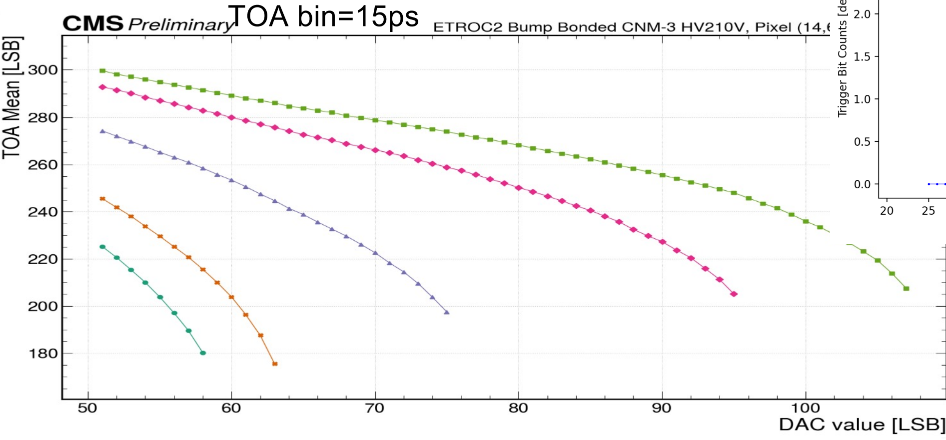
Initial operation: ~39 ps per hit

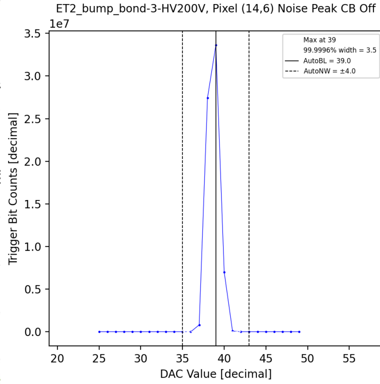
End of life operation: ~47ps per hit



CAL ~207

TOA bin=15ps

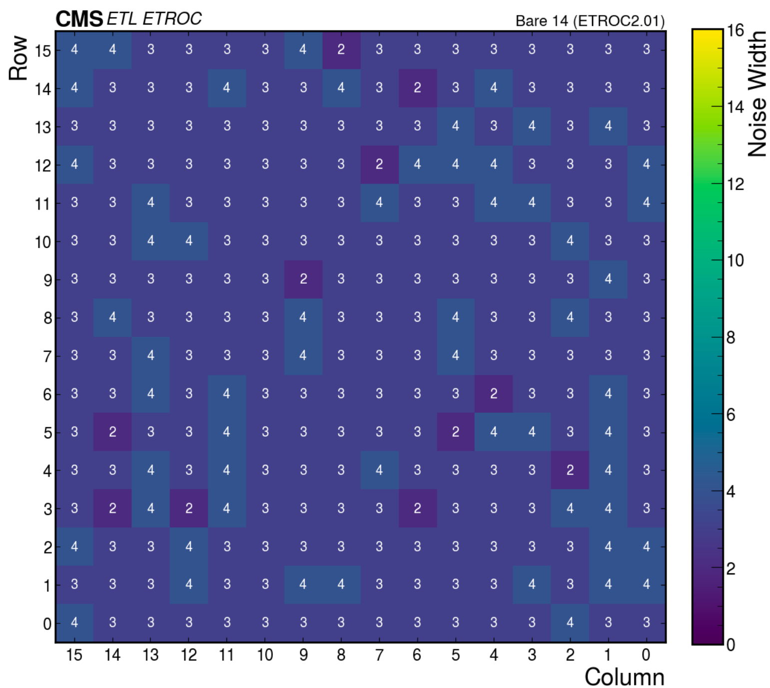




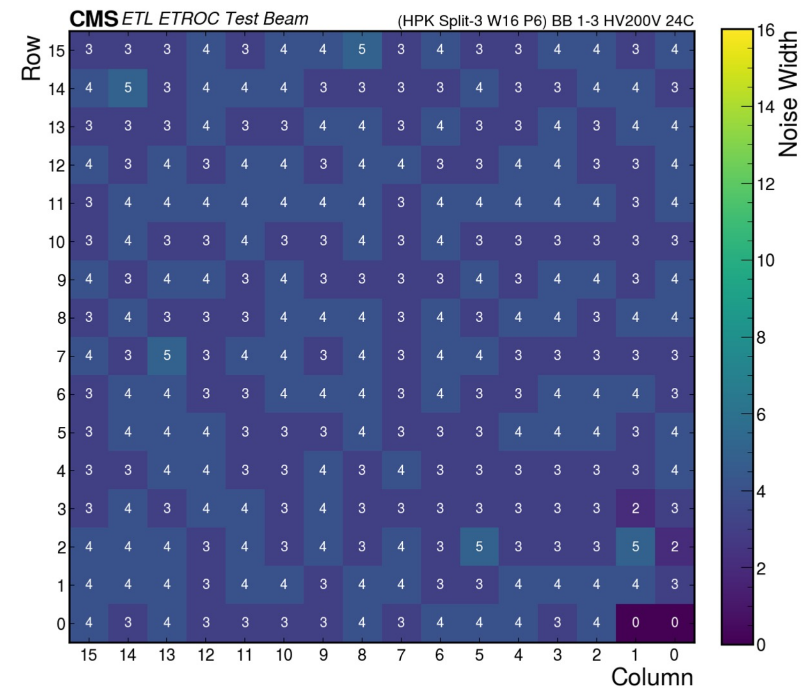
ETROC2 has in-pixel automatic threshold scan capability (through I2C command), to determine the baseline and noise width for each pixel (very fast, to map out 16x16 array), see paper below:

https://iopscience.iop.org/article/10.1088/1748-0221/16/09/T09006

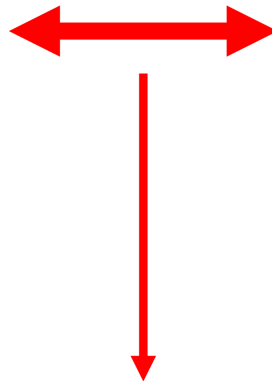
Bare ETROC2 noise width map



Bump bonded ETROC2 noise width map



Look very similar



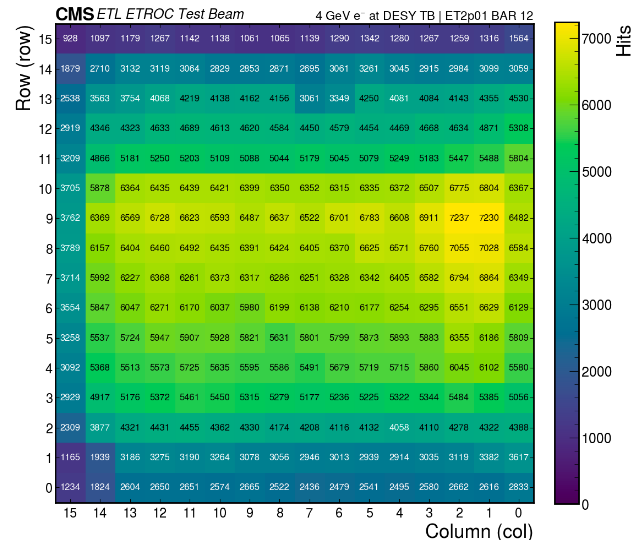
The bump bonded ETROC2 noise is so low that it is NOT easy to tell if a pixel is bump bonded with sensor

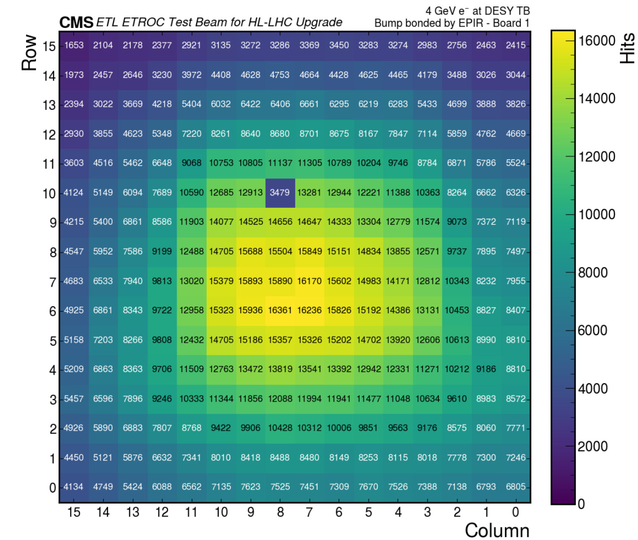
Beam spot (hits occupancy map)
on ETROC2 bump bonded with sensor

All pixels are connected
(100% bump bonding)

Left: done at Barcelona

Right: fully processed by EPIR (sensor/ASIC)



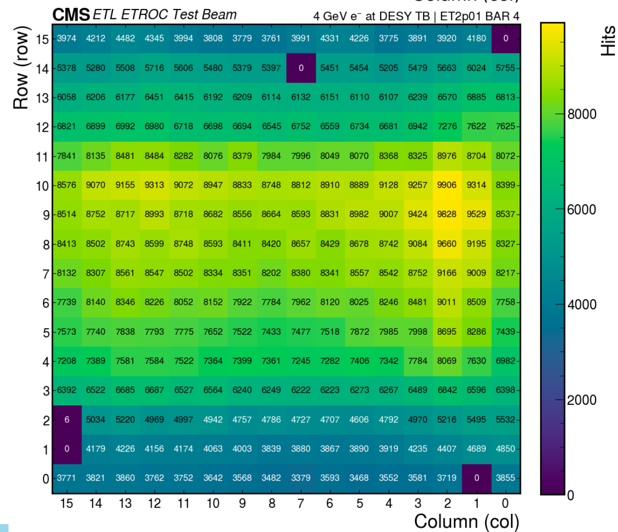


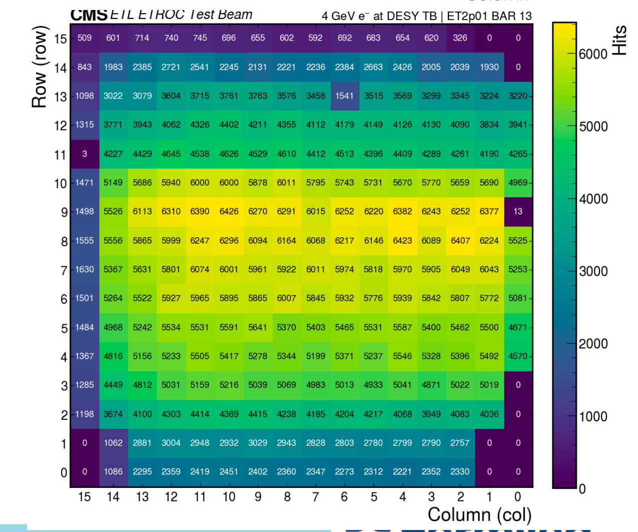
Just some examples used in beam tests

some chips with
pixels not fully connected

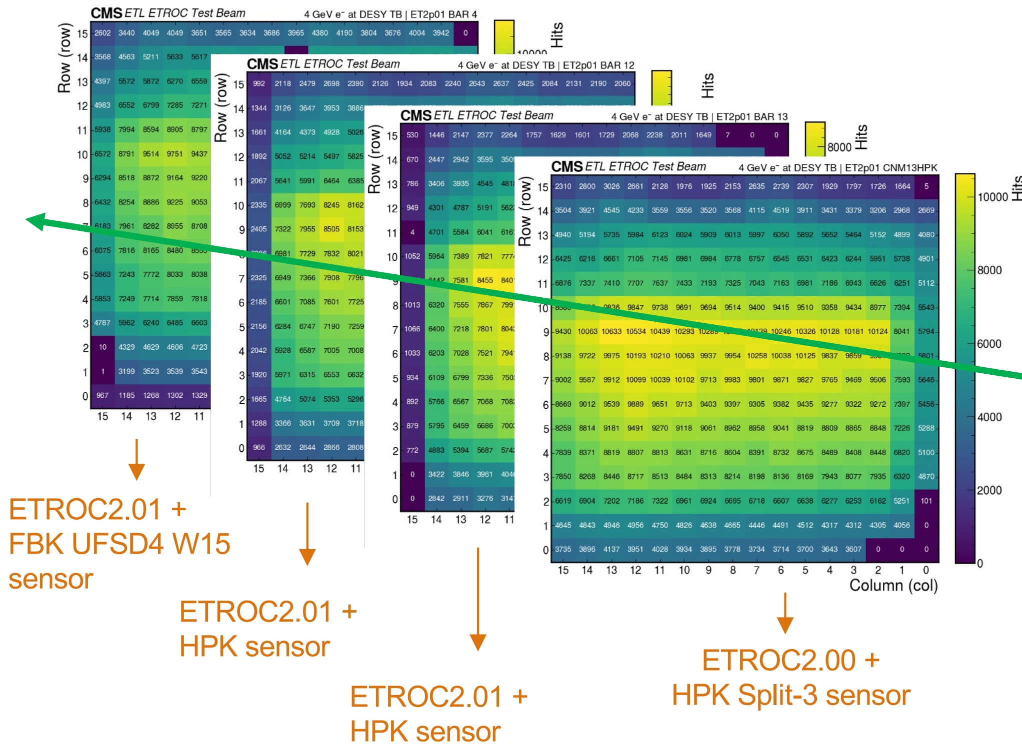
(some poorly connected, not shown here)

Bump bonding yield to be improved





ETROC2 Telescope at DESY Jun 2024



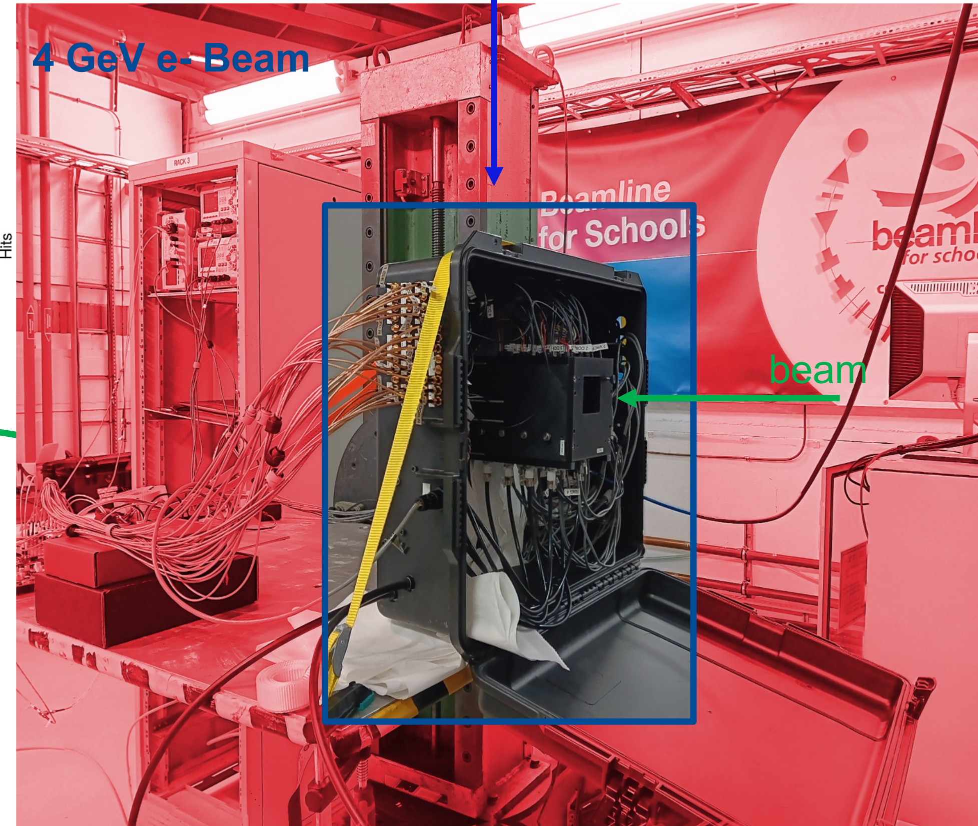
ETROC2.01 + FBK UFSD4 W15 sensor

ETROC2.01 + HPK sensor

ETROC2.01 + HPK sensor

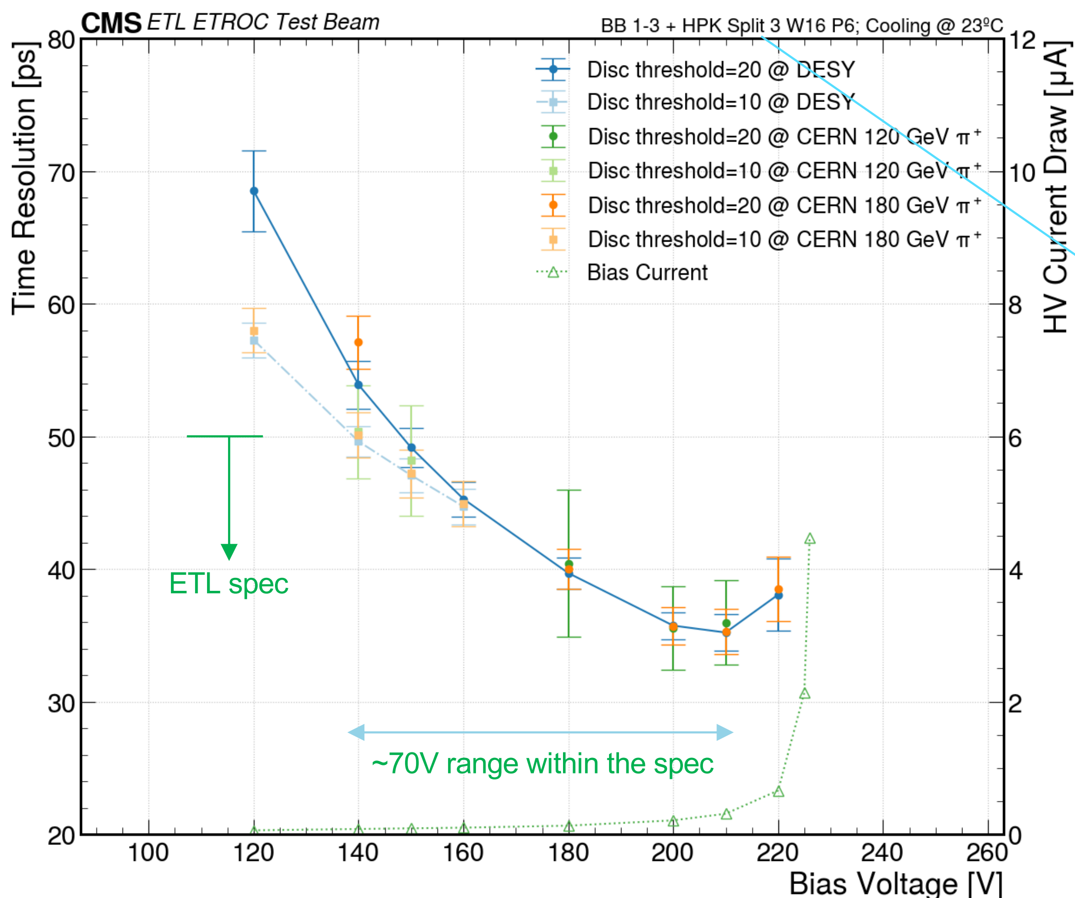
ETROC2.00 + HPK Split-3 sensor

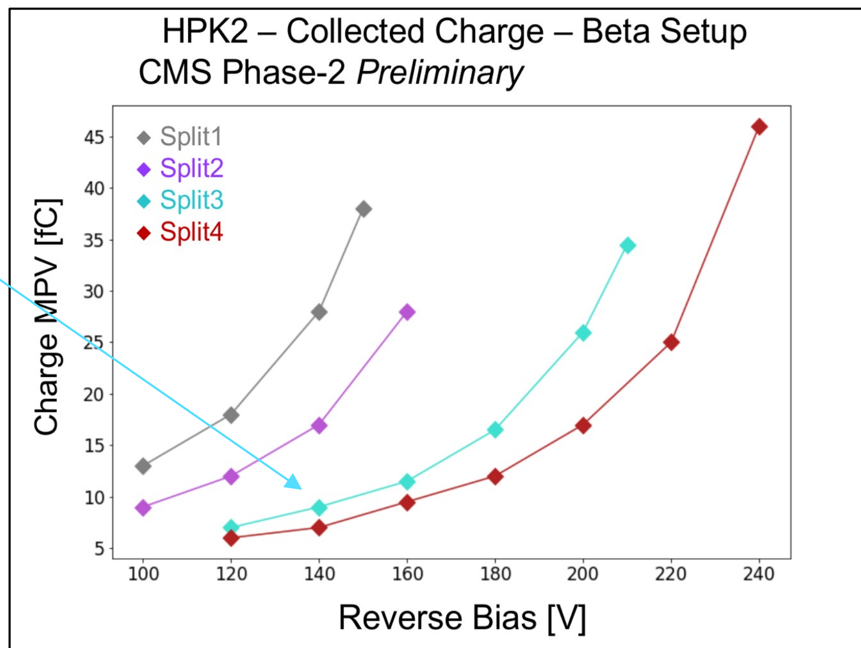
ETROC2 suitcase telescope



Fermilab

ETROC2 beam test at DESY (June) and CERN (Aug and Sep 2024)

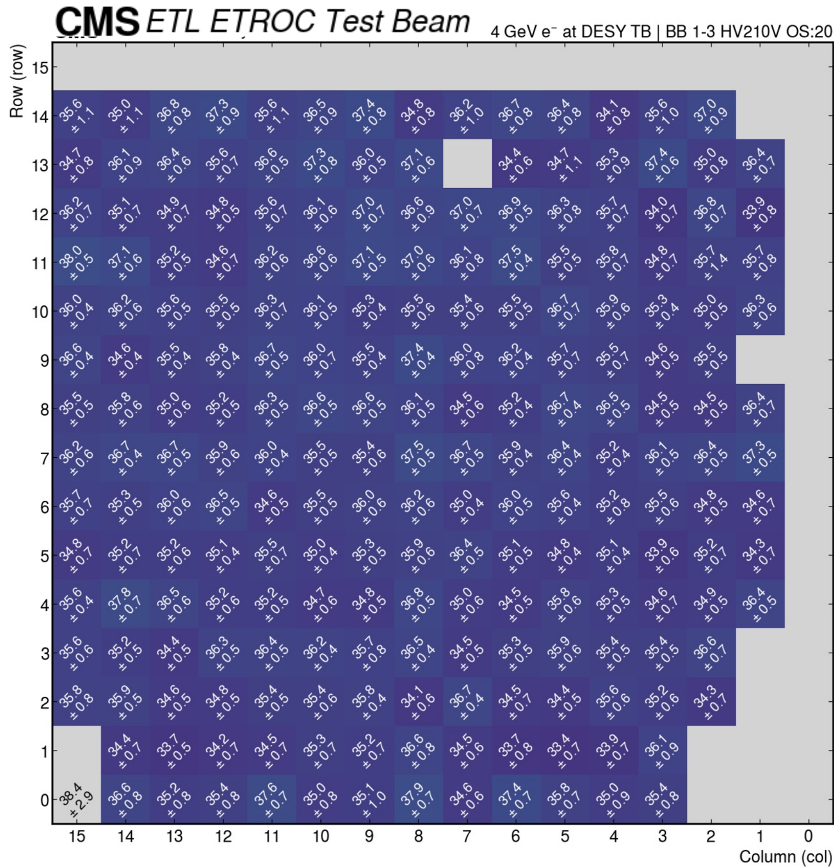


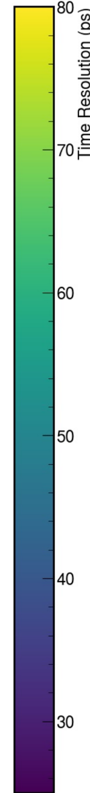


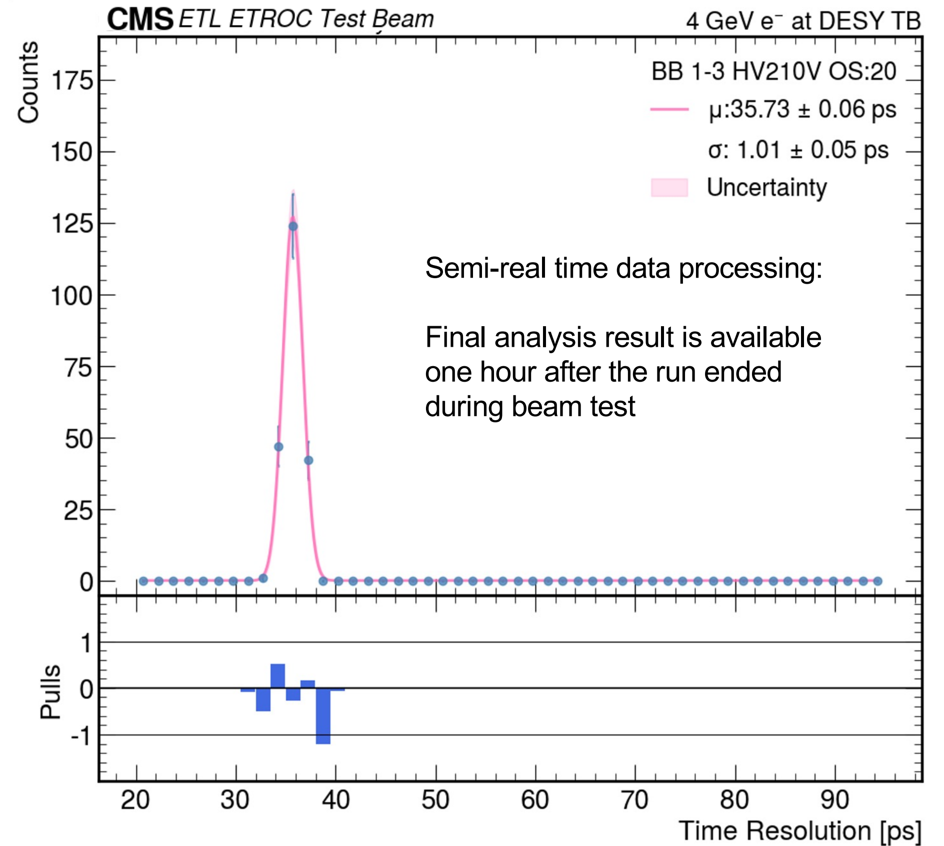
Successfully reproduced ~35ps res. with this board. Results from CERN 120-180 GeV π^+ beams agree with those from DESY 4GeV e^- beam

To be done: test in cold, and w/ irradiated sensors

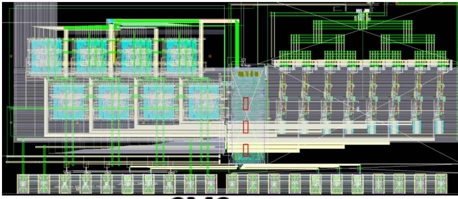
210V HV point for HPK Split-3 + ETROC2.00





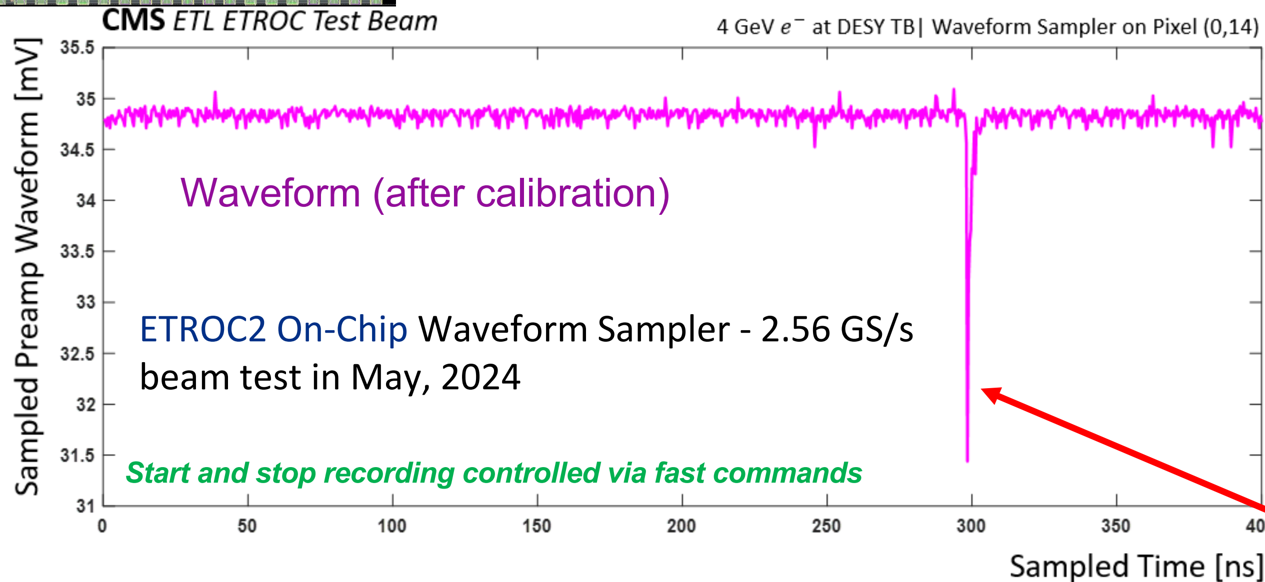


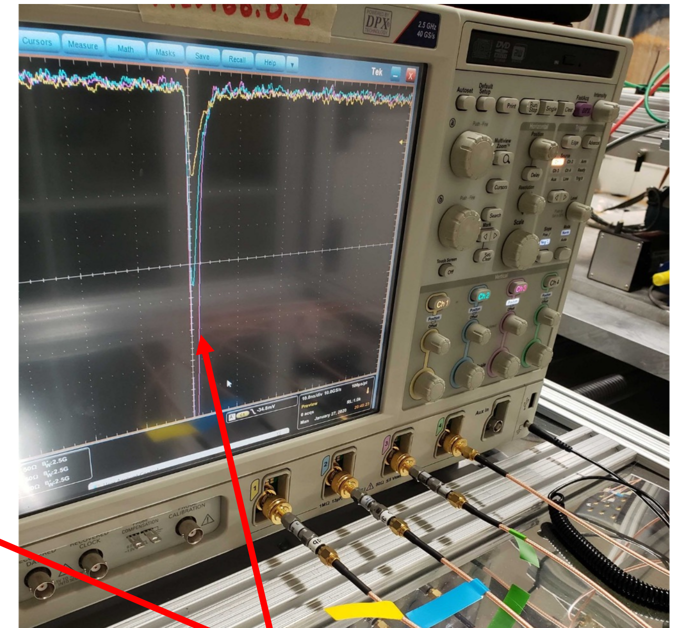
Pixel resolution map over 16x16 array



ETROC2 Waveform Sampler

Paper: IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Volume: 30, Issue: 2, Feb. 2022) Page(s): 123 – 133



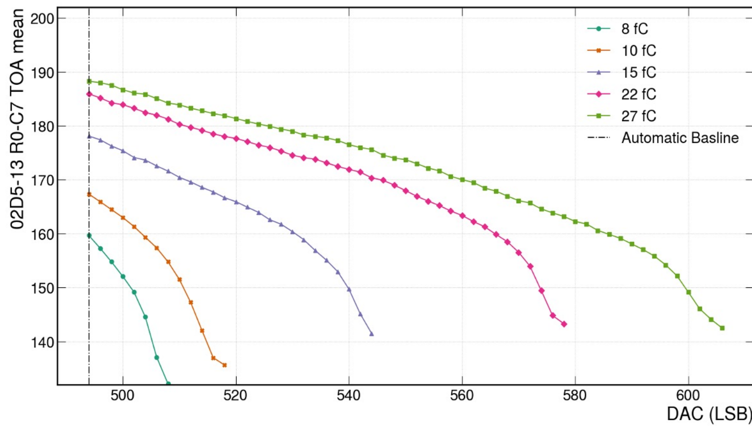


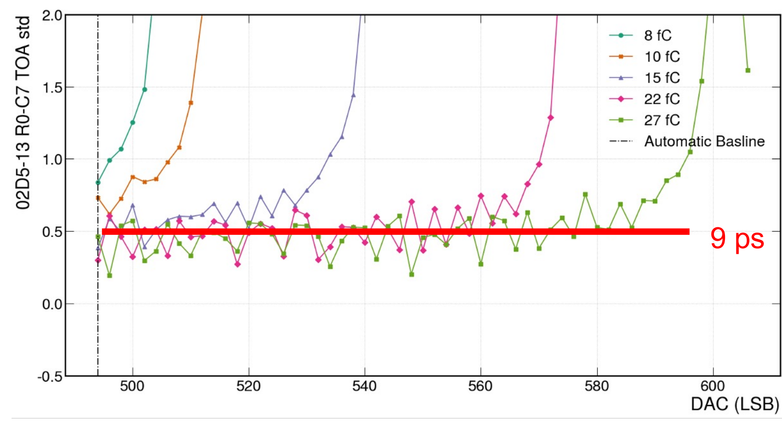
ETROC0 Preamp output waveform by Oscilloscope (40GS/s) in Jan, 2020 (beam test at Fermilab)

- 4 years after the recording of ETROC0 preamp waveforms using high speed Oscilloscope, we can now use ETROC2 on-chip waveform sampler to do the same with ETROC2 self-triggering capability

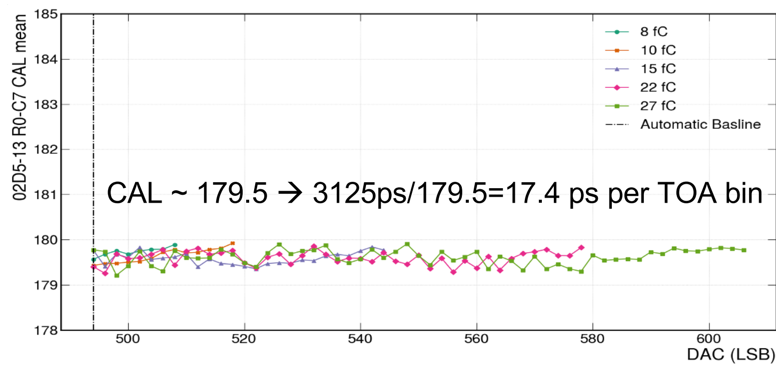
How does one travel with precision timing telescopes?

Charge vs DAC scan after 200 Mrad. (ETROC spec is 100MRad)





ETROC2.01



Temperature vs Voltage vs TID scan
done at CERN in Aug 2023 for ETROC2.01
T: from -30C too +30C
V: from 1.3V to 1.0V
TID: from 0 to 200 MRad
All works, pushed TID to 400MRad, still works.

ETROC2.03: repeated the tests in Aug 2024 at CERN and works as well, all the way to 400MRad.

Tested few chips with voltage from 1.0V to 1.4V (analog and digital) and still work

Overview of SEU protection of ETROC2

Readout operation

- Global readout: heavily TMR protected because it is critical for detector operation
  - In addition, CRC code is used for each data frame/package.
- Pixel readout: No need for TMR
  - The readout architecture ensures that all readout is globally coordinated/controlled. Non-TMR structure saves digital power, footprint, and easy for place and route
  - Instead, **Hamming code** is used for each TDC data to detect and correct errors.

Configuration registers

- All configuration bits are heavily TMR protected (global and pixel)
  - Critical global register bits could affect entire chip during detector operation. Critical pixel register would only affect one pixel in operation
  - Bit-flip should be kept at a minimum level. SEU test should pay special attention to global registers.

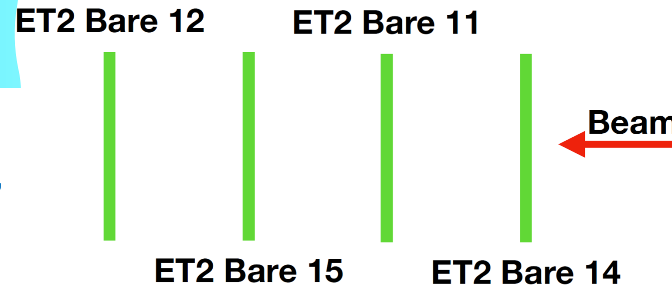
Status registers

- Registers are TMR protected but can be disabled by user
  - Most registers are unused during detector operation, except PLL capacitor array configuration and pixelID.
  - This feature can be used to monitor beam spot during beam testing(16x16 pixels)

everything should be TMRed has been TMRed, and carefully checked/verified at block level.

The proton beam SEU campaign

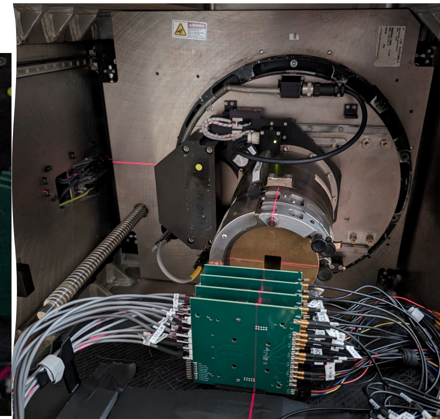
- Beam:
  - Northwestern Medicine Proton Center in Chicago, May 11th, 2024
  - Proton beam @ 217 MeV
  - Beam size 2x2 cm^2 – Measured about 3x3 cm^2
- Setup:
  - 4 "Bare" ETROC chip boards were configurated in Qinj mode. Fixed time delayed L1A commands were sending to ETROC chips during irradiation.
  - ETROC chip was reconfigured before all runs. The I2C configuration/status change were checked for each run

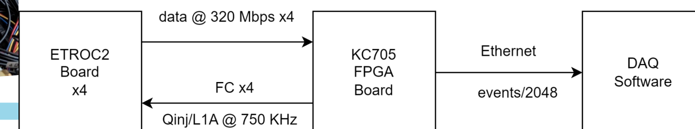


The weighted average ETL fluence is 2.86×10^{14} h/cm^2

4 "Bare" ETROC chips were irradiated up to 6.82×10^{13} p/cm^2 over 17 runs

The setup is rather involved with many long cables … To be improved…

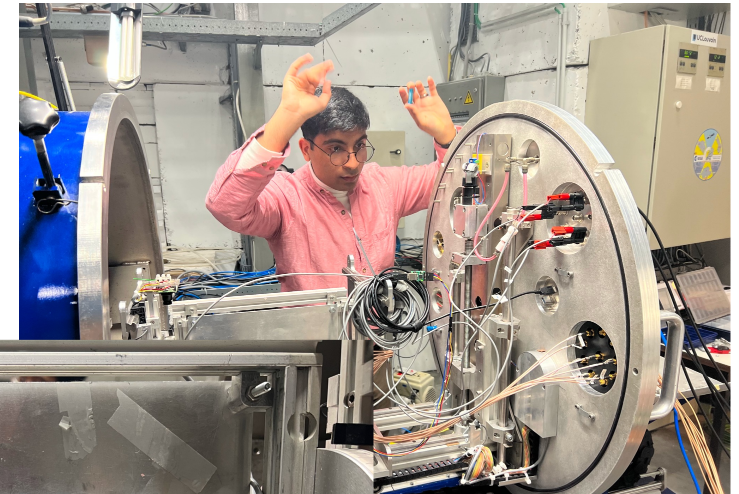


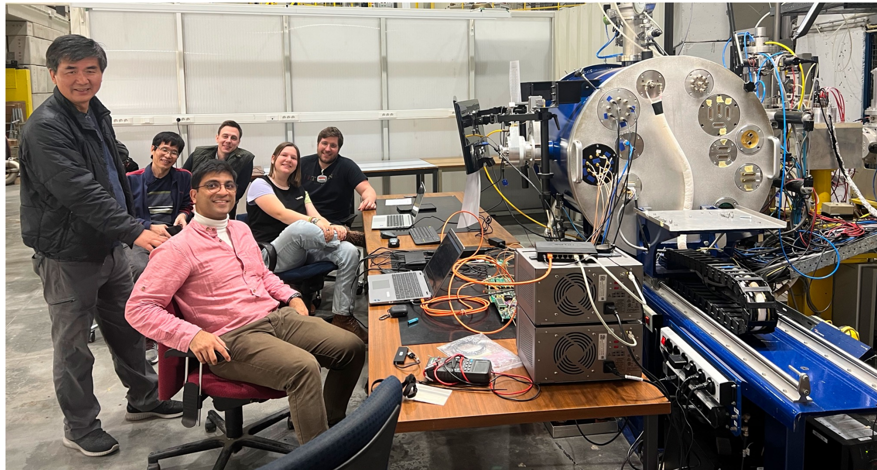


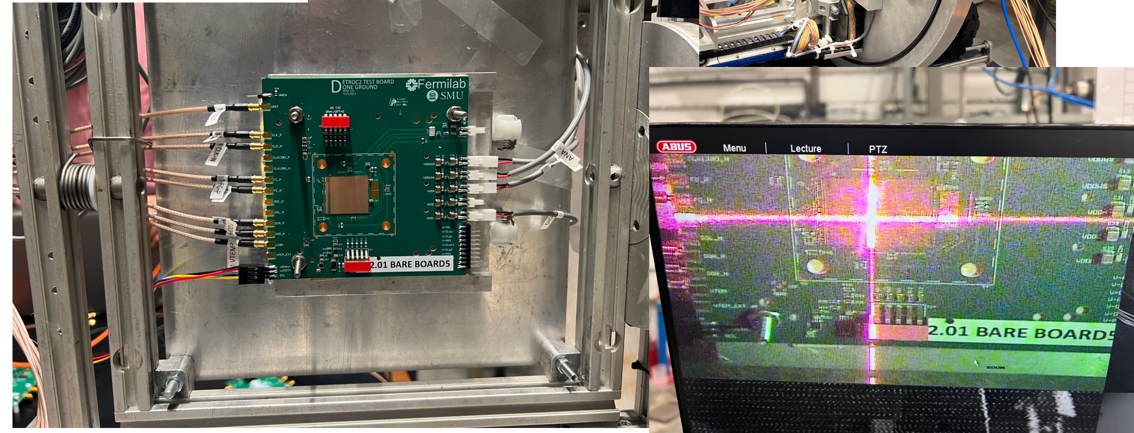
Heavy Ion SEU test at UC Louvain

Bits flipping pattern similar with proton beam
Next time: run additional HI with Al, Cr and Rh, with improved setup

Ion	LET [MeV/mg/cm²]	Fluence [p/cm²]	Time [s]	Important Peripheral Config Bit Flips	Important Pixel Config Bit Flips
Ar	9.9	1.20E+08	8640	0	0
Kr	32.4	4.00E+07	2880	0	1
Xe	62.5	6.50E+07	4935	0	22

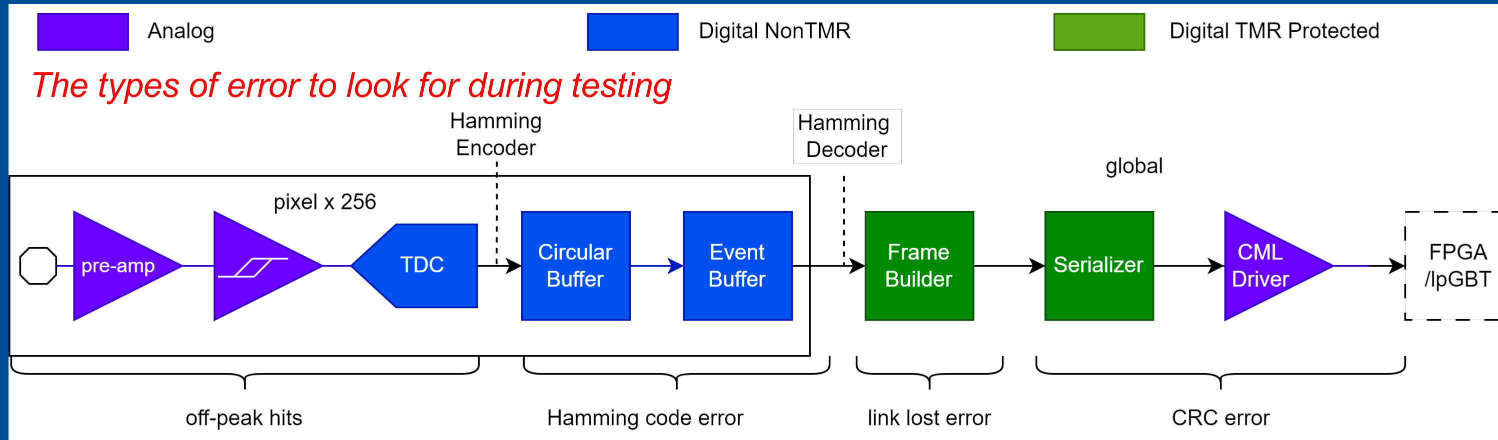






SEU event type in readout

FRAME HEADER	0	15'H3C5C	2'B00	L1Counter(8B)	TYPE (2B)	BCID (12B)
DATA	1	EA(2B)	Col_ID(4B)	Row_ID(4B)	TDC_DATA/TEST PATTERN(29B)	
FRAME TRAILER	0	CHIPID(17B)	STATUS(6B)	HITS(8B)	CRC (8B)	



- **Off peak hits**: Qinj events are expected to produce fixed CAL, TOA and TOT codes. Hits that fall beyond four standard deviations of the expected values are categorized as off-peak.
- **Hamming code error**: Two bits of EA are checked for each TDC data: 00 indicates no error, 01 indicates a 1-bit error (corrected in frame builder), and 10 indicates a 2-bit error (uncorrected).
- **CRC errors**: Data frames failing the 8-bit CRC check are flagged as CRC errors.
- **Link lost error**: Indicates that the FPGA cannot reconstruct data frames.

Summary of ETROC2 SEE testing

- No link loss errors were observed in the proton and heavy ion beam test
- No bit-flips in the global configuration registers were observed in proton and heavy ion beam test
- Proton beam tests demonstrated:
  - A low cross-section for the pixel configuration register errors, at the ~10^{-5} level over a 24-hour run
  - low Hamming code and off-peak error (~10^{-6} level)
- Future tests will feature improvements in setup to further verify readout stability in detector operations.

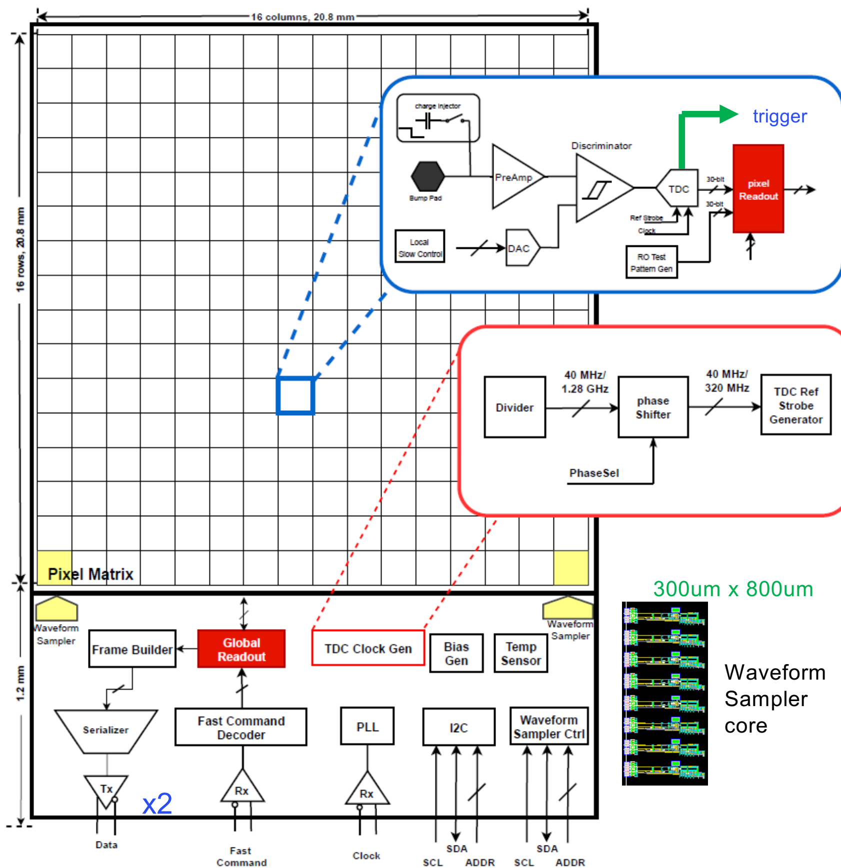
For details, see backup slides

Towards the future

- How to scale the pixel size from current 1.3mm x 1.3mm down to, say, 250um x 250um?
- A lot of new challenges…
  - Much smaller pixel size means much less room for ASIC circuits
  - Much higher power density thus much higher power consumption
    - Much more digital activities …
    - Much more IR drop …
  - Much more demand for clock distributions to deliver clocks to so many more nodes/pixels
  - …
- One fresh on-going R&D example next

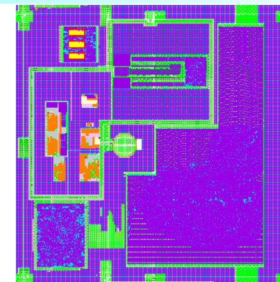
ETROC: pixel size vs design block size

65nm implementation



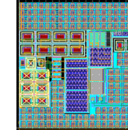
300um x 800um

Waveform Sampler core



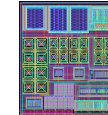
ETROC pixel layout

Preamp



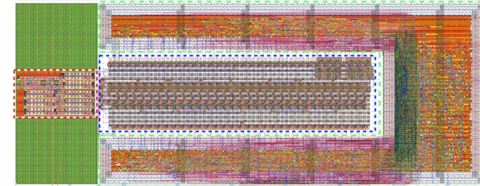
90 um X 94 um

Discriminator



81 um X 67 um

TDC: 467 um X 166 um (can be optimized and subdivided)



RAM hit buffer
250 um x 150 um

Hit circular buffer

Future challenges: how to reduce the pixel size from 1.3mm x 1.3mm to, say, 250µm x 250µm?

Towards the future: What can 3DIC VERTICAL INTEGRATION help?
→ repartition the design blocks into multi-tiers → VTROC

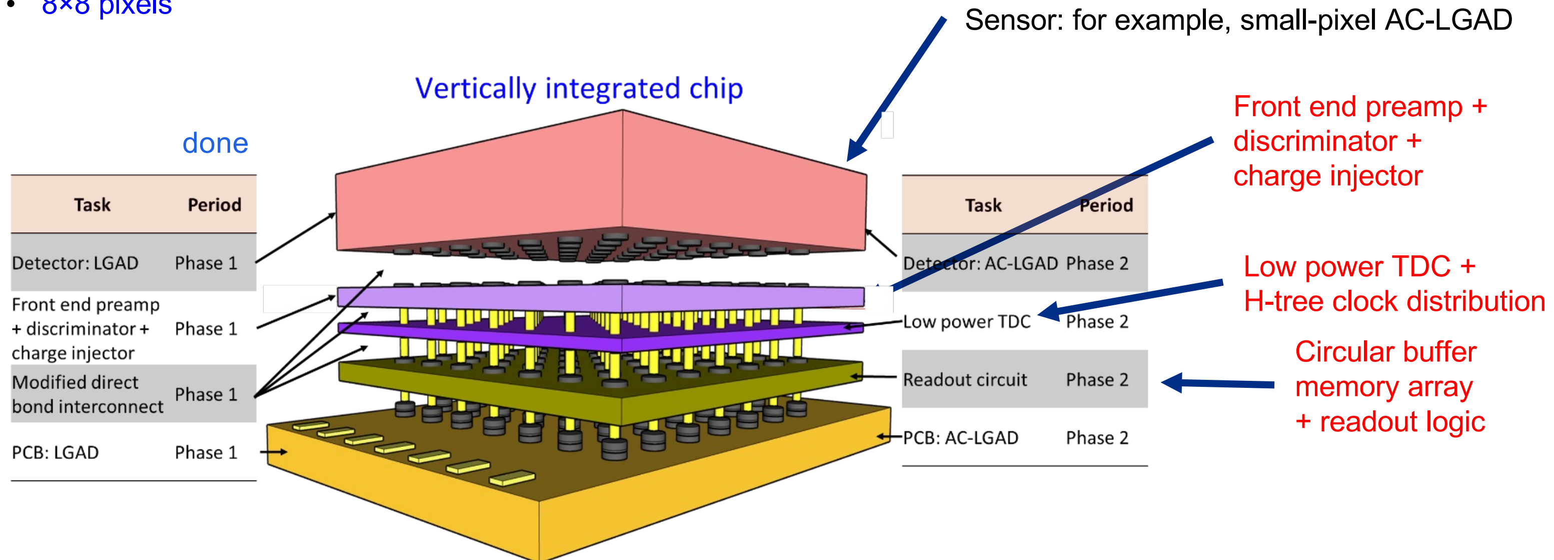
Phase II SBIR (EPIR-Fermilab) award:

"Versatile, high-density, high-yield, low-capacitance 3D integration for nuclear physics detectors" (phase 2)

For Proof-of-principle demonstration:

- 250μm x 250μm pixel
- 8×8 pixels

Sensor: for example, small-pixel AC-LGAD



Front end preamp + discriminator + charge injector

Low power TDC + H-tree clock distribution

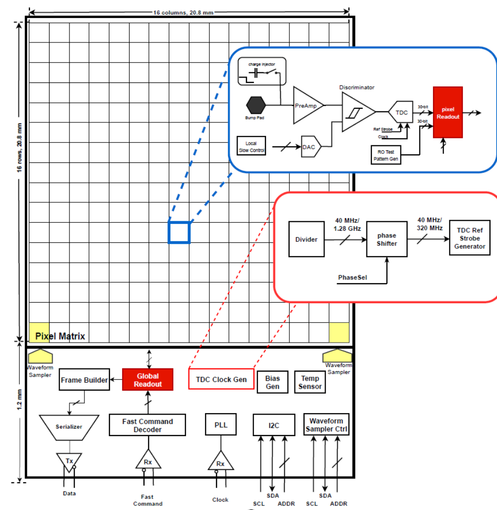
Circular buffer memory array + readout logic

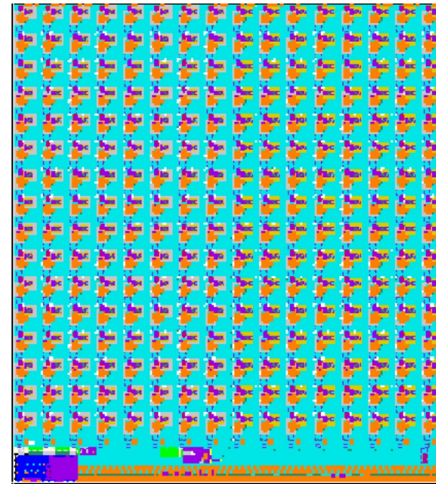
3DIC providing separation of low-noise analog circuitry from digital blocks.

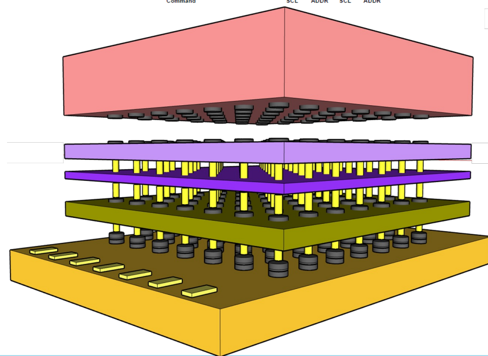
Interconnections made by TSVs and Direct Bond Interconnect (DBI).

From CMS ETROC to future R&D (VTROC1)

CMS ETL ETROC: from Concept (2019) to full chip design ETROC2 submission (Oct 2022)







"Versatile, high-density, high-yield, low-capacitance 3D integration for nuclear physics detectors" (phase 2)

Phase 1 done

Phase 2 awarded and moving to Phase 2A next (with ultra low power front-end R&D)

VTROC R&D: From Concept to first demonstration for proof-of-principle

Outlook:
Precision Position & Timing detector & Future Hadron Colliders

- Generally speaking, the ultimate physics reach of any higher energy hadron collider (given a center-of-mass energy) will be governed by its luminosity.
- Given the huge cost associated with any future higher energy hadron collider, *it is crucial to push for higher luminosity* (similar to HL-LHC). This is to maximize the new physics reach of the huge investment already made, before a new higher energy collider can be built.
- *Because precision position & timing information is the most effective means for triggering and high pile-up mitigation,* ***high precision position and timing tracking detector will be mandatory for any future hadron colliders***
- ***3DIC technology allows an open flexible architecture for future precision position and timing detector development (within and beyond HEP)***

The existing new precision timing detector projects (such as CMS MTD, ATLAS HGTD): not only will they be important for the success of physics program in the HL-LHC era, they also lay some of the technological foundations for the future of the field…

Many people involved in the ETROC2 tests (with strong support from CERN and DESY!)

ETROC2 Engineering Run at TSMC

20 wafers split in 2 lots (ETROC2)

N60R91:
6 corner wafers
(3 FFF + 3 SSS)
ETROC2.00

ESD defects observed by TSMC

2 FFF diced for testing
works well with very high yield
Extensively tested

N60R80: 14 typical wafers

8 wafers released:
ETROC2.00

2 diced for testing
works well with lower yield (~70%) due to ESD issue
Extensively tested

6 wafers on hold at TSMC. TSMC used them for investigation, and TSMC replaced them with a new lot TMSI07B-T1EAZN (for free)

ETROC2.01 (N9VX36): extensively tested
2 wafers (7&8) released in July 2023 (with high yield: 97%)
(H-tree shielding grounded at metal 3: ESD issue solved)
processed at Pactech for UBM & bumps

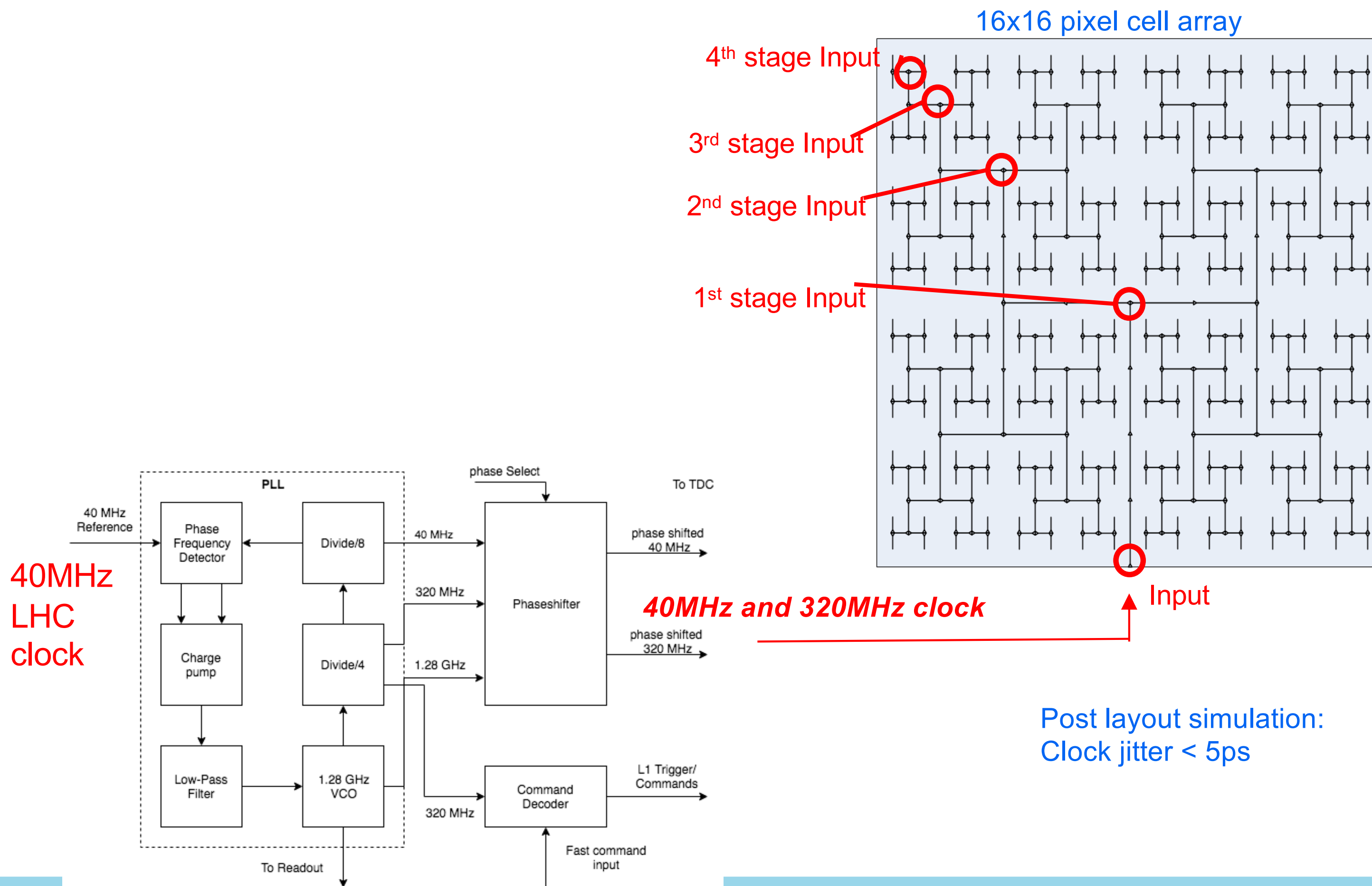
ETROC2.03 (N9VX61): rapid progress in testing since July 2024
released at TSMC in May 2024
fixed three known minor issues from ETROC2.00
added optional dummy bump pads per pixel
One wafer thinned and diced for testing (received July 2024)
One wafer processed at Winstek (UBM&bump) (received Sept 2024)

2 more wafers still on hold at TSMC

Submitted Oct 2022.

Diced chips received late April 2023

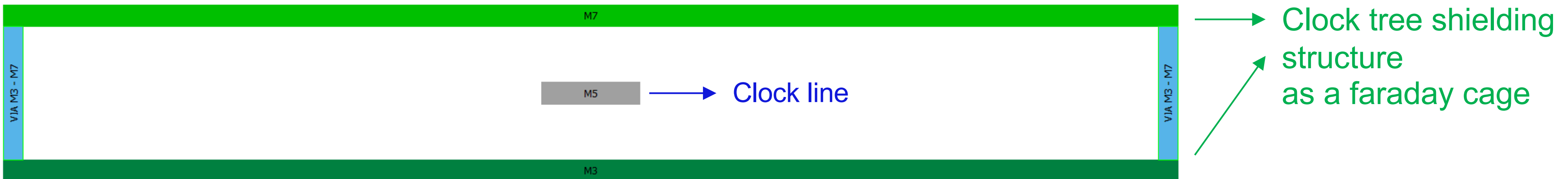
ETROC Clock Distribution (H-Tree based)



Post layout simulation:
Clock jitter < 5ps

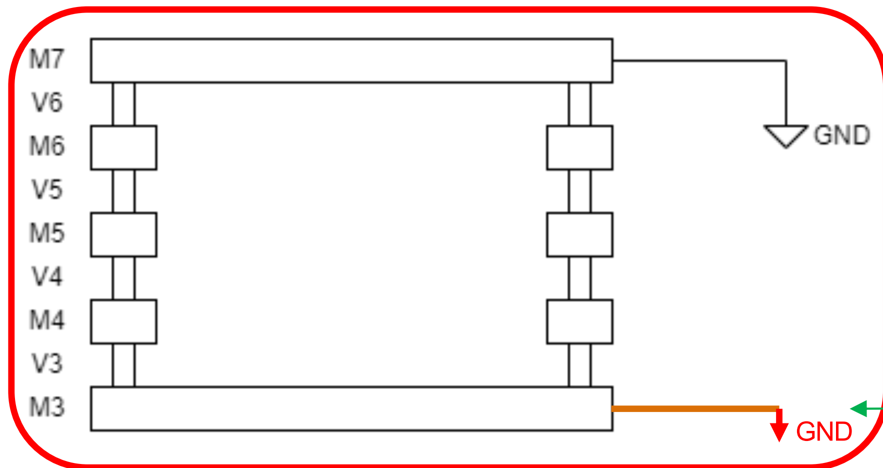
Clock Tree Layout Cross Section

Clock trace in M5 shielded by M7 and M3 (scaled diagram)



Clock tree shielding structure as a faraday cage

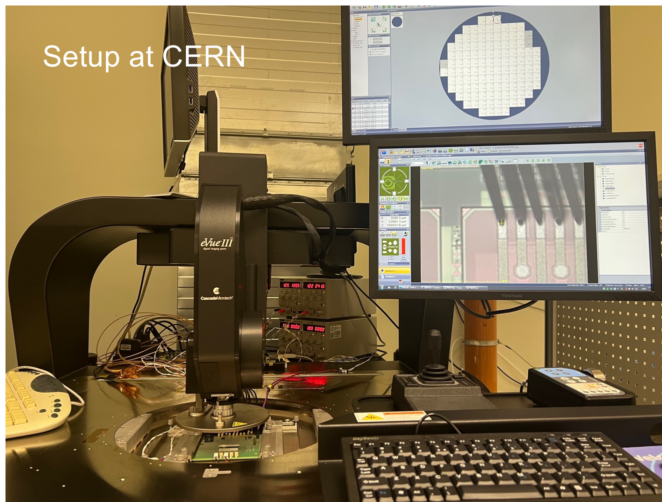
Shielded M7 and M3 connected to ground (not scaled diagram)

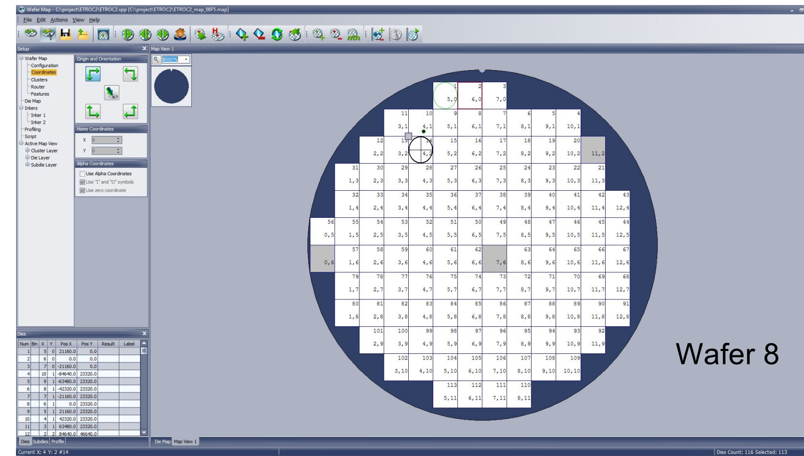


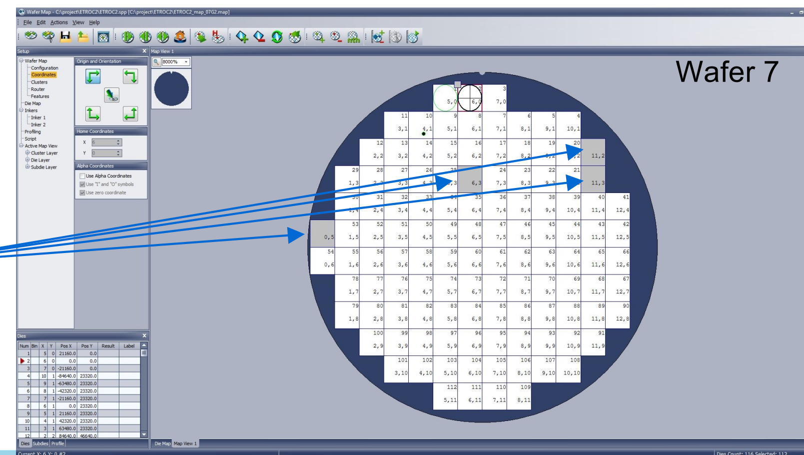
- For clock H tree shielded layers, it was not connected to the ground before M7. The large-area M3 layer keeps floating before M7 is built. This situation could accumulate large charge due to the large size of the shielding in M3, large enough to potentially cause damage during the fabrication process.
- ***This results in 10-30% defected dies/chips per wafer***
- Antenna check could not check this situation, because the antenna effect is related to protecting the gate (poly) in the manufacturing process due to the long metal line causing accumulated charge.

A simple fix (ETROC2.01): also grounded at M3

Wafer probe testing for ETROC2 wafers







Two new ETROC2.01 wafers from TSMC
Arrived CERN in Aug 2023

probe testing shows ***only 4 bad dies (out of 116 dies) per wafer in each case***

Now much higher yield achieved.

Production QC procedure developed and established for wafer probe testing.

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ETROC2.03 (N9VX61): rapid progress in testing since July 2024
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fixed three known minor issues from ETROC2.00
added optional dummy bump pads per pixel
One wafer thinned and diced for testing (received July 2024)
One wafer processed at Winstek (UBM&bump) (received Sept 2024)

2 more wafers still on hold at TSMC

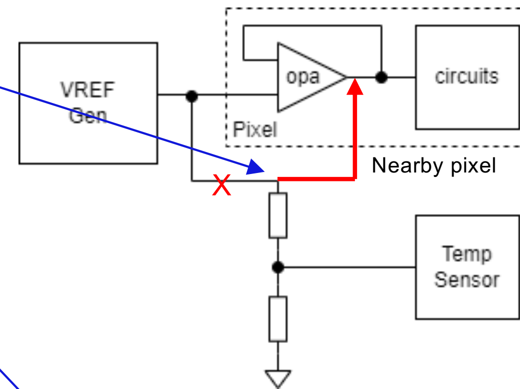
Submitted Oct 2022.

Diced chips received late April 2023

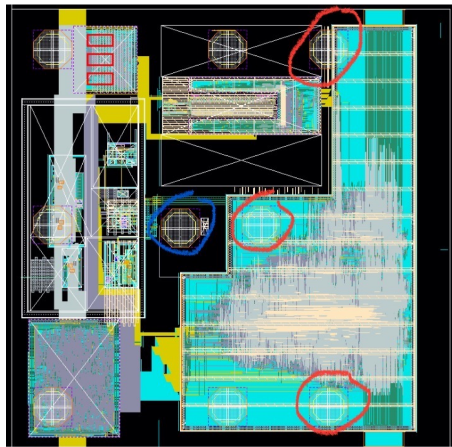
ETROC2.03: three minor modifications at metal layers with wafers on hold at TSMC

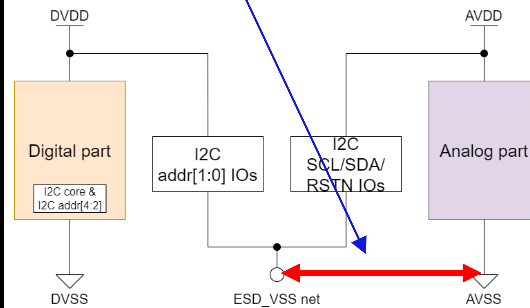
Three minor modifications at metal layers implemented in ETROC2.02 in late 2023 (submitted but not fabricated)
In early 2024, added dummy pads for each pixel, submitted as ETROC2.03 for two wafers on hold at TSMC

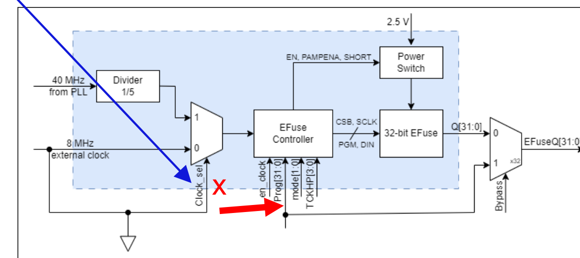
1) Disconnecting the VREF of TS (Temp Sensor).
2) Connecting floating ground net in WS.
3) Change the clock selection for Efuse.



ETROC2.03 chips received in July 2024







8 dummy/***optional*** pads added, to study bump density vs yield, plan to test only with 3 dummy pads (circled in red).

ETROC2.02: ETROC2.01 + the 3 minor fixes above
ETROC2.03: ETROC2.02 + optional dummy pads

ETROC2.03 eFuse register definition

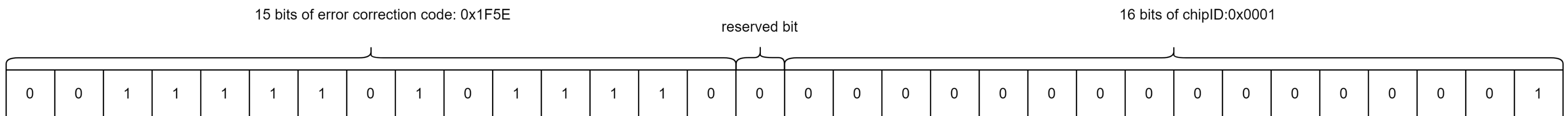
- The codeword is stored in eFuse 32-bit register
- The 32 bits of the word is divided into ChipID(16 bits), reserved bit(1 bit) and error correction bits (15 bits)
- We can further define for production: batch#, wafer #, and chip location on each wafer
  - For example: 3 bits 6 bits, 7 bits
  - Would mark: 8 batch. 2x25=50 wafers ~120 chips per wafer

Efuse ChipID can help us to keep track each ETROC chips for production:

From cradle to grave

More importantly, helps us to keep track of which sensor is bump bonded with which ETROC

From bonding to grave



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ETROC2 Testing Road Map

ETROC2.03 chips received in July 2024

Blue: done
Green: on going
Red: not yet

ETROC2 chips received in late April 2023

ETROC2 chip level testing
- Bare ETROC2 testing
  - Single pixel scan
    - Torture testing
      - *Wafer probing yield study*
      - *Temp vs Voltage vs TID to scan operation phase space*
    - TID
    - *SEU*
- Sensor + ETROC2 testing

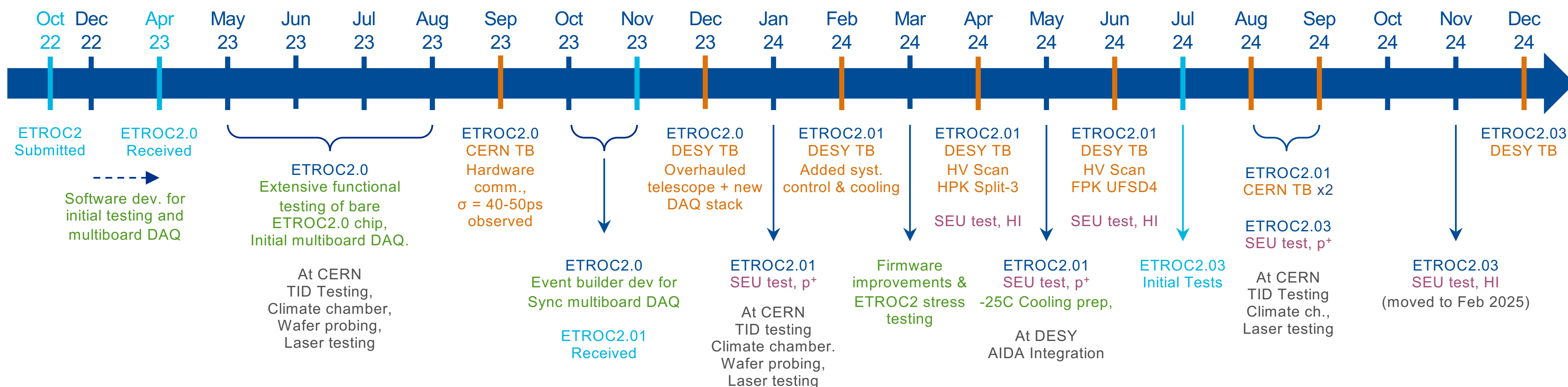
System level testing
- With Bare ETROC2
- With sensors

ETROC2.03 testing: rapid progress over past three months:

Like ETROC2.01, also very high yield;
Three fixes all confirmed successful;
Temperature vs Voltage vs TID scan all good (done at CERN);
First bump bonded ETROC2.03 seen beam in Sept, 2024
First SEU with proton beam on Sept 28, 2024
One wafer processed for UBM/Bumps by Winstek completed, ready for bump bonding;
…

ETROC2.00/2.01 have been extensively tested, ETROC2.03 is being tested as if it is the final version

ETROC2 Test Schedule



ETROC2 Testing Summary...

- ETROC2.00 and 2.01 have been extensively tested over the past year, performance meets/exceeds specifications
- ETROC2.03 testing on going, so far so good (all three minor fixes confirmed successful)

To be done: testing with irradiated sensors in beam; Improving SEU test setup for one more round of testing, improving bump bond yield.

Aim for ETROC2 PRR next summer (skip ETROC3), then production

Special thanks to the wonderful support provided by CERN/DESY for our testing

ETROC power consumption estimate vs measurements

ETROC0/ETROC1 testing results

ETROC0/1 design simulation results

Table from TDR

Circuit component	Power per channel [mW]			Power per ASIC [mW]	
Preamplifier (low-setting)	0.67	0.76	0.74	171.5	189.4 (preamp low power)
Preamplifier (high-setting)	1.25	1.31	1.27	320	325.1 (389, the highest power)
Discriminator	0.71	0.87	0.84	181.8	215.0
TDC	0.2	0.07	0.1	51.2	25.6
SRAM (→ memory)	0.35	0.25 (sim)		89.6	64.0
Supporting circuitry	0.2	0.2		51.2	51.2
Global circuitry		(reserve)		200 →	234.5

- Measurements agree with simulation of ETROC0 and 1 design
  - ***But should assume up to 20% variation with real production***
  - Note: preamp highest setting (4th gear) power is 1.52mW (measured), the high-setting above is the 3rd gear.

Sum: ~780/915/980 mW (low/high/highest power)
Use 980mW & add 20% for worst case.

ETROC2 measurements on three bump bonded chips (room temperature):

Earlier estimate during design stage:

Typical chip low power: 346/138 mA analog/digital → 581 mW
Corner FFF low power: 402/247 mA → 779 mW
↔ 780mW (preamp low power)

Typical chip high power: 477/138 mA analog/digital → 738 mW
Corner FFF high power: 525/247 mA → 926 mW
↔ 980mW (preamp high power)

The ETROC2 power consumption meets ETL requirements (the original estimate was conservative enough)
Much of the power saving was due to extensive optimization of the digital activities (to minimize noise)

Lower temperature → lower power

Number of ETROC2 chips tested so far

TID tests

Board	Generation	TID	Date	Comment
02D5 #11	ET2.00, Typical	200 MRad	2023 Aug	
02D5 #12	ET2.00, Typical	200 MRad	2023 Aug	
02D5 #13	ET2.00, Typical	200 MRad	2023 Aug	
01E2 #48	ET2.00, Typical	200 MRad	2023 Sep	
01E2 #52	ET2.00, Typical	200 MRad	2023 Sep	
ET2 W36-6		400 MRad	2024 Jan	Wire-bonded
ET2.03 Bare 7	ET2.03, Typical	200 MRad	2024 Aug	
ET2.03 Bare 9	ET2.03, Typical	400 MRad	2024 Aug	

SEU tests

Board	Location	Fluence (p/cm2)	Date	Comment
ET2.01 Bare 1	Northwestern hosptial	4.75E+13	2024 Jan	
ET2.01 Bare 4	Northwestern hosptial	4.75E+13	2024 Jan	
ET2.01 Bare 5	UC Louvain	Xe: 1.1804E+8	2024 Apr	
		Ar: 2.7E+7		
		Kr: 2.7E+7		
ET2.01 Bare 11	Northwestern hosptial	6.19E+13	2024 May	
ET2.01 Bare 12	Northwestern hosptial	6.19E+13	2024 May	
ET2.01 Bare 14	Northwestern hosptial	6.19E+13	2024 May	
ET2.01 Bare 15	Northwestern hosptial	6.19E+13	2024 May	
ET2.01 Bare 7	UC Louvain	Xe: 6.5E+7	2024 Jun	
		Ar: 1.2E+8	2024 Jun	
		Kr: 4.0E+7	2024 Jun	

+ 8 ETROC2.03
in proton beam for SEU
on Sept 28, 2024.

In total,

8 ETROC2 wafers have been probe tested (~116 dies/wafer)

163 chips have been tested on ETROC test boards;

8 chips tested for TID (200-400MRad)

16 chips tested for SEU

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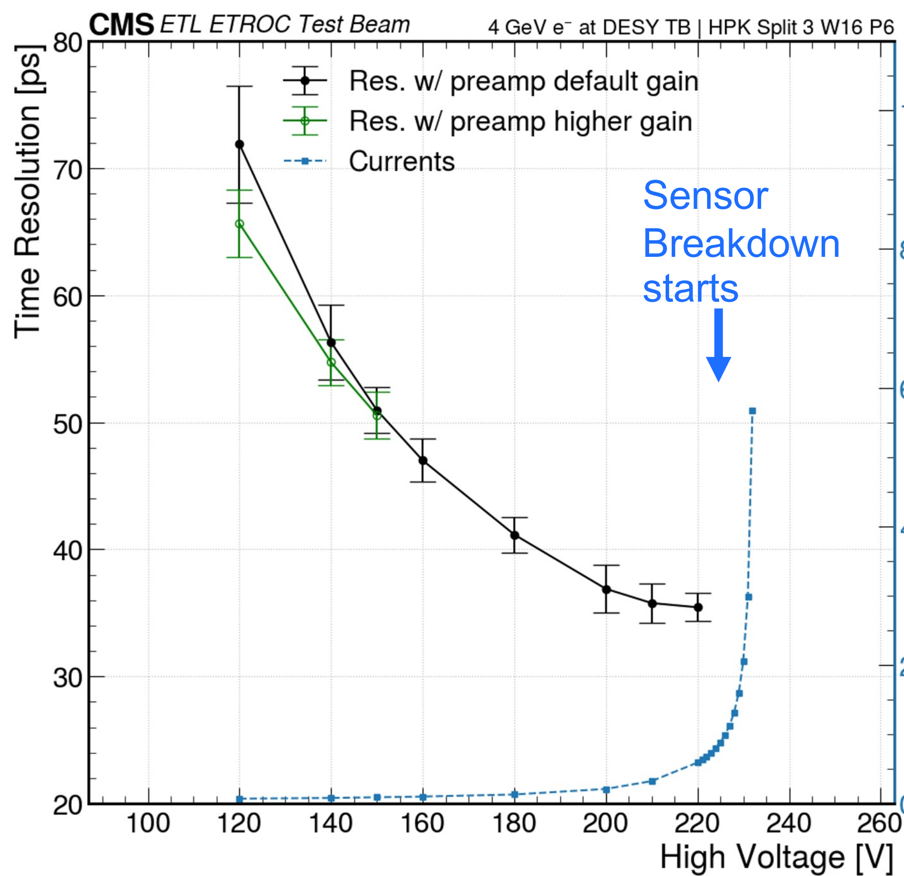
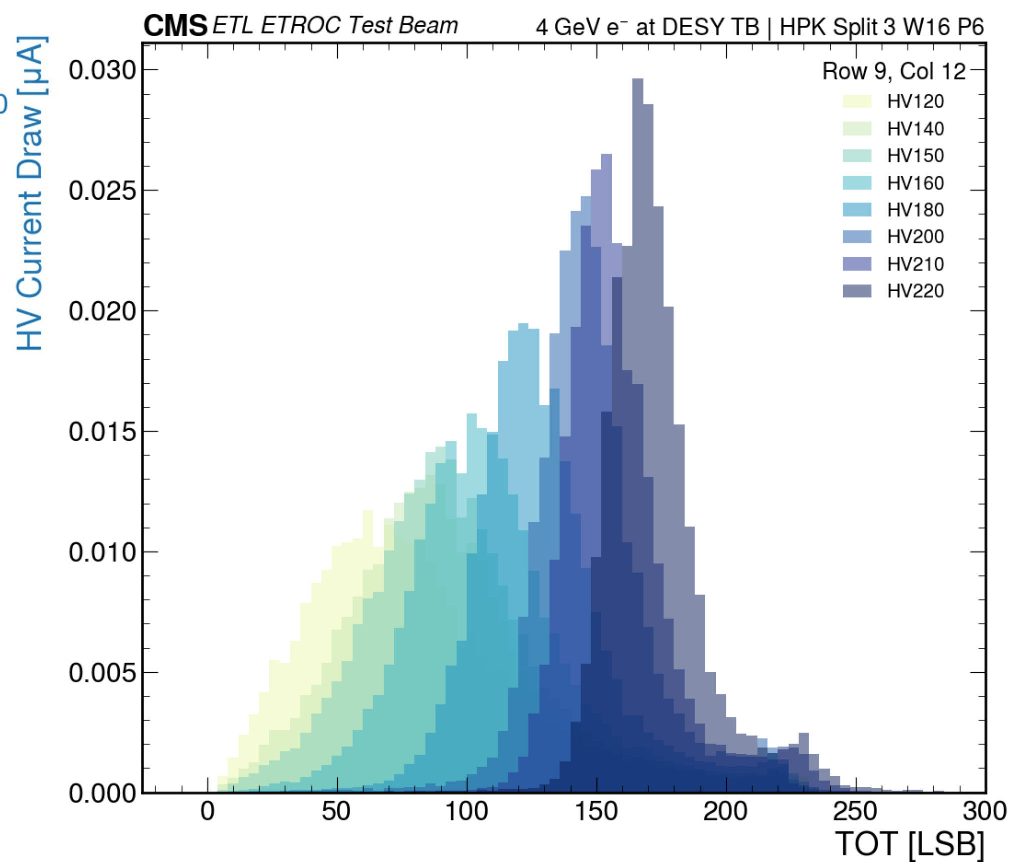
HV Scan for HPK Split-3 + ETROC2.00: w/o temp control





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