

# Readout ASIC for GRAIN IAr SiPM arrays

## Update

GRAIN Meeting  
September 27, 2024

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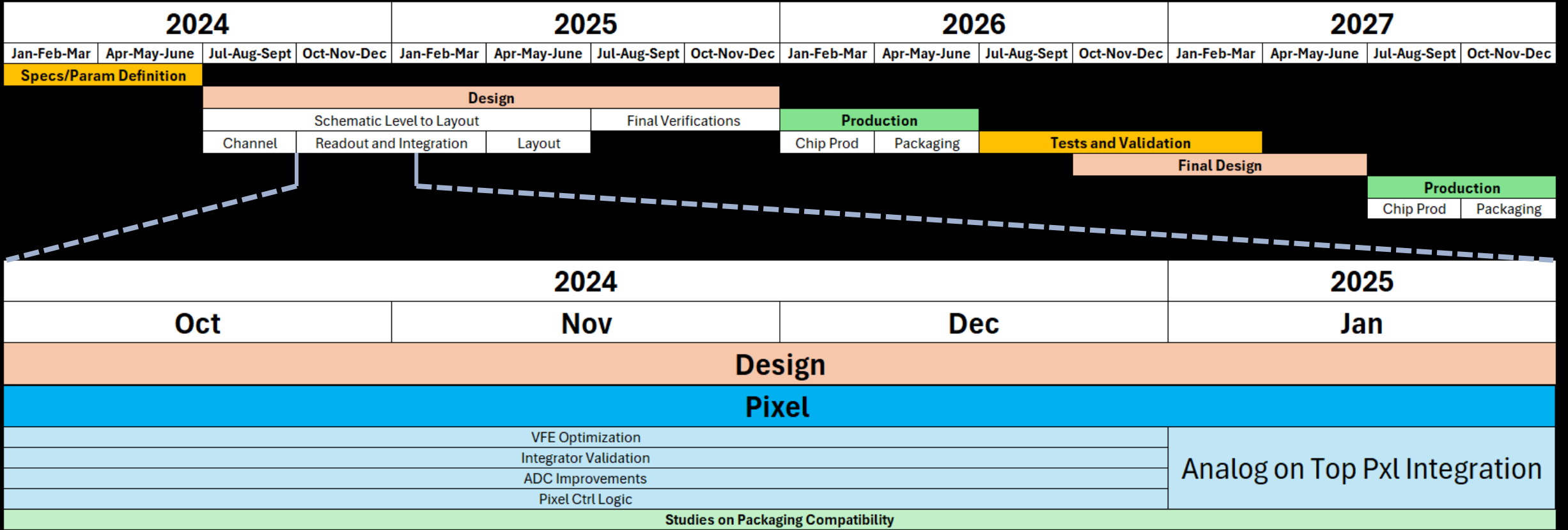
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1. Timeline and Short/Medium-Term Goals
2. Ongoing Activities

# Timeline

2024				2025				2026				2027							
Jan-Feb-Mar	Apr-May-June	Jul-Aug-Sept	Oct-Nov-Dec	Jan-Feb-Mar	Apr-May-June	Jul-Aug-Sept	Oct-Nov-Dec	Jan-Feb-Mar	Apr-May-June	Jul-Aug-Sept	Oct-Nov-Dec	Jan-Feb-Mar	Apr-May-June	Jul-Aug-Sept	Oct-Nov-Dec				
Specs/Param Definition				Design				Production				Tests and Validation							
Schematic Level to Layout				Final Verifications				Chip Prod				Packaging							
Channel	Readout and Integration		Layout					Final Design				Production							
												Chip Prod				Packaging			

# Timeline: Short-Term Goals



+ Cryogenic and room temperature ALCOR tests

# Timeline: Medium-Term Goal

1024 pixels prototype designed with a scalable approach:

- **By  $\approx$  April : 2 x 2 Pixels Matrix Prototype**
  - GdsII
  - **NO real production!**
  - Case study for optimizing the full integration flow

# Ongoing Activities: Pixel Design

## Integrator Design:

- Transistor level design in Virtuoso
  - Current mirror based
  - DC current compensation
  - Two gains
- First simulation analyses soon

## ADC Design Improvements :

- Backward compatibility
- New SAR-based conversion algorithm
  - Faster conversion
  - Control logic and current injection improvements
- Block ready for integration expected by the beginning of December

## VFE Optimization :

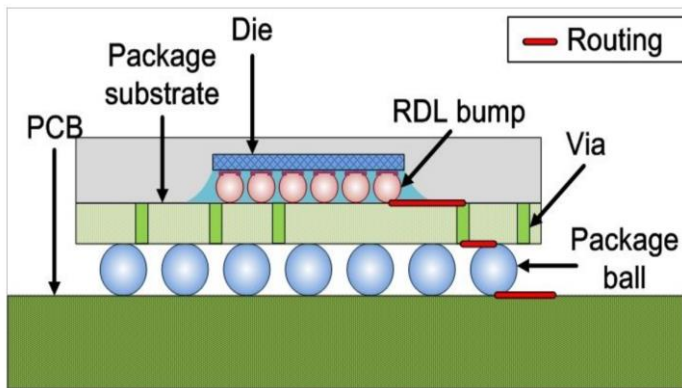
- ALCOR Cryogenic tests and simulations showed:
  - $V_{th}$  and R variations impact mostly the TIA and the DACs
- Optimization
  - TIA and DACs design optimization
  - Configurable resistor arrays and current correction

# Pixel

# Flip-Chip BGA package

Slide from : S.Durando, «The New ASIC for GRAIN», July 11th, 2024, INFN-LNF

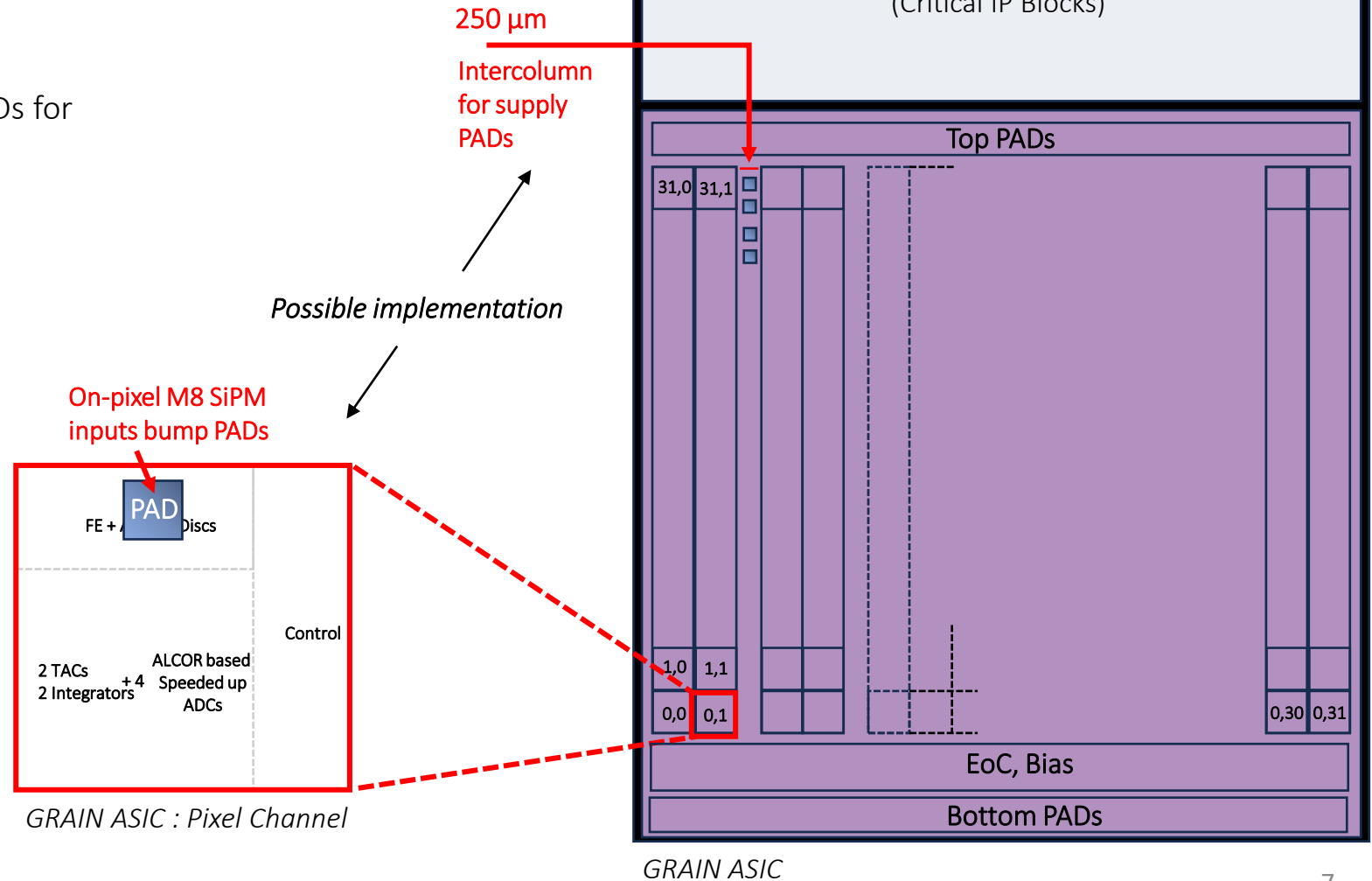
- The ASIC is bump-bonded to an interposer connected to the board with package balls
  - On-pixel PAD for SiPM
  - Inter-column supply and ground PADs for reduced IR drops
- Similar approach is followed for ALCOR v3 implementation for EIC



Flip-chip BGA working principle

Hsu, Hsin-Wu & Chen, Meng-Ling & Chen, Hung-Ming & Li, Hung-Chun & Chen, Shi-Hao. (2012). On effective flip-chip routing via pseudo single redistribution layer. 1597-1602.

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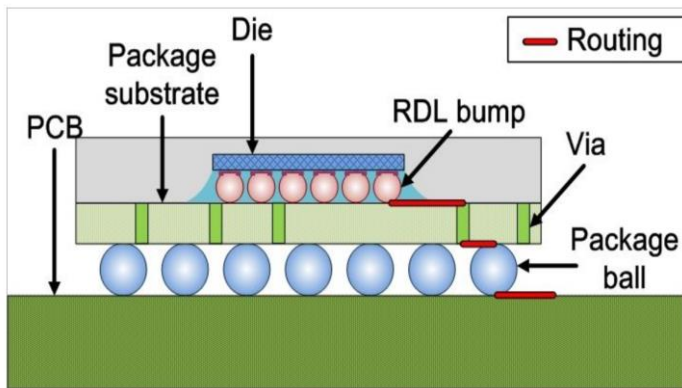


GRAIN ASIC : Pixel Channel

GRAIN ASIC

# Ongoing Activities: Pixel Design

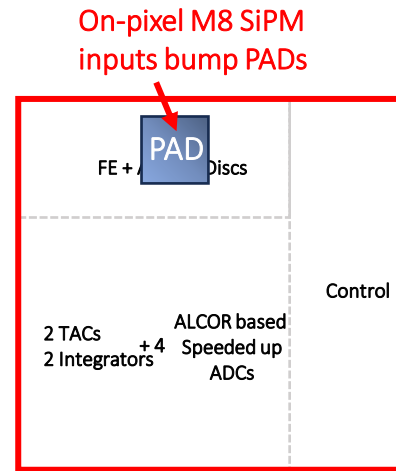
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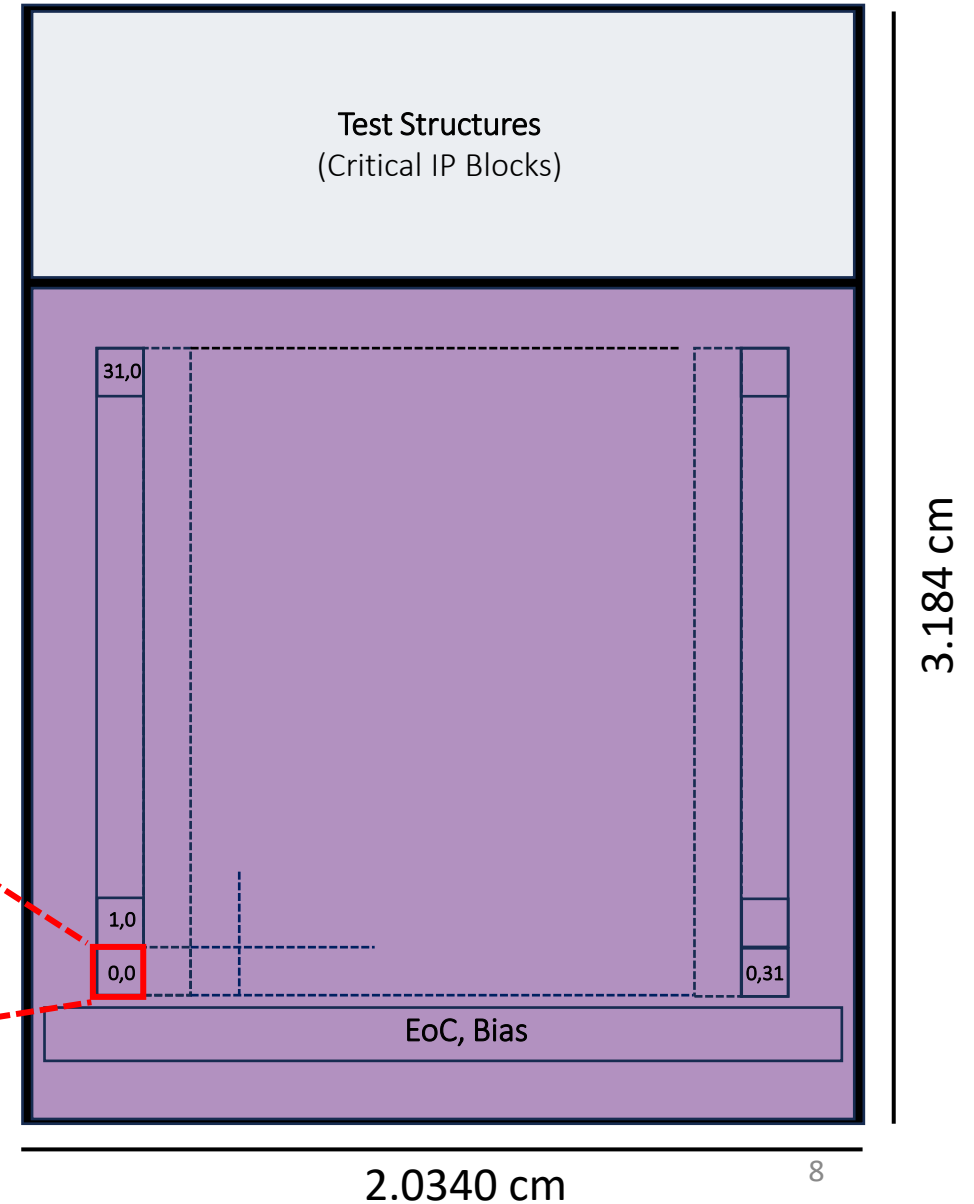
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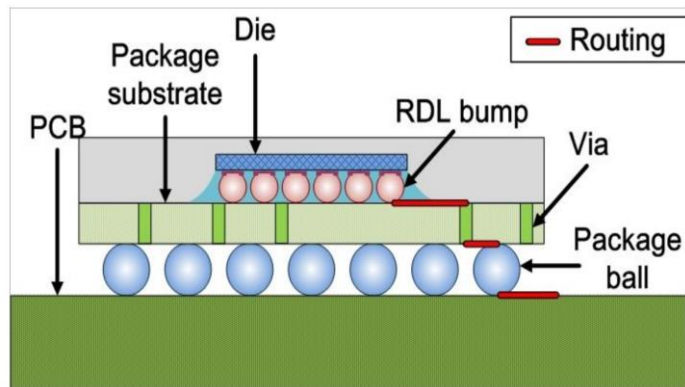
GRAIN ASIC : Pixel Channel





# Ongoing Activities: Pixel Design

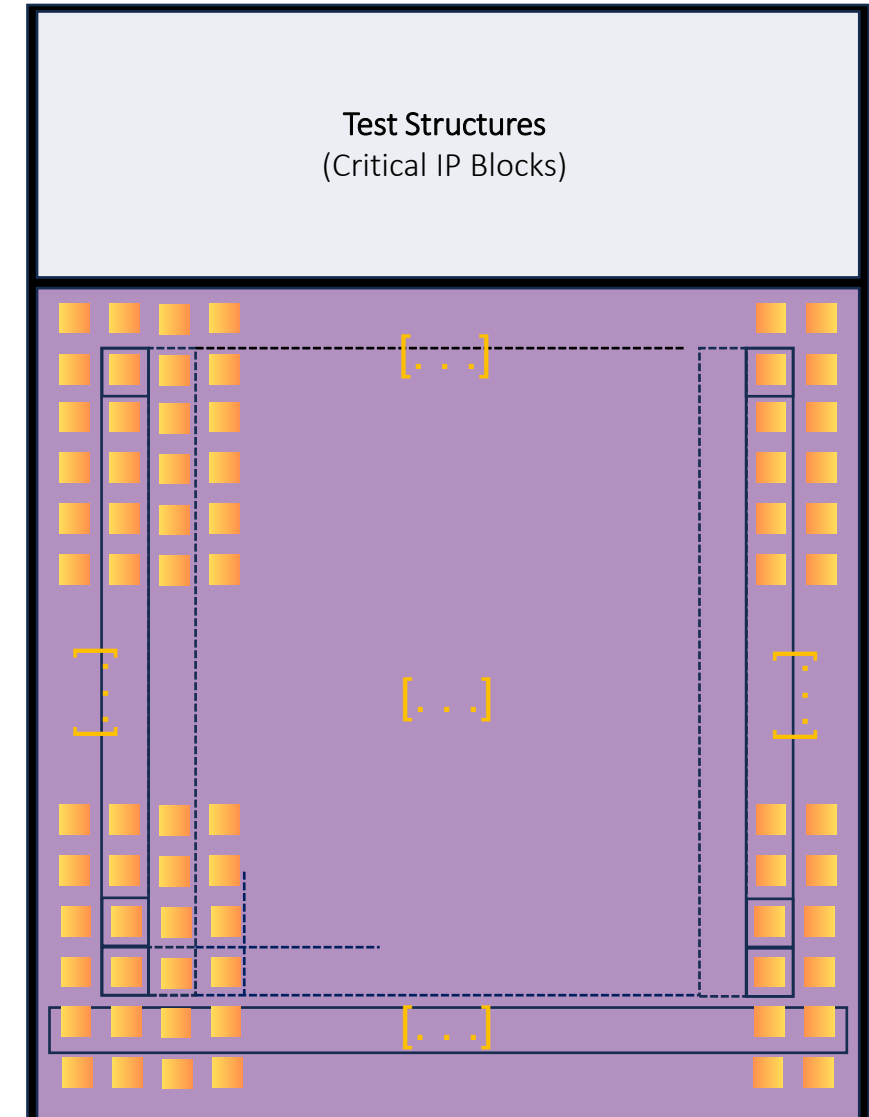
- The ASIC is bump-bonded to an interposer connected to the board with package balls
  - On-pixel PAD for SiPM
  - Inter-column supply and ground PADs for reduced IR drops
- Similar approach is followed for ALCOR v3 implementation for EIC
- 40 x 40 PADs uniformly distributed : Easier Assembly and interface to the SiPM matrix



*Flip-chip BGA working principle*

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The background of the slide is a photograph of an open book. The left page is covered in a fine, light-colored grid pattern, resembling graph paper. The right page is a solid, reddish-brown color. The book is resting on a dark, textured surface.

**Thanks**

The background of the slide is a photograph of a slide tray. The tray is a light blue or grey color with a fine grid pattern. It is positioned diagonally, with the top-left corner towards the upper left of the frame. The tray is resting on a dark, textured surface, possibly a desk or table. The lighting is soft, creating a slight shadow on the right side of the tray.

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