DAPHNE V3 Update

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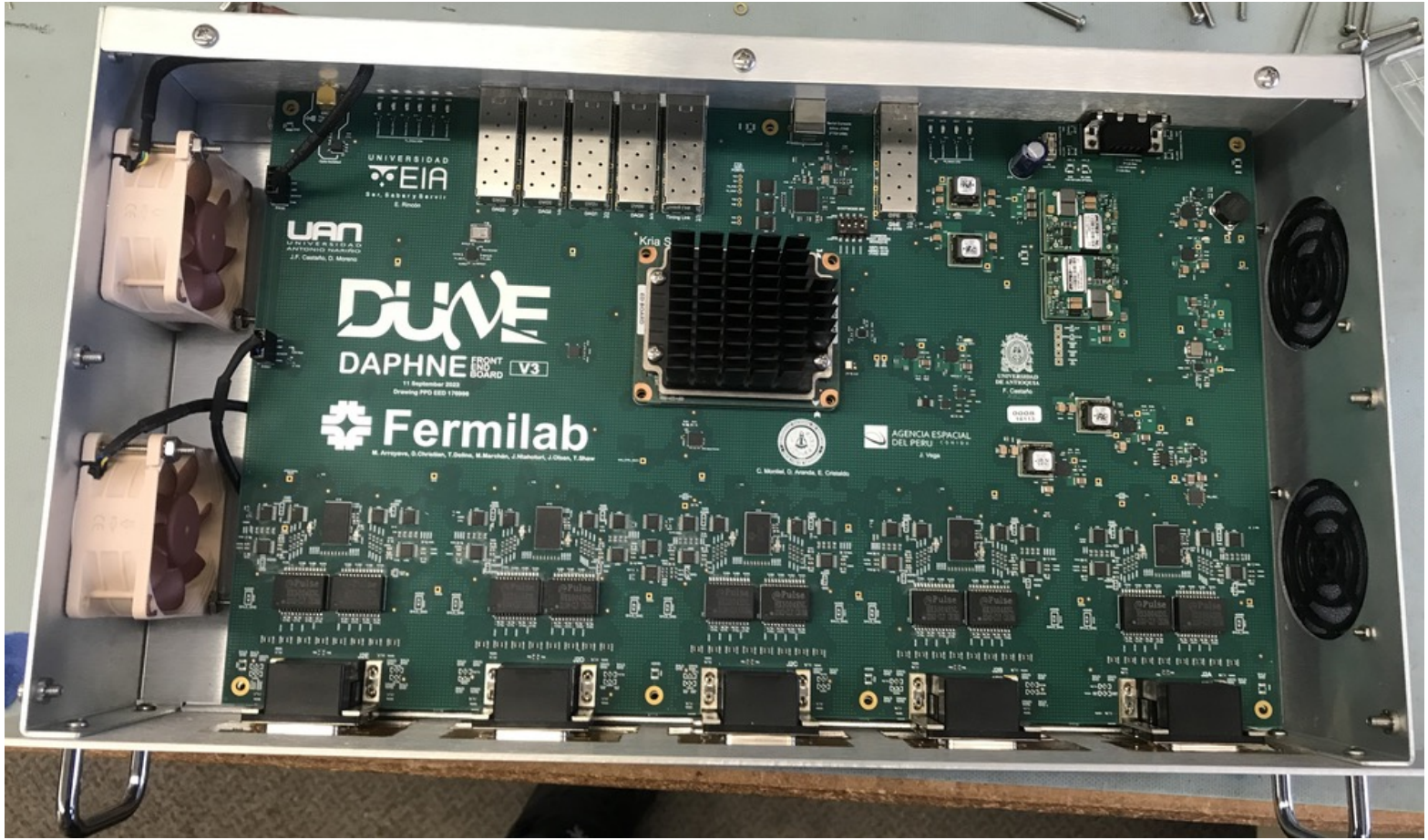
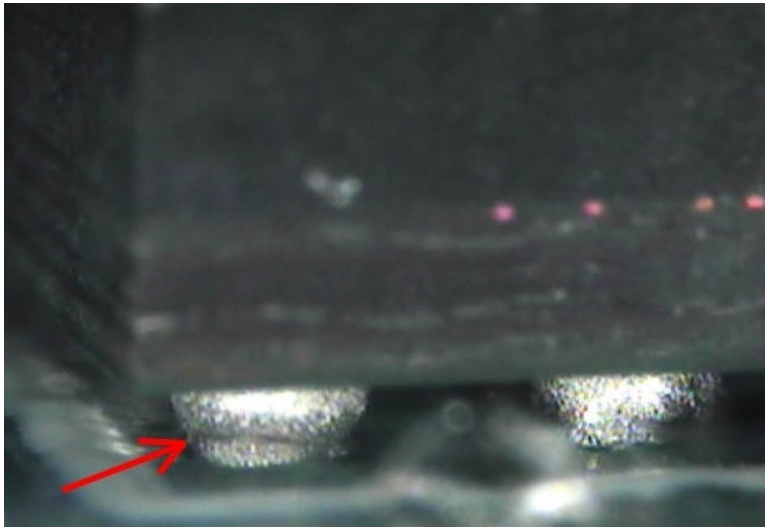
3 October 2024


UNIVERSIDAD EIA
UAN
DUNE
DAPHNE FRONT END BOARD V3
Fermilab
AGENCIA ESPACIAL DEL PERU

Prototype Run

- Late 2023: 10 boards made in one run, no first articles.
- Assembly vendor had issues with solder ball reflow
  - “head in pillow” opens
- The boards sent back for reflow January 2024
  - Initially looked good, but found opens later in the data lines between AFE chips and FPGA
- A few boards sent to another vendor to remove, clean pads, and replace some AFEs (BGA packages) August 2024
  - Some connections were fixed, but we still have boards with open connections
  - Bad connections may be on the Kria connector (also BGA)
- We suspect bad solder paste/flux and bad temperature profile at assembly vendor is the cause.



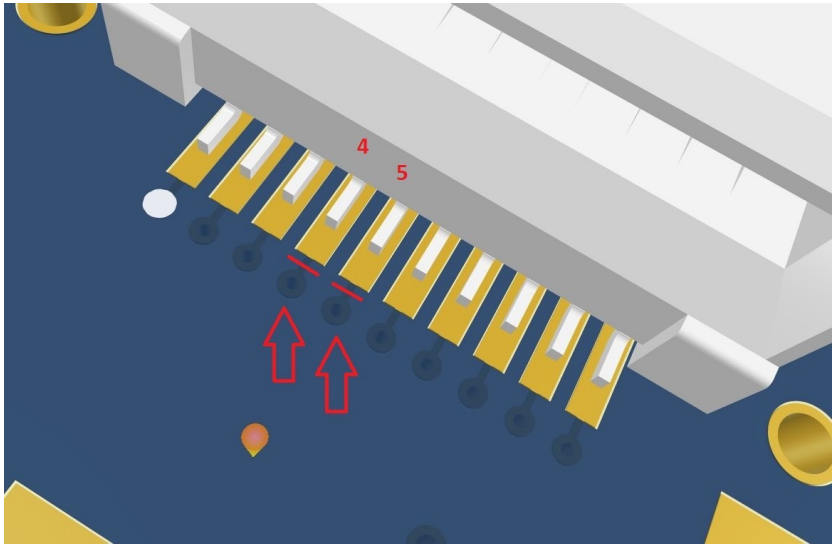
Recent I2C Issues

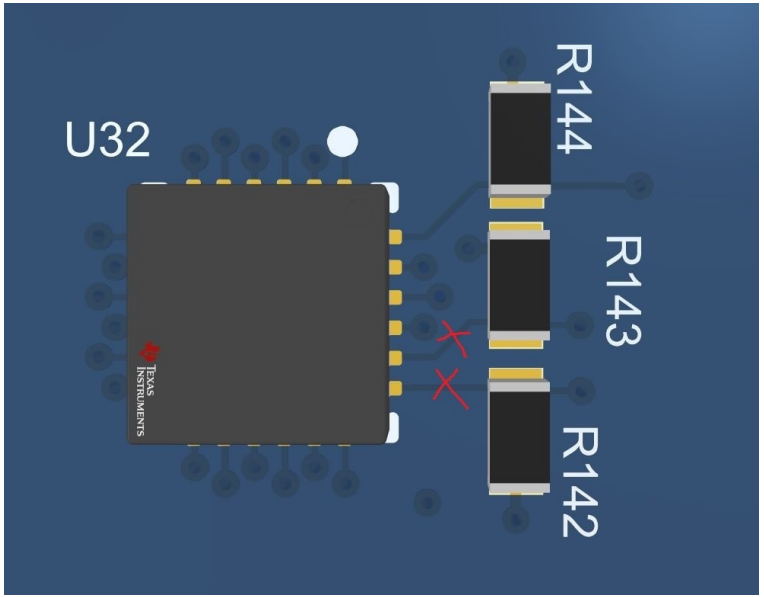
- Two I2C buses on DAPHNE
- Address conflicts with devices on both buses
- PL (logic side)
  - Conflict prevents reliable communication with the Clock Generator
  - We need to configure Clock Generator to produce the reference clocks we need to test 10G DAQ link
  - Cut traces to remove U32 switch from I2C bus
- PS (processor side)
  - Conflict prevents communication with EEPROM
  - Cut traces to remove SFP switch

Kria PL (Logic) I2C Bus			
Reference	Device	Description	Address (7 bit)
U32	TCA9548ARGERQ1	I2C expander/switch for 5 SFPs:	112 (!)
J1	SFP+	0: DAQ 10G GTH2	80
J10	SFP+	1: DAQ 10G GTH1	80
J8	SFP+	2: DAQ 10G GTH0	80
J16	SFP	3: Timing Interface	80
J7	SFP+	4: DAQ 10G GTH3	80
U18	SI5338A-B-GMR	Clock Generator	112 (!)
U39	PJT004A0X43-SRZ	PMBus Regulator +3.3VD	18
U36	PJT004A0X43-SRZ	PMBus Regulator +1.8VD	54
U33	PJT004A0X43-SRZ	PMBus Regulator +3.6V	50
U42	PJT004A0X43-SRZ	PMBus Regulator +2.1V	22

Kria PS (Processor) I2C Bus			
Reference	Device	Description	Address (7 bit)
N/A	M24C64	EEPROM on the Kria SOM	80 (!) and 88
J18	SFP	Gigabit Ethernet optical SFP module	80 (!)
U9	MCP9808-E/MS	Temperature sensor	24
U37	ADS7138QRTERQ1	ADC 8 ch (monitor +3.3VD, +1.8VD, bias, CEV)	16
U40	ADS7138QRTERQ1	ADC 8 ch (monitor +1.8VA, +3.3VA, -5VA)	23

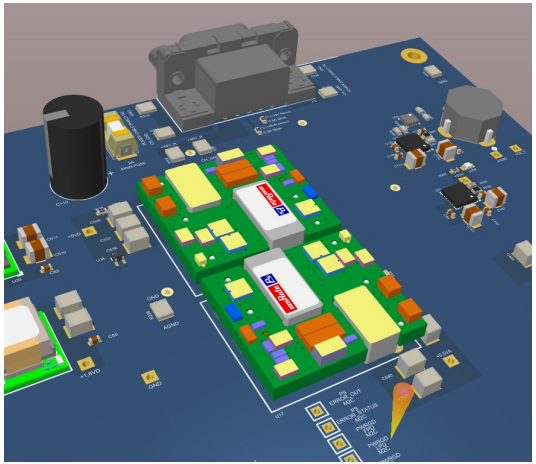
I2C Fix: Board Mods

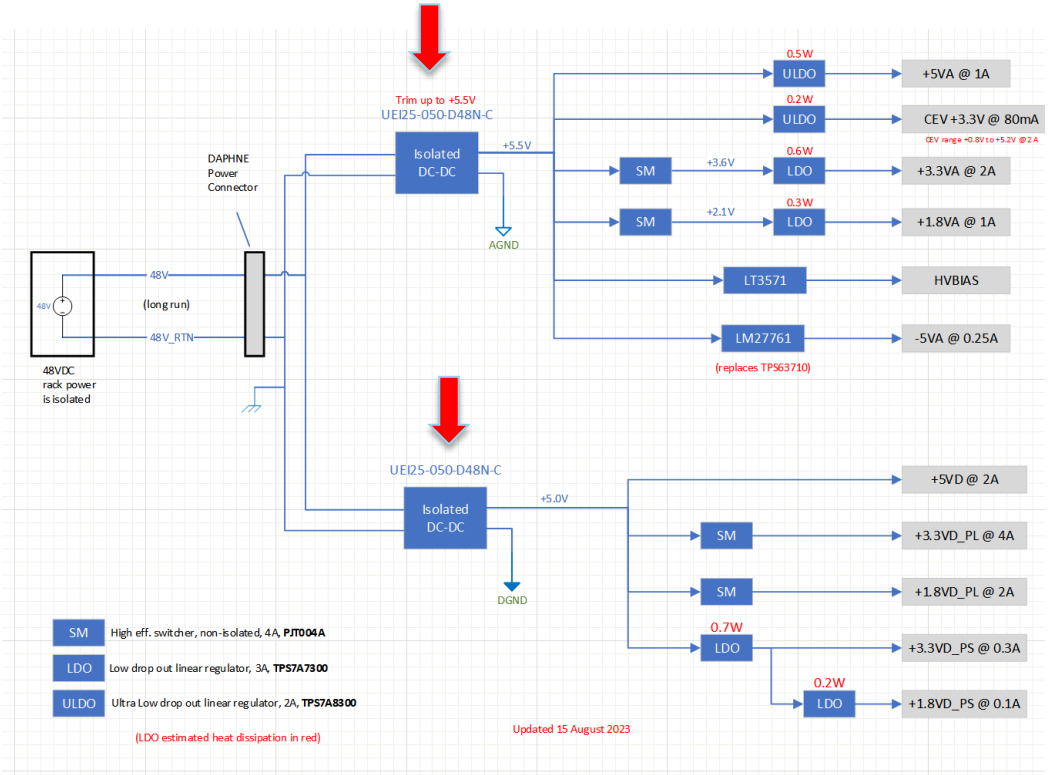




Power Supply Changes

- Observed switching noise coming from the two isolated DC-DC converters
- Replace them with shielded versions which are footprint compatible



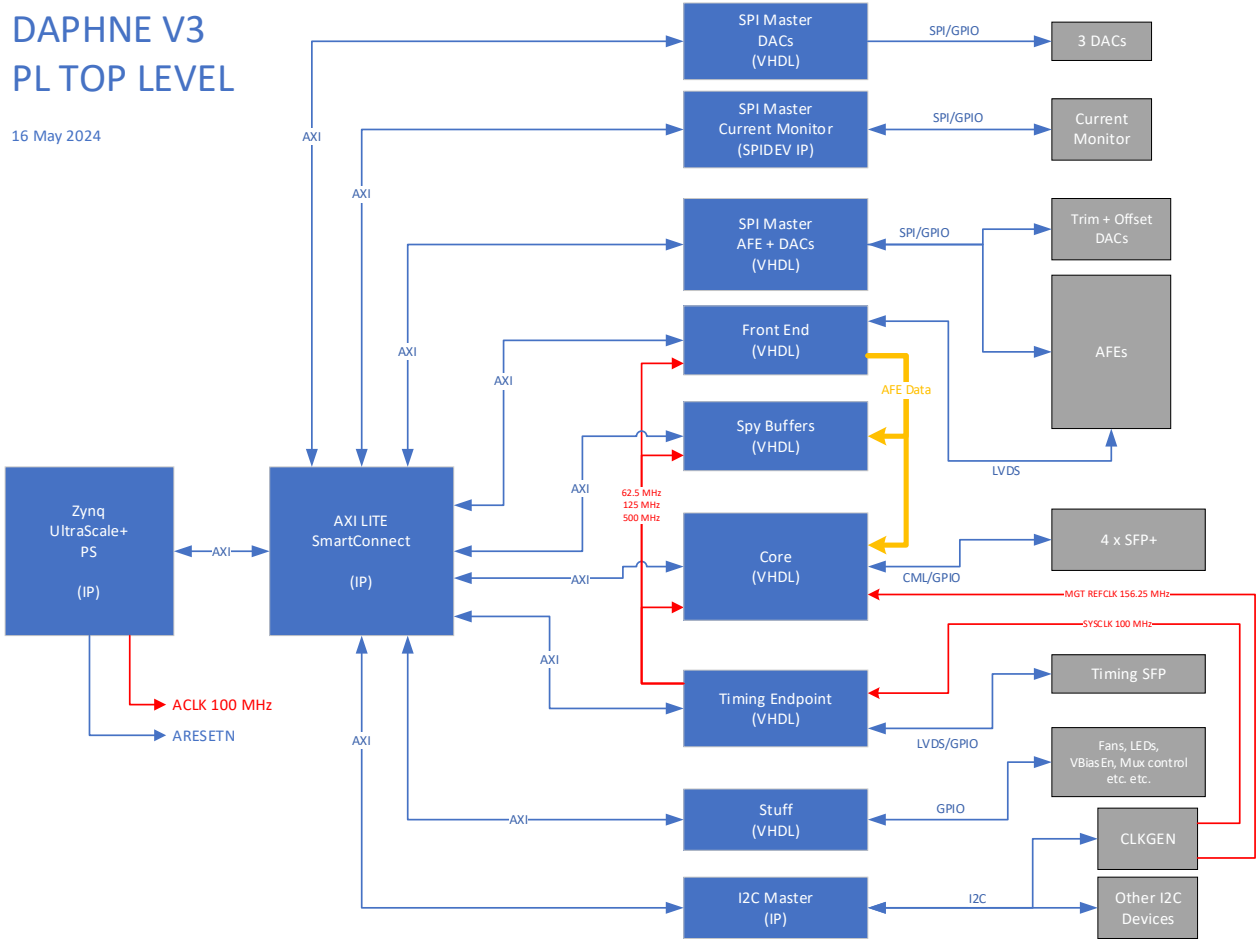


Firmware Status

- From the Kria processor we can communicate with all board level components (I2C + SPI)
  - Many custom firmware blocks (PL) connected via AXI-LITE to processor (PS)
- Timing Endpoint is working
- Front End data deserialization and alignment is working
- Input spy buffers are working
- Self Triggered mode sender working in simulator + synth + implementation
- 10G Ethernet sender synth + implementation no issues
  - Hardware testing after Clock Generator I2C issue is resolved
- Timing constraints met

DAPHNE V3
PL TOP LEVEL

16 May 2024



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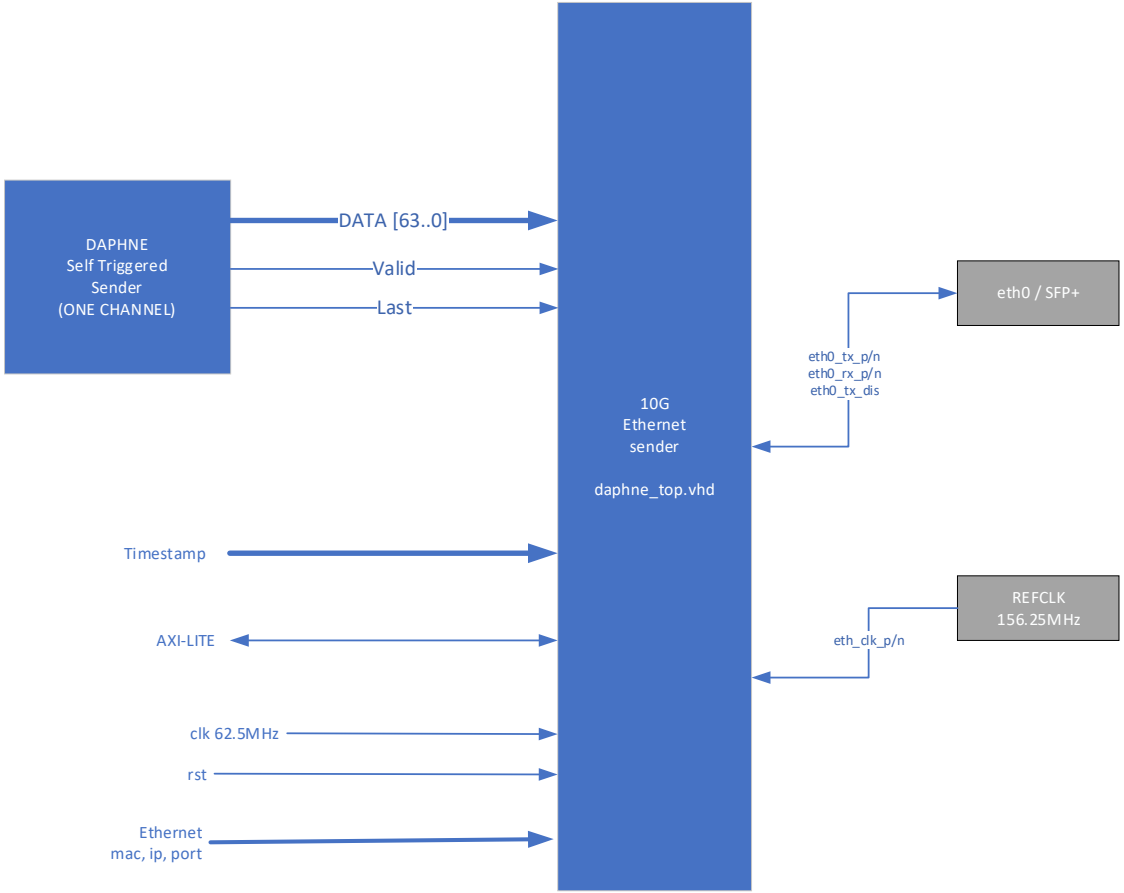
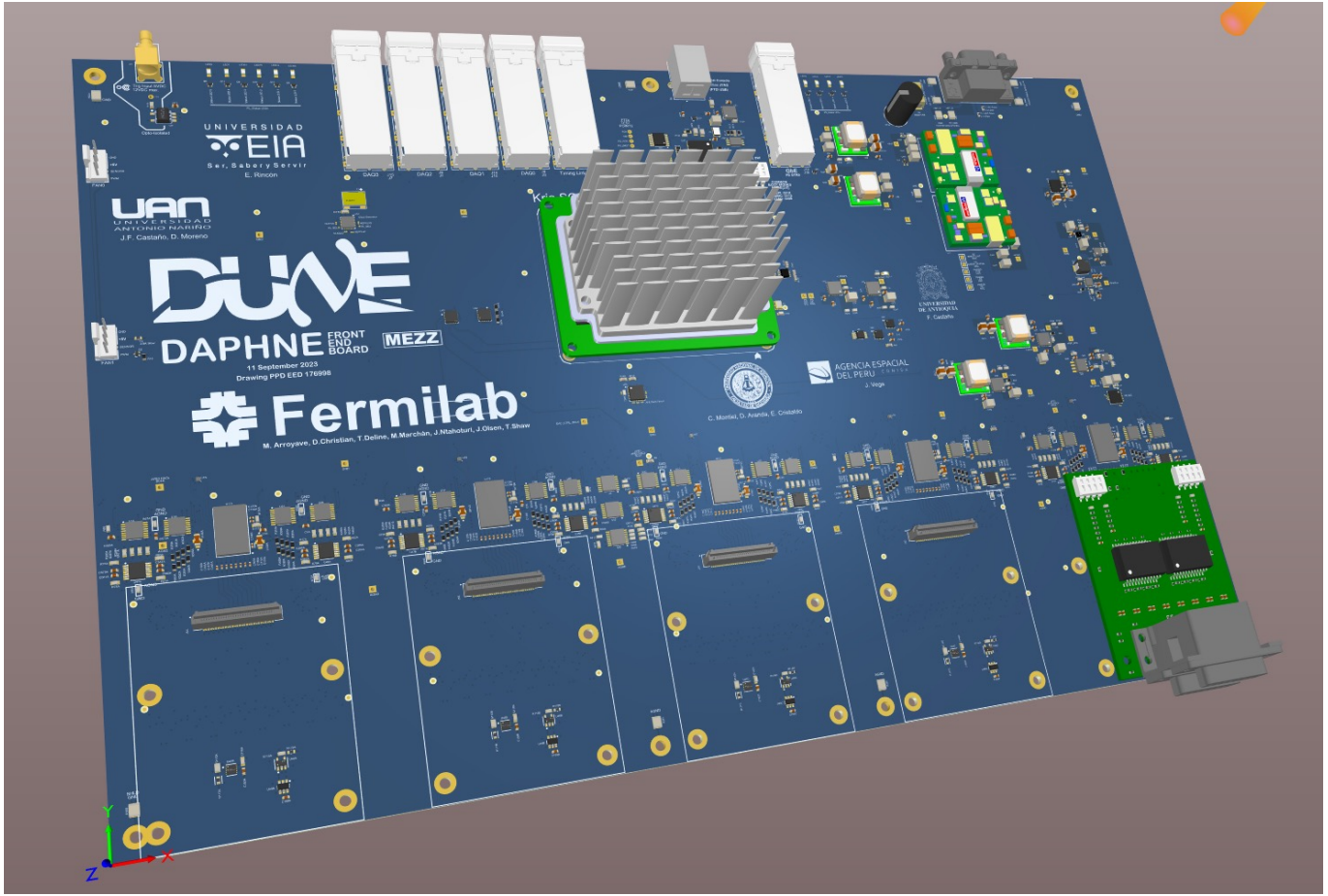

DAPHNE
Self Triggered
Sender
(ONE CHANNEL)
DATA [63..0]
Valid
Last
10G
Ethernet
sender
daphne_top.vhd
eth0 / SFP+
eth0_tx_p/n
eth0_rx_p/n
eth0_tx_dis
Timestamp
AXI-LITE
REFCLK
156.25MHz
eth_clk_p/n
clk 62.5MHz
rst
Ethernet
mac, ip, port

Software Status 1

- On power up Kria loads U-BOOT from QSPI
- U-BOOT then loads Petalinux from EMMC memory
- Problem is U-BOOT is configured to assign a random Ethernet MAC address every time it starts
  - We need static MAC address to get on the CERN network
  - Cannot currently over-ride this and set a static MAC address
- Jacques and Tom working on building new U-BOOT image that allows for changes
  - Reprogram QSPI via JTAG cable and go

Software Status 2

- 10G Ethernet sender firmware requires software to configure it
  - IP Bus commands over the network
- This software runs on the Kria PS processor
- Software builds OK
- Very similar to WIB interface
- Working with Adam Barcock @ STFC UK


UNIVERSIDAD EIA
Ser, Saber y Servir
E. Rincon
UAN
UNIVERSIDAD ANTONIO NARIÑO
J.F. Castaño, D. Moreno
DUNE
DAPHNE FRONT END BOARD MEZZ
11 September 2023
Drawing PPD EED 176998
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X
Z

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