Digital Readout: From VD to FD3 (Status update)

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APEX biweekly working group meeting

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Update from last year

- Slides from the DUNE FD3 Mini-Workshop on June 27, 2023, with notes in red where recent progress has been made.

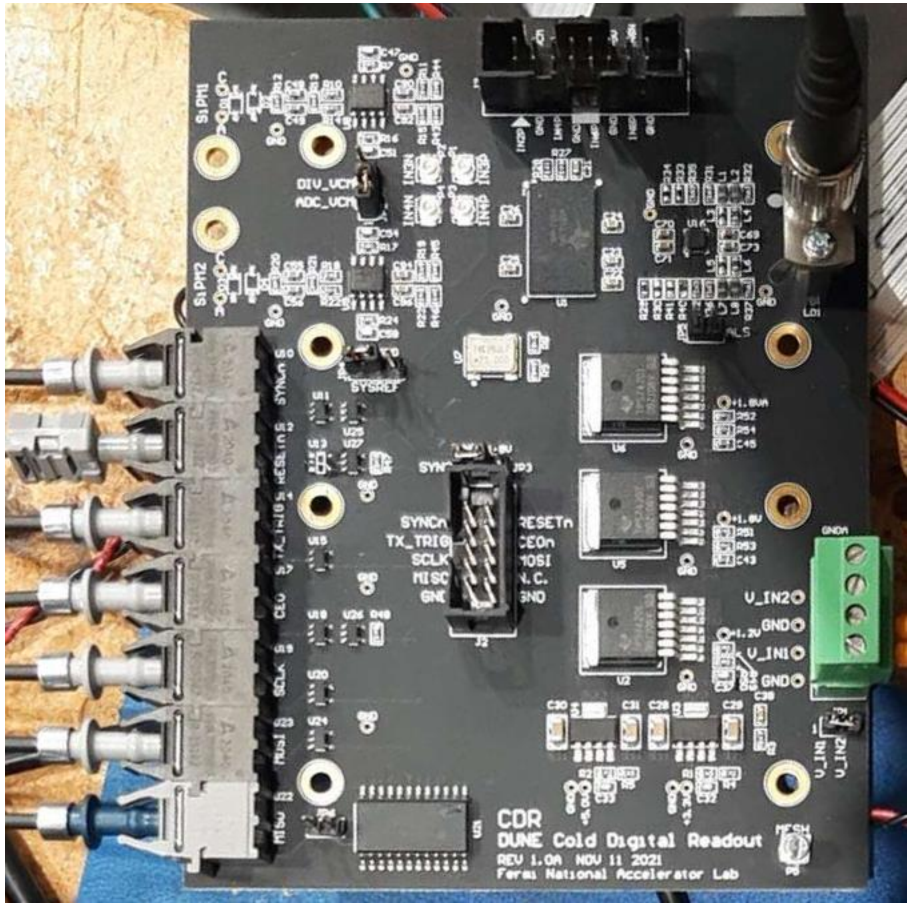
Cold Digital Readout Concept

Objective: Low part-count digital ADC solution compatible with cryogenic operation.

Cold Digital Readout Operation

1. A single low-power ADC clocked by a free-running oscillator continuously digitizes multiple input-channels.
2. The samples are transmitted over a single optical fiber using the deterministic-latency JESD204B subclass 2 protocol.
3. An FPGA in the warm recovers the transmission/sampling clock and decodes the samples for multiple digitizers.

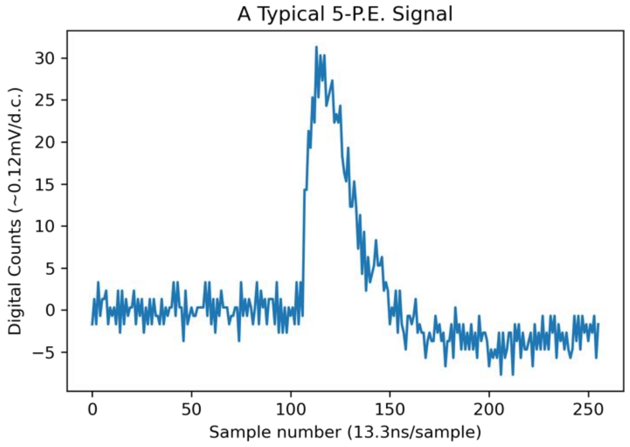
- A thought: Continuous digitization has a relatively flat power draw, which is a good match for power over fiber. Triggered processing at the edge does not pay off as well here.

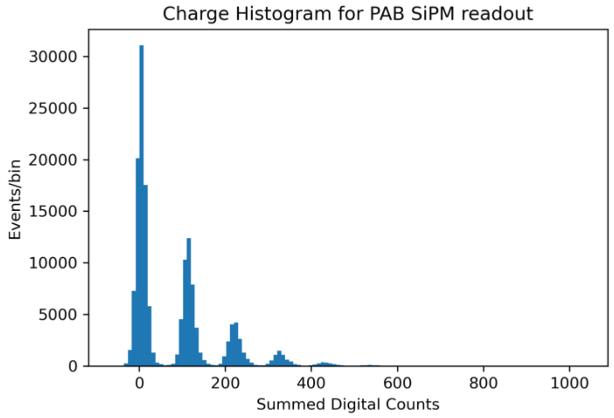


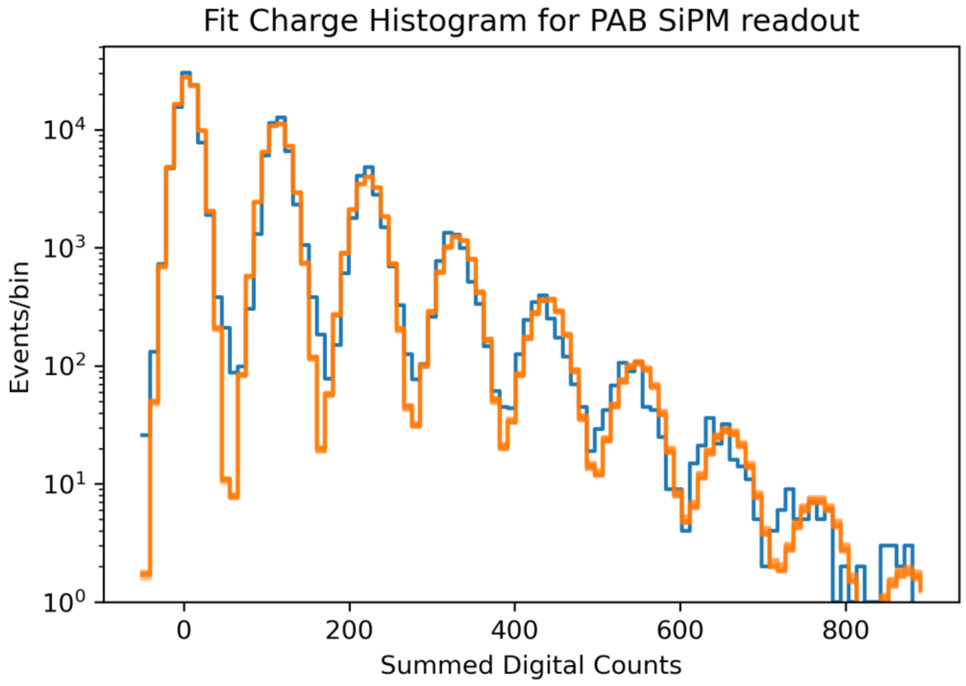
Cold Performance at Fermilab

- 14-bit digitization at 75MHz, (slightly outside of the datasheet specification)
- The Cold Digital Readout board operates reliably at both lab temperatures and in liquid Argon/Nitrogen without any configuration changes.
- **Fitting the charge spectrum with a combined Poisson and SiPM crosstalk model allows measuring the crosstalk probability directly.**
  (Can measure based on the dark-noise spectrum alone)

Best fit results
Pedestal: 5dc
Pedestal RMS: 11.2dc
SPE: 109dc
SPE RMS: 7.7dc
Average SPE/trigger: 0.59
Crosstalk Probability: 0.15



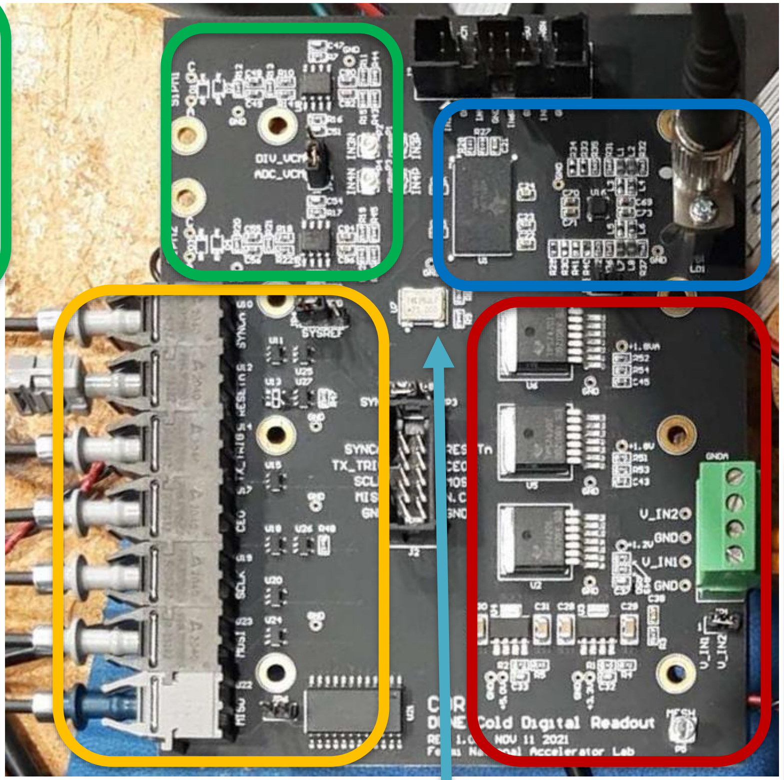




Prototype overview (Version 1, for reference)

Analog front-end
X10 gain, copied from analog design
Could use multiple gains.

Control and timing
LED-based signaling over plastic optical fiber, stable at DC levels and multiple MHz in liquid argon.



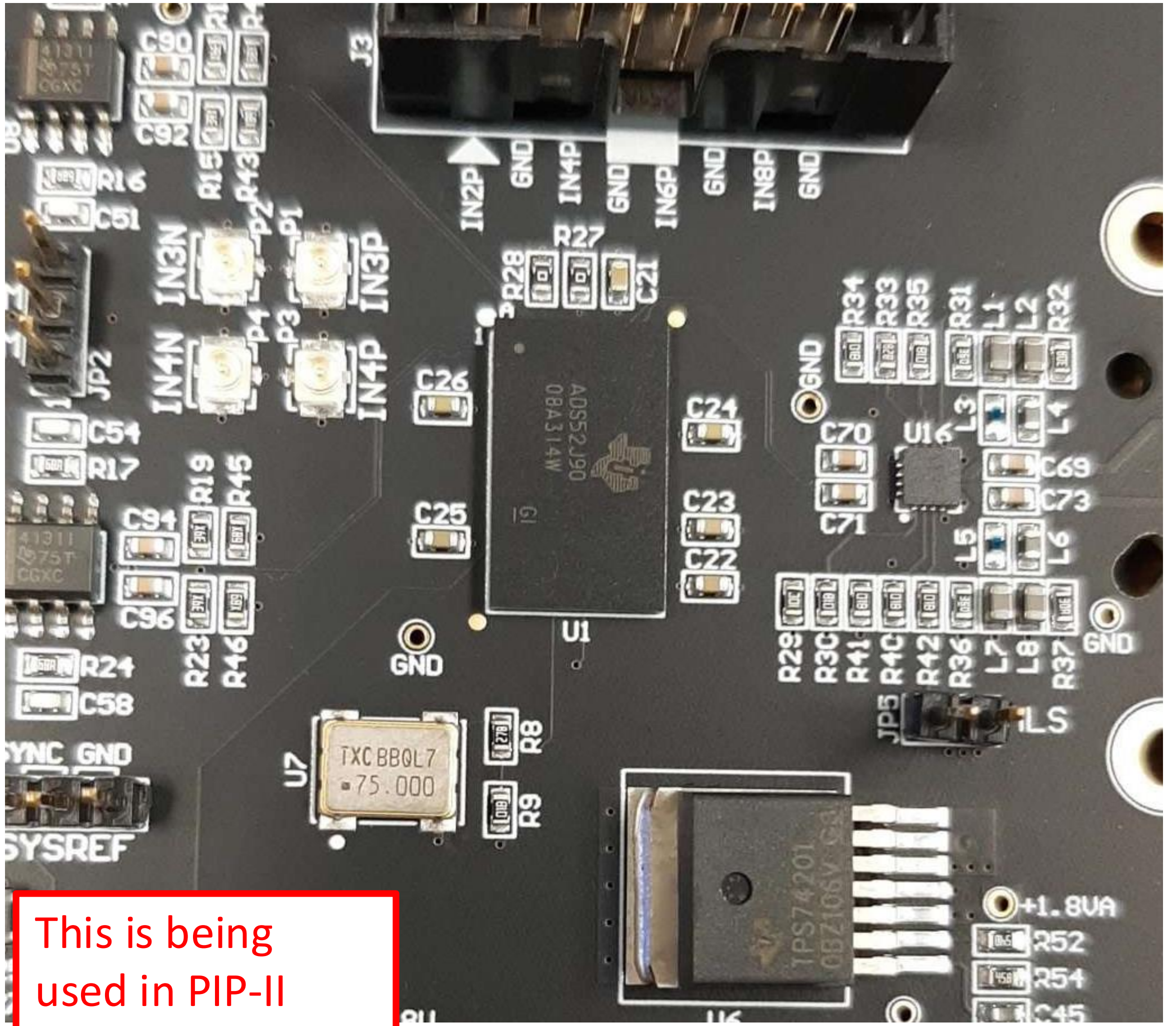
75MHz free-running crystal oscillator with CMOS output.

ADC and Laser Driver
Unique to this design (laser diode shared with analog design)

Power
Linear regulators chosen from existing cryo designs.
5V (Analog front end and controls)
3.3V Laser driver and Oscillator
1.8V digital and analog for ADC

ADC Chip

- Version 1: TI ADS52J90
  - 14-bit 16-channel ADC with 5Gbps JESD204B serial output
  - Chosen from experience with cold operation in LBNL-Fermilab CryoDAQ targeting Liquid He operation.
  - Supports up to 32 differential input channels (configurable) over 2 fibers
  - Total power ~30mW/ch at 40MSPS (16ch) Requires 2 fibers.
- Version 2: ADI AD9656
  - 16-bit 4-channel ADC with 8Gbps JESD204B serial output
  - Successfully tested in Liquid Argon at Fermilab.
  - Defaults to 4-channels over 1 fiber at startup, only requires standard JESD204b signals.
  - Total power as low as 100mW/ch at 40MSPS (per datasheet)
- So far untested: TI ADS52J65
  - 16-bit 8-channel ADC with 12.8Gbps JESD204B serial output
  - 38mW/ch at 40MSPS (8-ch). Would only require 1 fiber.
- Best efficiency when many channels can be utilized.

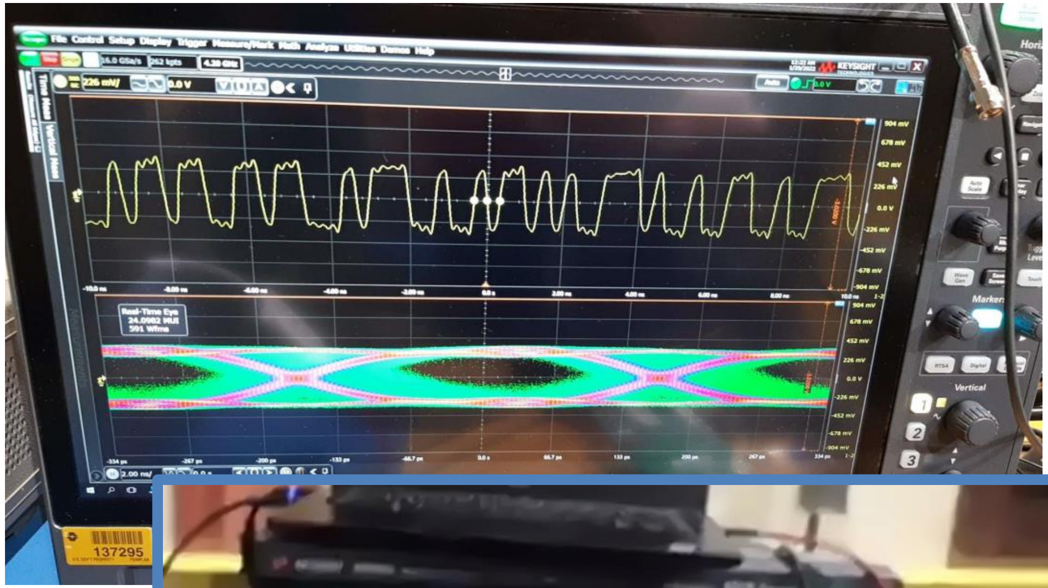


This is being used in PIP-II MPS, on my desk now.

Laser and Laser Driver

- Laser bias and modulation settings optimized and set with onboard resistors.
- Reliable operation at 5gbps (higher datarates not yet tested)
- FC coupled lasers worked in shallow liquid argon, but quickly flooded.
- “Sealed” pigtail lasers operated at depth in liquid argon, but eventually flooded.
- New, “unfocused” lasers available to solve the flooding problem.
- Signs that the laser driver can operate reliably at lower voltages.

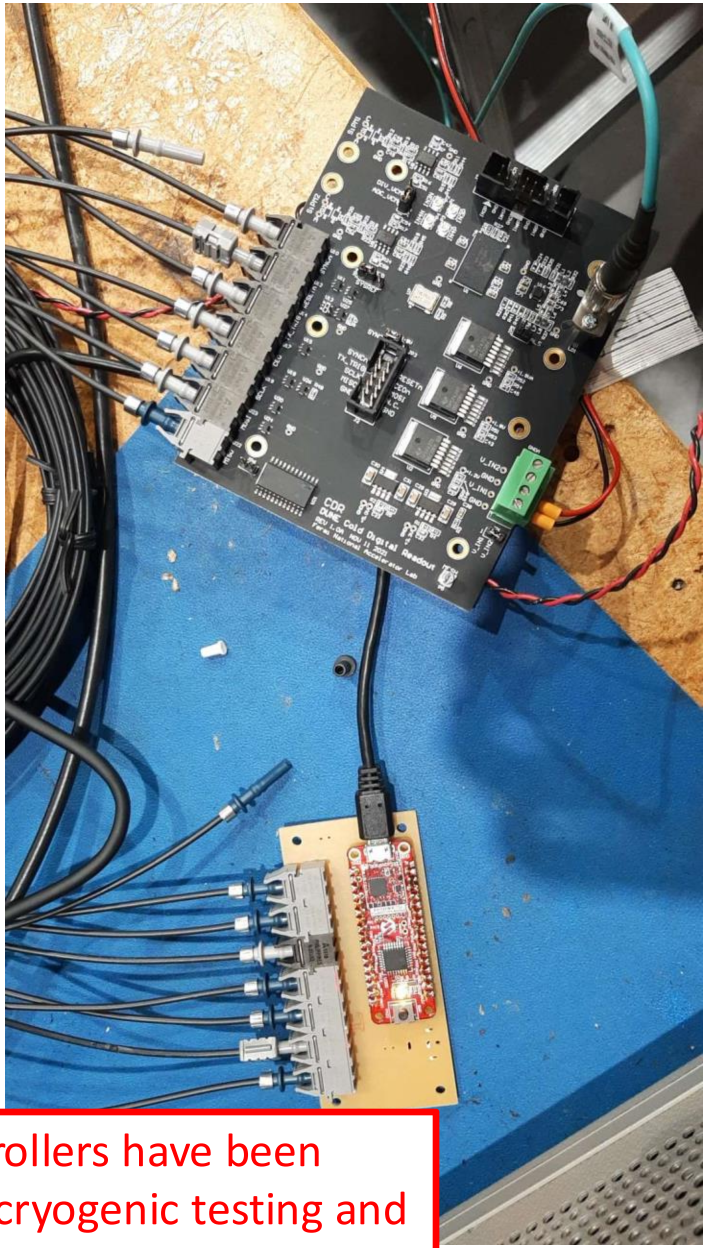
Before optimizing:



After optimizing:
(3gbps)

Control signals

- ADS52J90 ADC requires several registers to be configured and multiple reset and sync signals. Prototypes used plastic optical fibers with LED transmitters.
- Two prototypes deployed to the coldbox at CERN.
- Both prototypes had significant issues with the optical slow-control fibers.
  - Difficult to keep track of 7 identical fibers through the cryostat penetration.
  - The requirement of being able to send DC signals (active high reset, resynchronization signal, etc.) meant using receivers sensitive to DC light levels, so termination and coupling problems caused communications failures.
- An onboard active controller device (ASIC, FPGA, Microcontroller) would greatly simplify the design, eliminating the need for most control.



5 Microcontrollers have been selected for cryogenic testing and we have the test PCBs for 3 of them in hand.

Power delivery

- Existing designs used:
  - 5.0V for Analog front end opamps
  - 3.3V for laser driver
  - 1.8V supplies for analog and digital ADC.
- PoF supplied ~6V, so >2/3 of the power was lost to the linear power regulars.

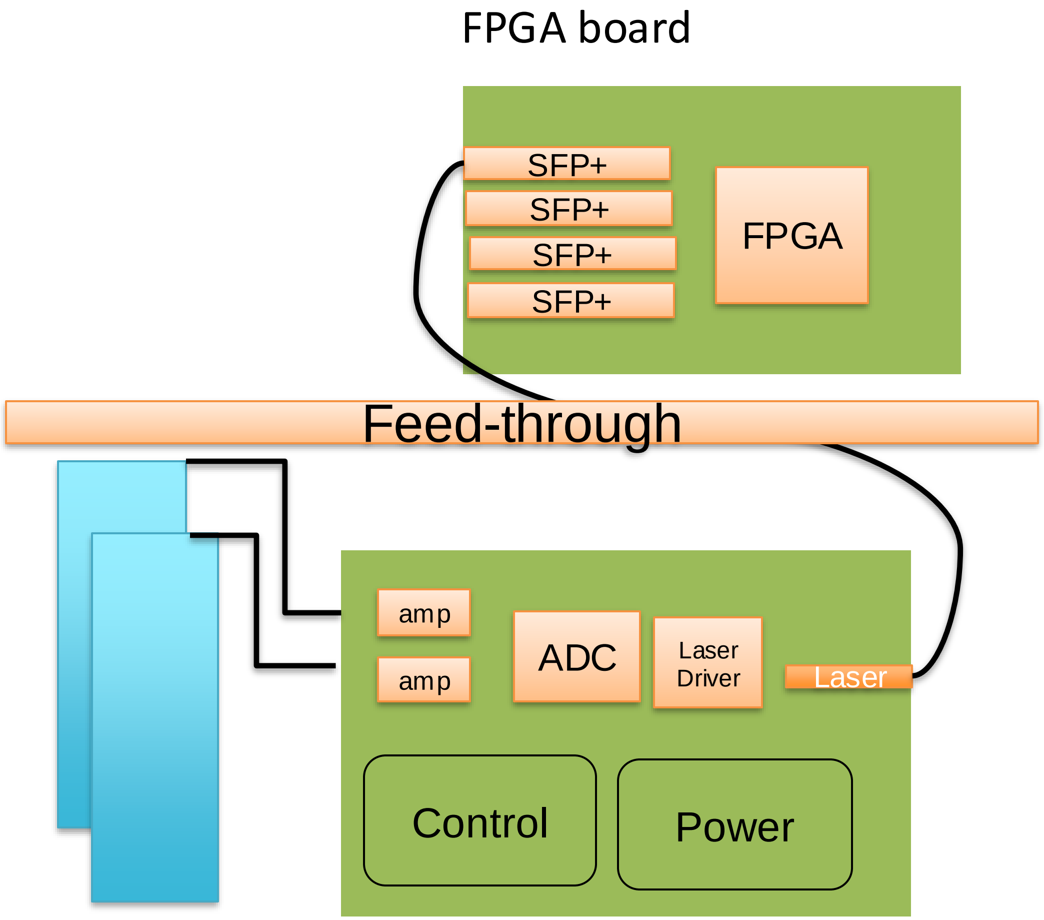
Next Steps:

- Immediately available:
  - New ADC available: TI ADS52J65, lower total power and reasonable channel count. ADCs being tested, need to plan cryogenic testing.
  - New laser available: Test the new unfocused laser diodes The work done for Analog readout can be dropped in
- Straightforward:
  - Improve efficiency of voltage regulation, perhaps with switch-mode regulators.
  - Optimize power of analog front end.
  - Could use an ADC channel to monitor input voltage modulate the input Power over Fiber.
- Needed:
  - Simple automatic or remotely-controllable configuration (FPGA, ASIC or microcontroller). First testing in the next couple weeks.
  - May want to provide external clock to simplify operation.
- The big questions:
  - Can we make use of multiple ADC channels to make the power/channel competitive with FD2 analog designs? There have been recent discussions about how to best use ~16 channels.
  - Does digital signal transmission provide a benefit that isn't otherwise available?

Backup slides

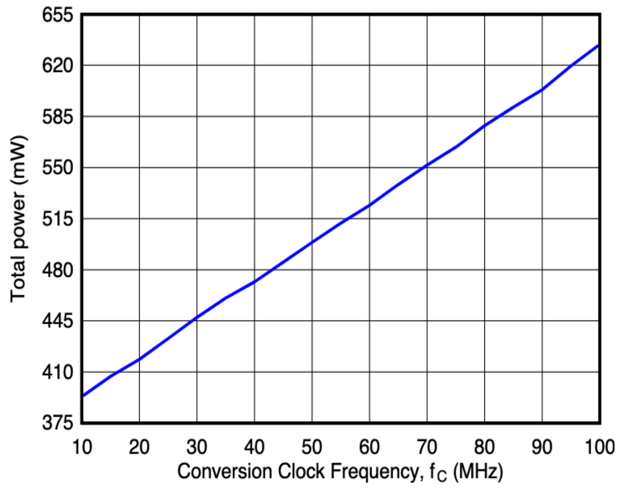
Digital readout concept

- Minimal digital electronics in the cold to minimize analog conversation steps.
- Flexible choices for input/output channels.
- Simplified electronics outside the cryostat (only digital)
- Analog front-end amplifier/filter and Power over Fiber same as analog design
- Laser Driver and laser tested working at 5Ghz
- Control over Plastic Optical Fiber with LED based transmitters/receivers
- Free-running crystal oscillator



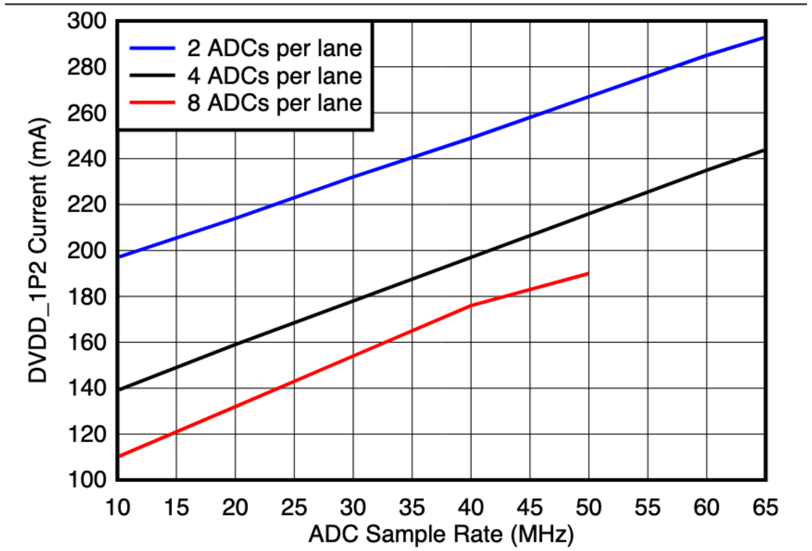
Additional plots from ADS52J90 Datasheet

CURRENT CONSUMPTION WITH JESD INTERFACE ENABLED				
I_{JESD}	Supply currents: JESD204B interface enabled, LVDS interface disabled at 12-bit, 80-MSPS, 4 ADCs per lane mode	AVDD_1P8 current(1)	170	mA
		DVDD_1P2 current(1)	260	
		DVDD_1P8 current(1)	40	
P_{JESD_CH}	Power dissipation in active mode per input channel: f_C = 80 MSPS, 12-bit mode, LVDS interface disabled, JESD interface enabled (4 ADCs per lane mode)	16-channel input mode	43.1	mW/channel
		32-channel input mode	21.6	



32-input mode, 10-bit resolution

Figure 36. Total Power vs Conversion Clock Frequency



ADC resolution = 14 bits, across lane modes

Figure 46. DVDD_1P2 Current vs ADC Sample Rate

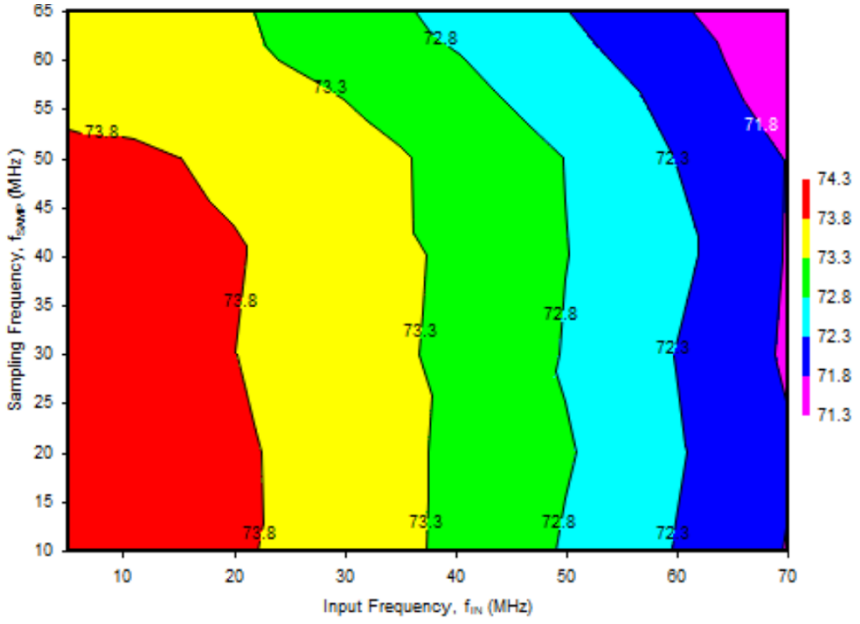


Figure 54. Signal-to-Noise Ratio in 14-Bit, 16-Input Mode

Fermilab DUNE