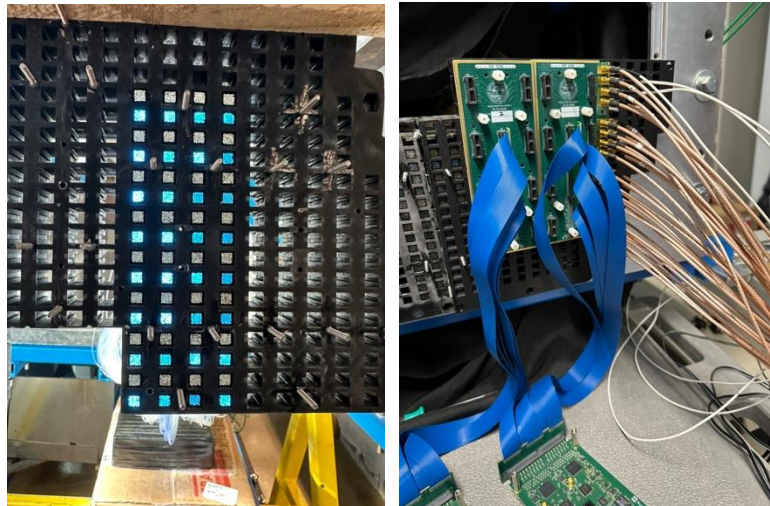
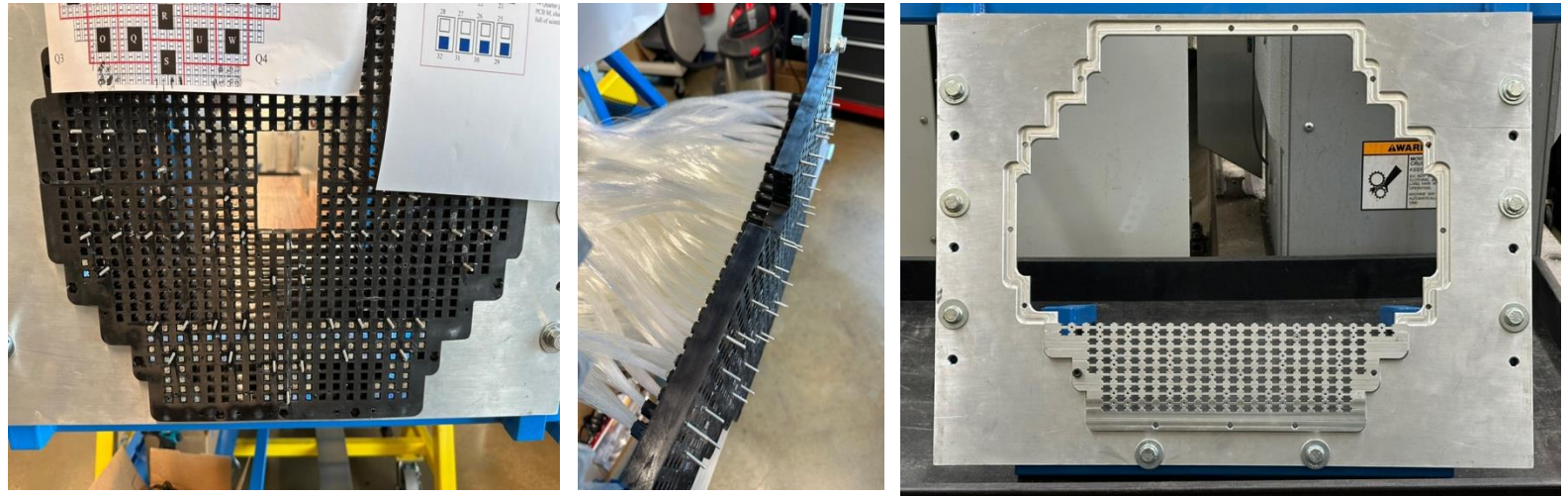


TTU Update

N. Akchurin, H. Brittan, J. Damgov, X. Delashaw, Yongbin Feng, M. Harris, M. Kelley, S. Kunori, C. Madrid, M. O'Donnell, T. Peltola, O. Schneider, C. Tidomore,, G. Vettters

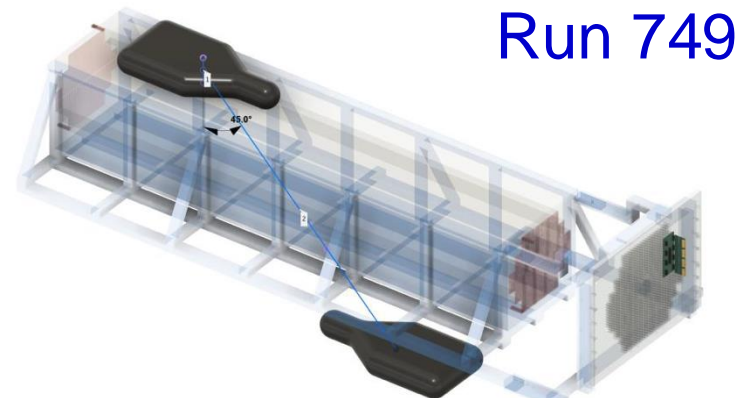
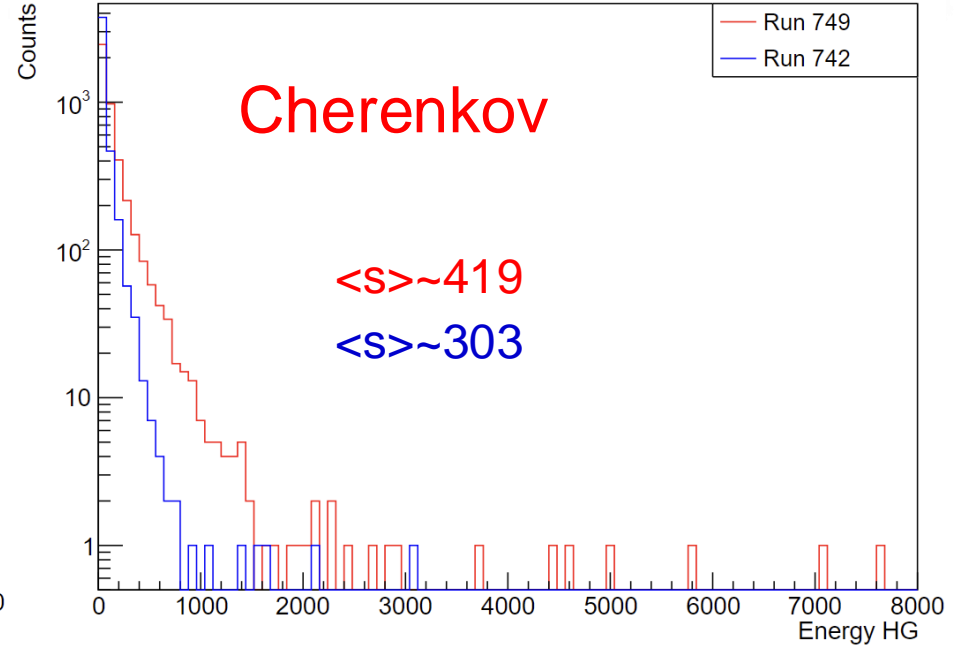
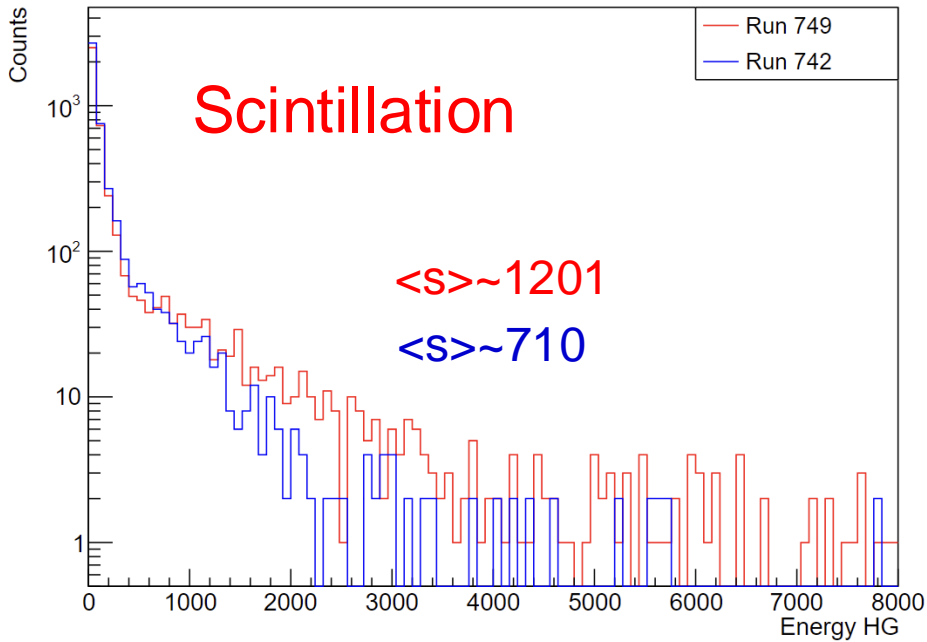
Reconstruction of HG-DREAM

The reconstruction of the module is continuing. The aluminum endplate is being machined (not 3D printed)

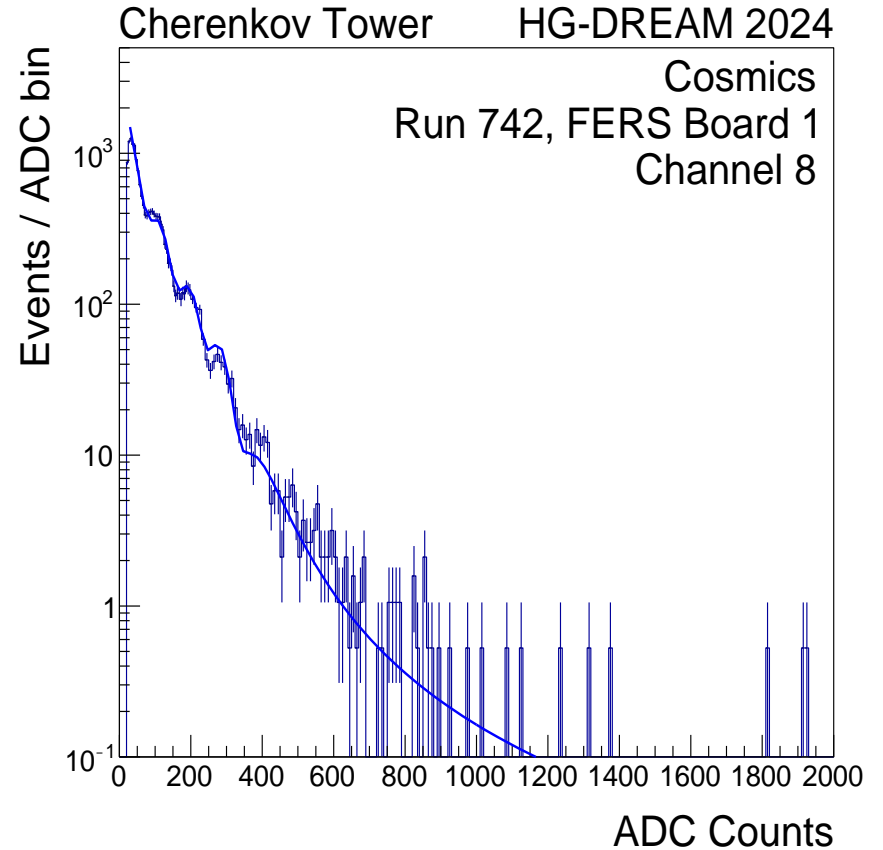
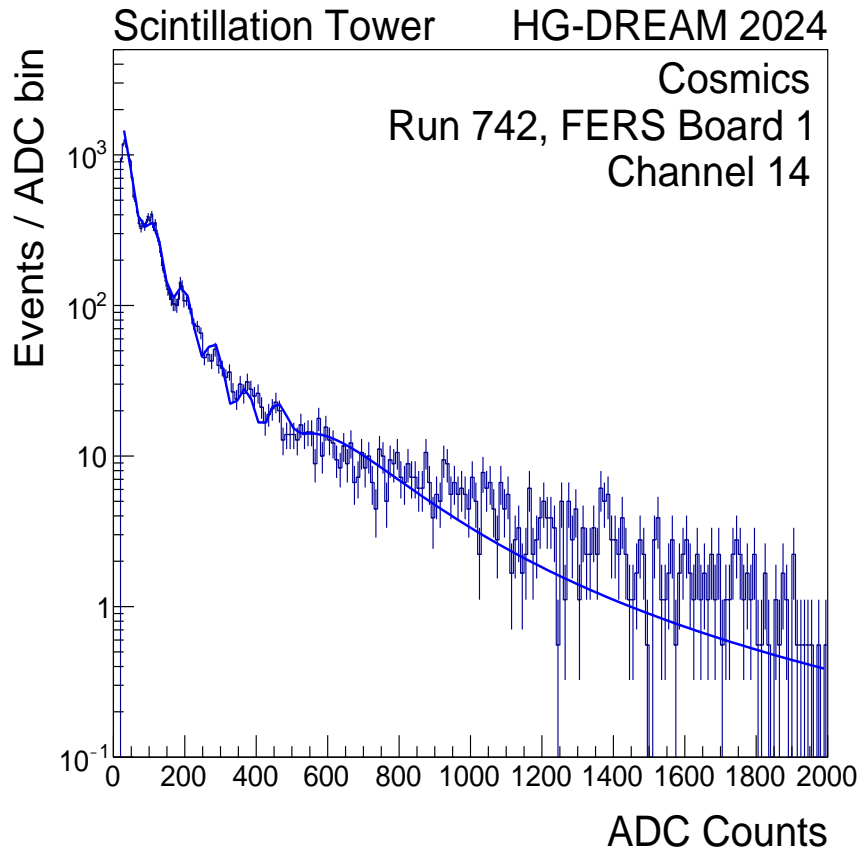


We continue to perform tests using partial optical and readout systems

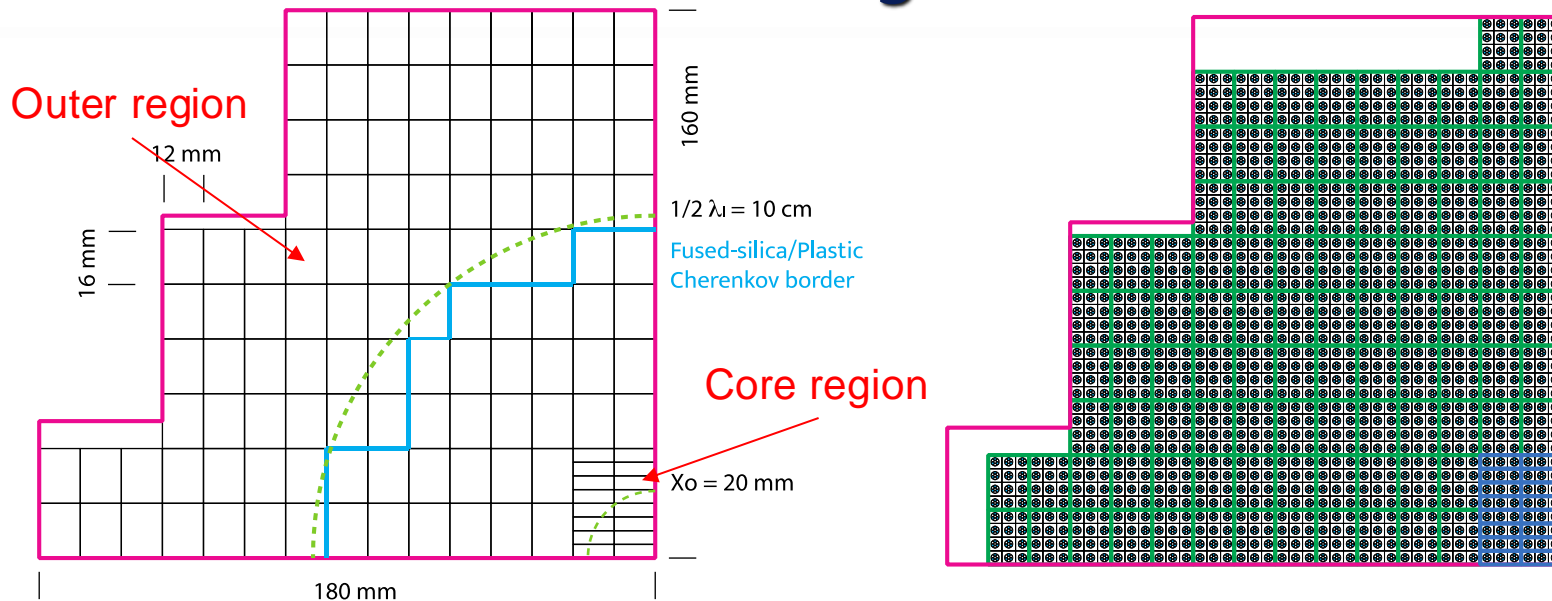
Cosmic Muon Runs - I



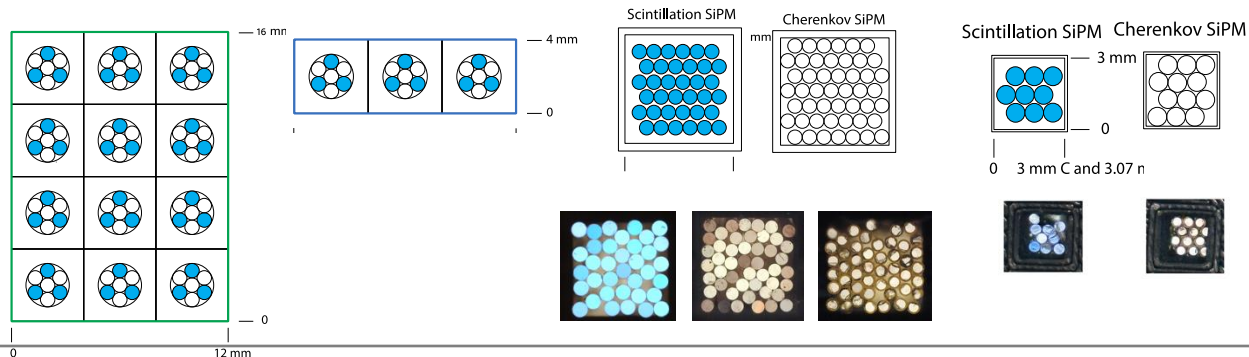
Cosmic Muon Runs - II



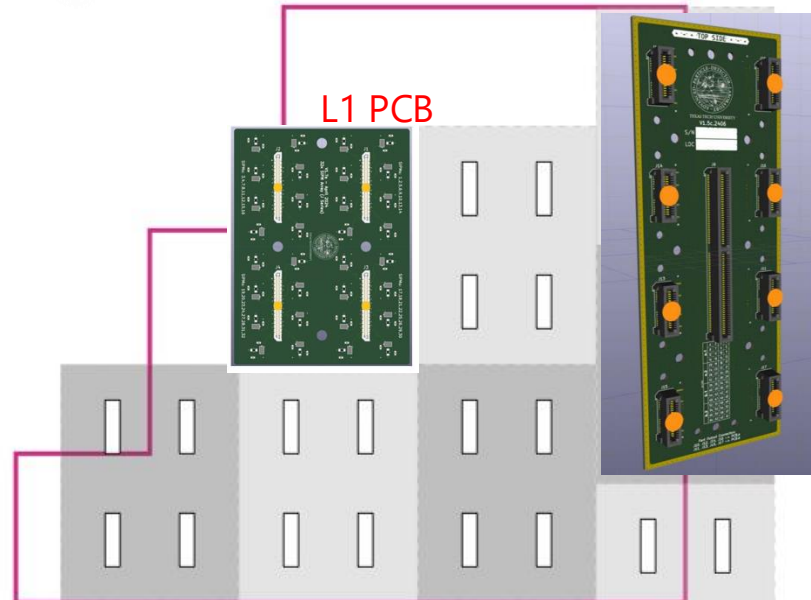
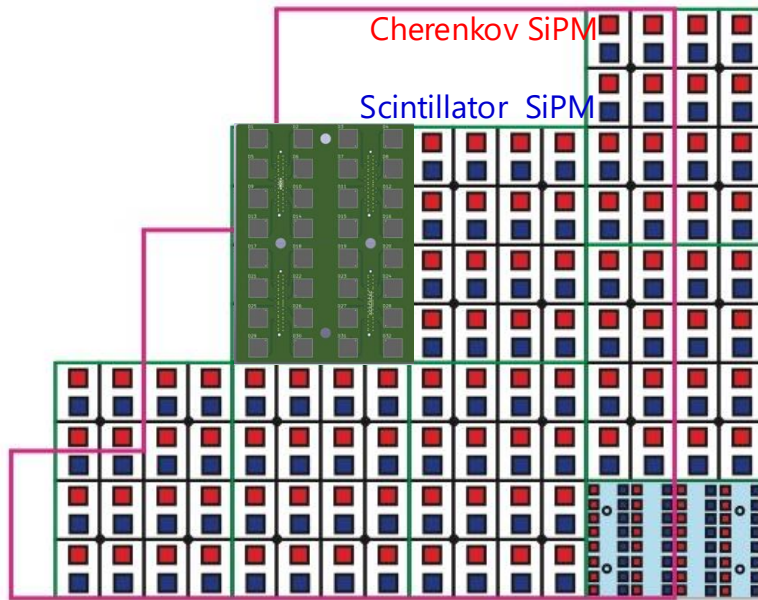
HG-DREAM Segmentation - I



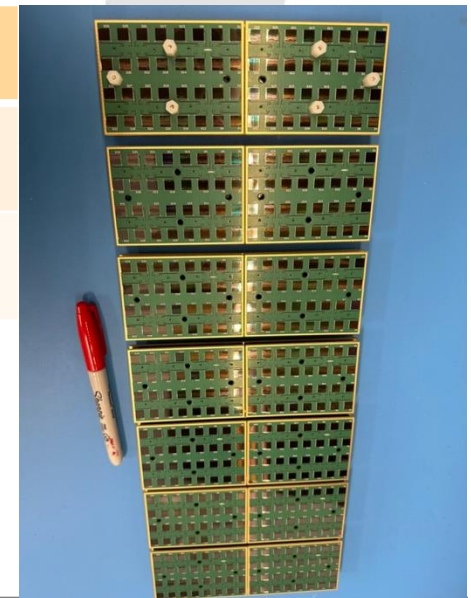
	Tower size (mm ²) (No of rods)	No. S/C fibers	SiPM area (mm ²)	No. of units
Outer region	12x16 (12)	36 S, 48 C	6x6	440
Core region	12x4 (3)	9 S, 12 C	3x3	64



HG-DREAM Segmentation - II



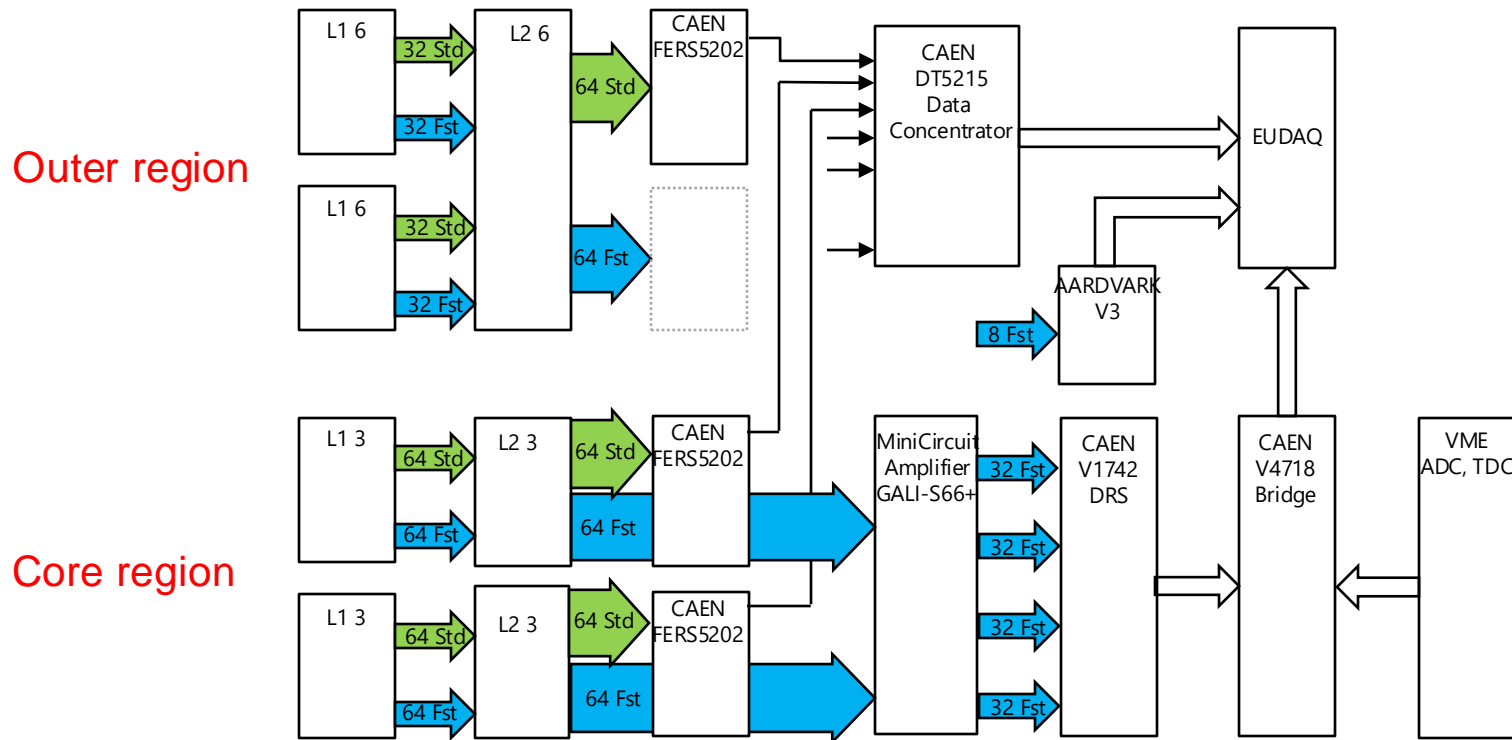
	L1 PCB	No. L1	No. L2	No. of units
Outer region	32 SiPMs	24	12	768 Std (FERS) 768 Fst
Core region	64 SiPMs	2	1/2	128 Std (FERS) 128 Fst (DRS)



L1 PCBs for 6 mm SiPMs are made and 3 mm SiPM design is complete

- Trace lengths are kept short: Std 15-18mm and Fst 6-10 mm (tested coplanar waveguide with ground (CPWG) and strip-lines (buried traces) in 6-layer boards)
- For Std & Bias HSEC8-170-01-S-DV (edge connect to A5202)
- For Fst MMCX Jack (female direct to amplifier or waveform digitizer)

HG-DREAM Readout Configuration

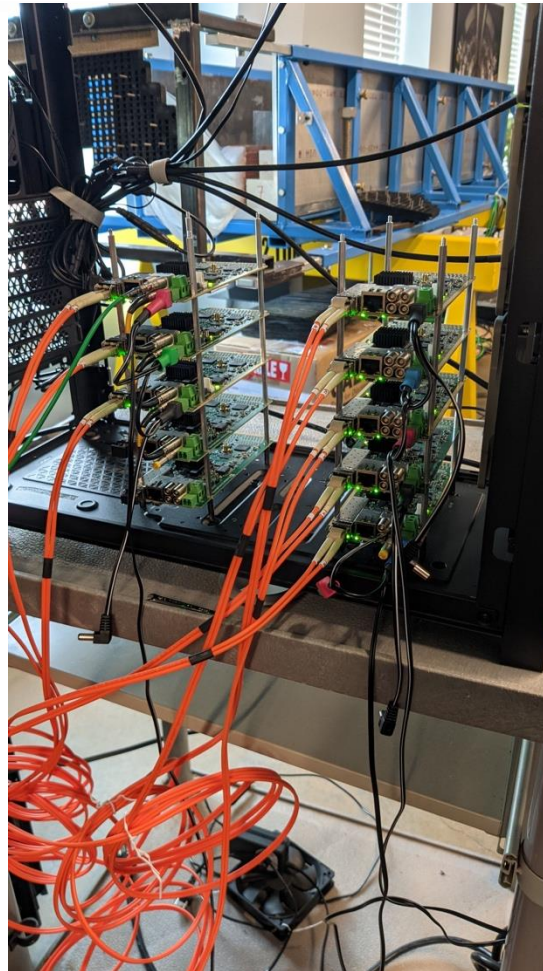
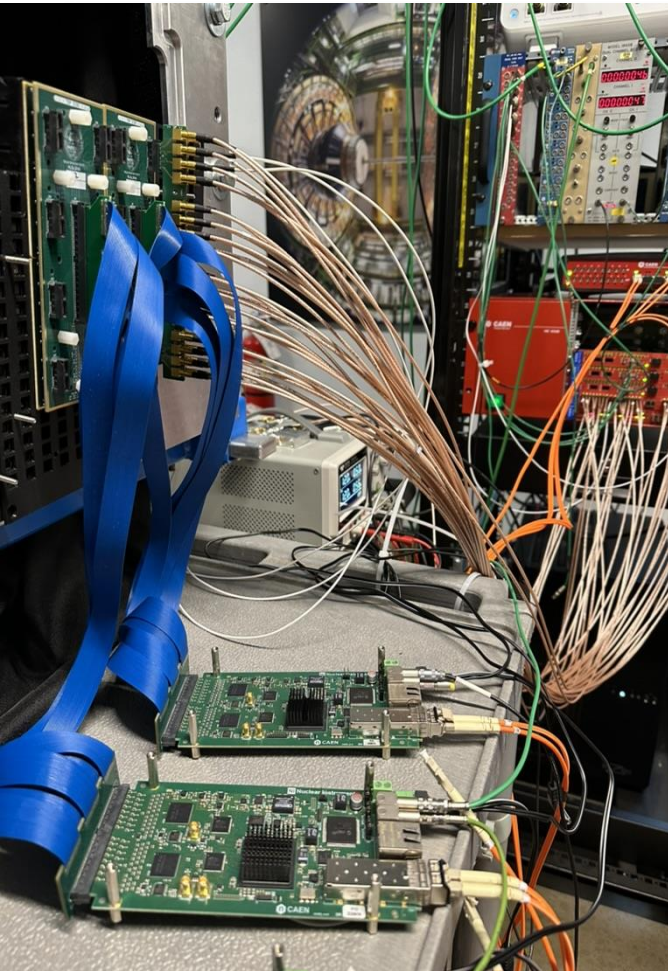


Different types of information from large number of channels need to be integrated and collected in a unified manner (EUDAQ)

Expected data size ~ 220 kB/event for DRS and ~ 1.7 kB/event for FERS

There is much room for data size optimization but need for on-detector processing becomes evident

Progress on DAQ

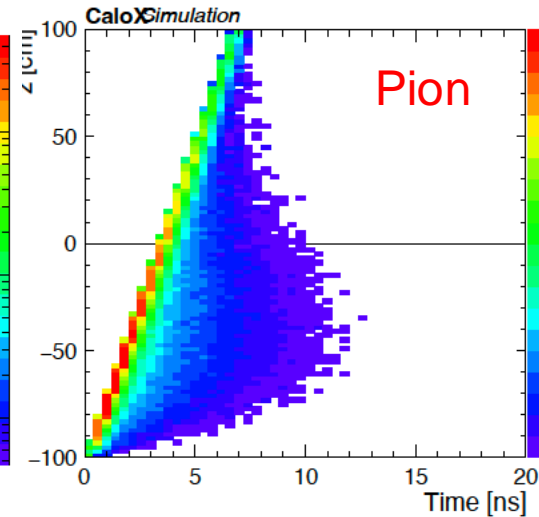
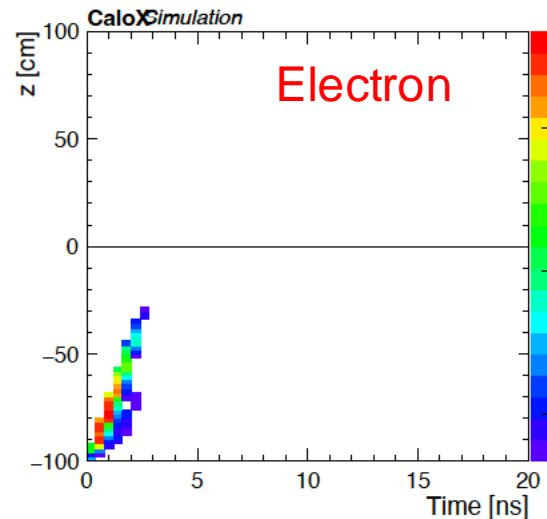
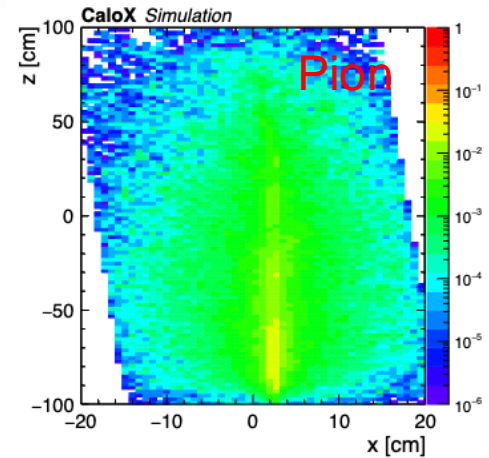
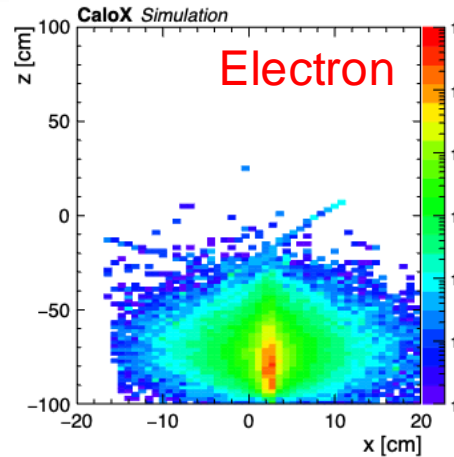
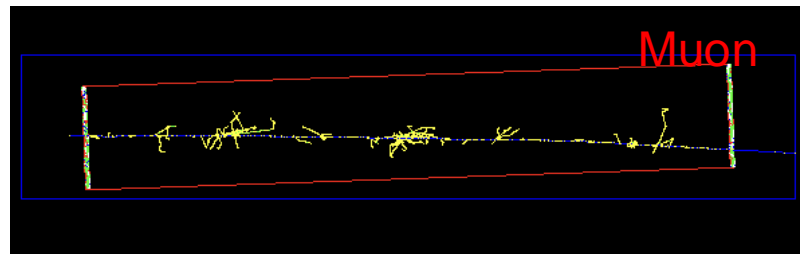
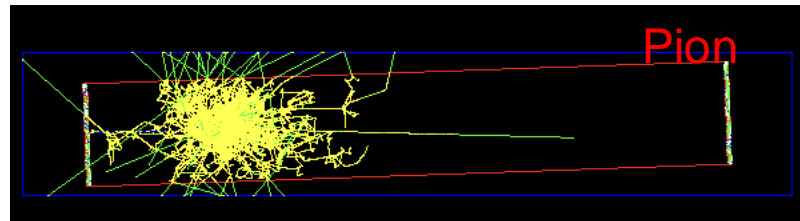
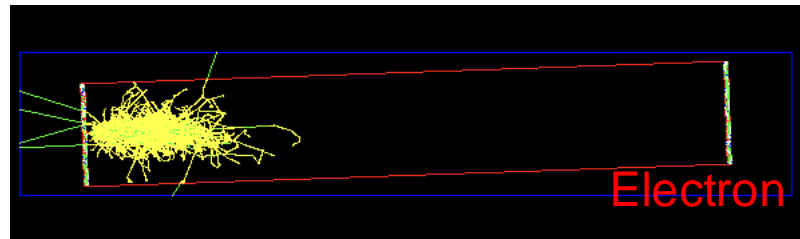


Chain	Status	# Board	RTT	Total Events	Event Rate (Hz)	Bw Usage (Mbps)	Info Buffer	Data Buffer	Enable
0	Running	1	358.4	0.0000e+0	0 Hz	0 bps/3 Gbps	0%	0%	<input checked="" type="checkbox"/>
1	Running	1	377.6	0.0000e+0	0 Hz	0 bps/3 Gbps	0%	0%	<input checked="" type="checkbox"/>
2	Running	1	377.6	0.0000e+0	0 Hz	0 bps/3 Gbps	0%	0%	<input checked="" type="checkbox"/>
3	Running	1	364	0.0000e+0	0 Hz	0 bps/3 Gbps	0%	0%	<input checked="" type="checkbox"/>
4	Running	1	371.2	0.0000e+0	0 Hz	0 bps/3 Gbps	0%	0%	<input checked="" type="checkbox"/>
5	Running	1	377.6	0.0000e+0	0 Hz	0 bps/3 Gbps	0%	0%	<input checked="" type="checkbox"/>
6	Running	1	377.6	0.0000e+0	0 Hz	0 bps/3 Gbps	0%	0%	<input checked="" type="checkbox"/>
7	Running	1	377.6	0.0000e+0	0 Hz	0 bps/3 Gbps	0%	0%	<input checked="" type="checkbox"/>

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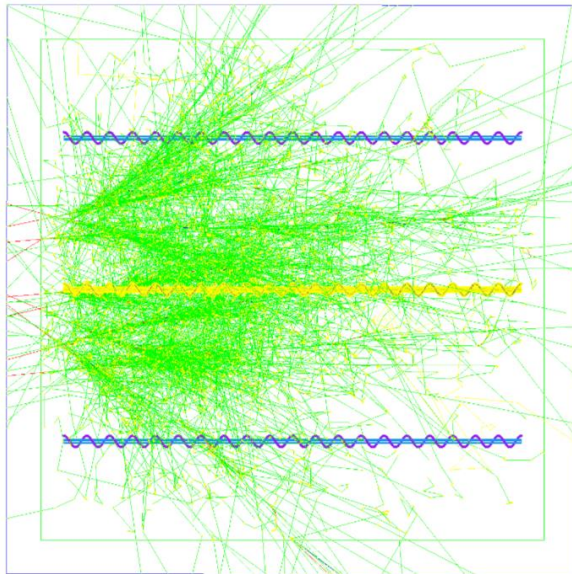
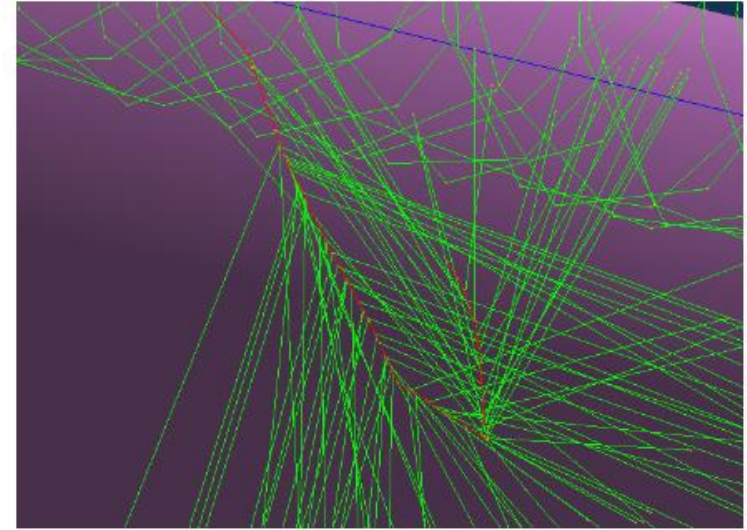
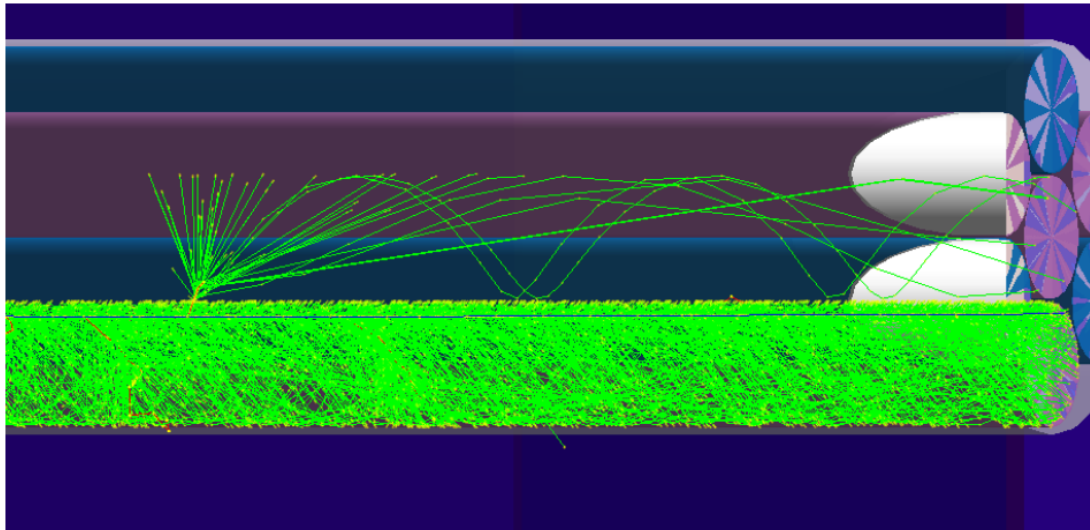
We were able to run 8 FERS. Occasionally, event synchronization fails. Investigating. We plan to have 14 FERS and 6 DRS boards. No issues with integrating DRS modules.

Simulation Studies - I



HG-DREAM simulation effort is progressing well. The basic sanity checks are being made. Results on timing and reconstruction algorithms will come soon

Simulation Studies - II



We explore conventional as well as unconventional fibers, e.g. sapphire, double-clad, helical, etc and will embed them in HG-DREAM for feasibility tests