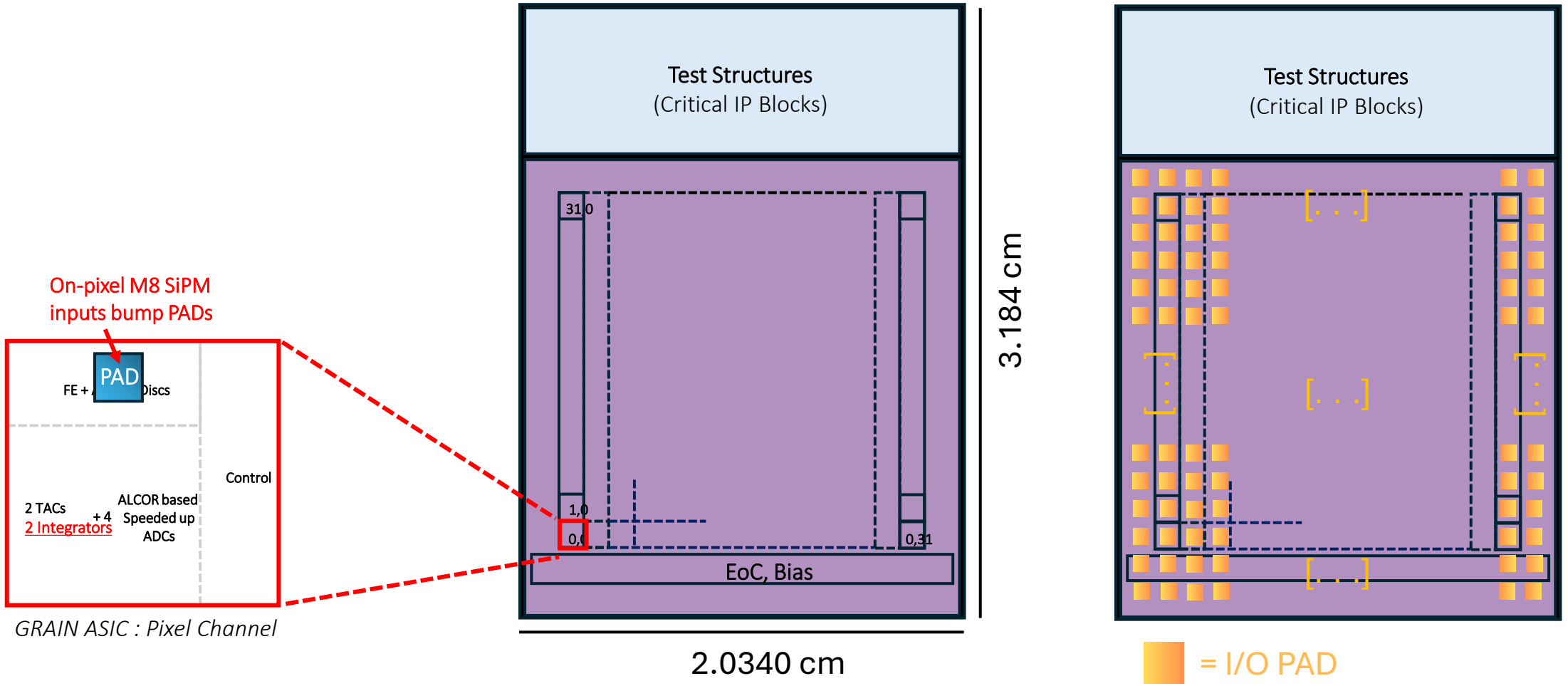
Investigating a Low Noise, Compact Integrator with super-600 mV Dynamic Range

Stefano Durando
Sofia Blua, Valerio Pagliarino, Angelo Rivetti

Preliminary!

On-Pixel Integrators



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A CMOS Low-Noise and Low-Power Charge Sampling Integrated Circuit for Capacitive Detector/Sensor Interfaces

Suharli Tedja, Jan Van der Spiegel, *Senior Member, IEEE*, and Hugh H. Williams, *Member, IEEE*

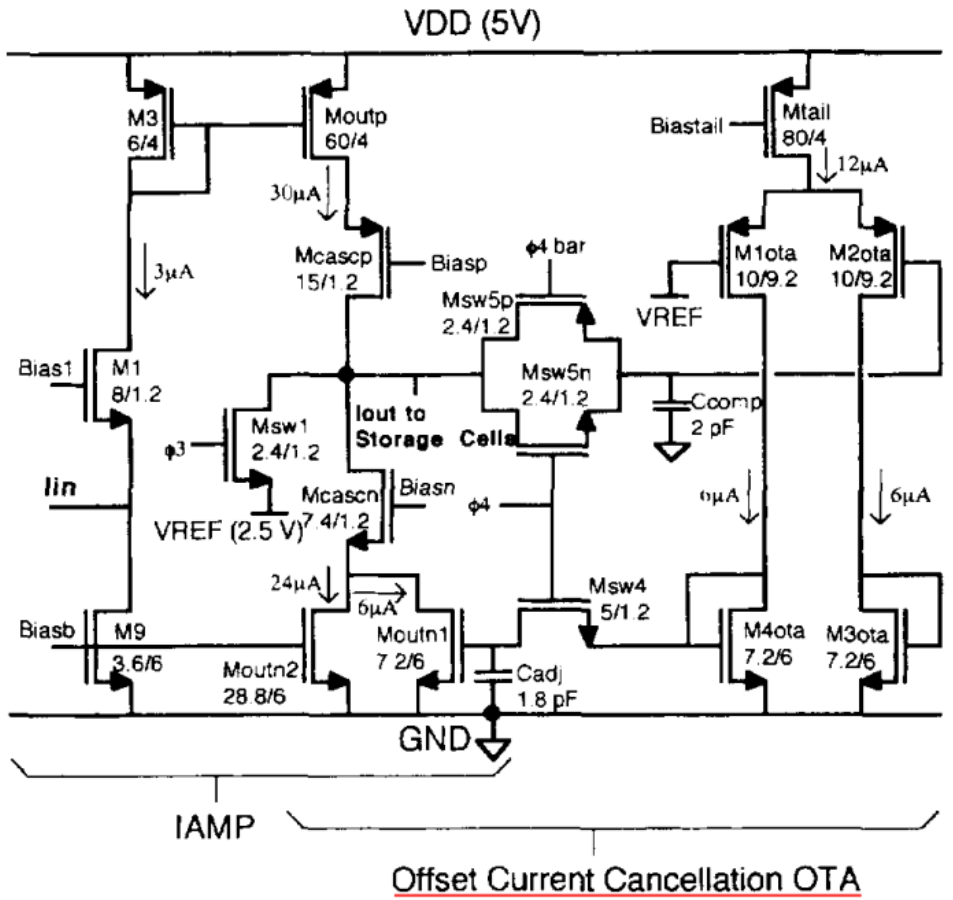

Fig. 4. Schematic of the Current/Charge-Mode Amplifier (IAMP) including the offset-current cancellation circuit.

Full citation: S. Tedja, J. Van der Speigel and H. H. Williams, "A CMOS low-noise and low-power charge sampling integrated circuit for capacitive detector/sensor interfaces," in *IEEE Journal of Solid-State Circuits*, vol. 30, no. 2, pp. 110-119, Feb. 1995, doi: 10.1109/4.341737. keywords: {Sampling methods;CMOS integrated circuits;Electrons;Detectors;Capacitive sensors;CMOS analog integrated circuits;CMOS digital integrated circuits;CMOS technology;Sensor phenomena and characterization;Analog integrated circuits},

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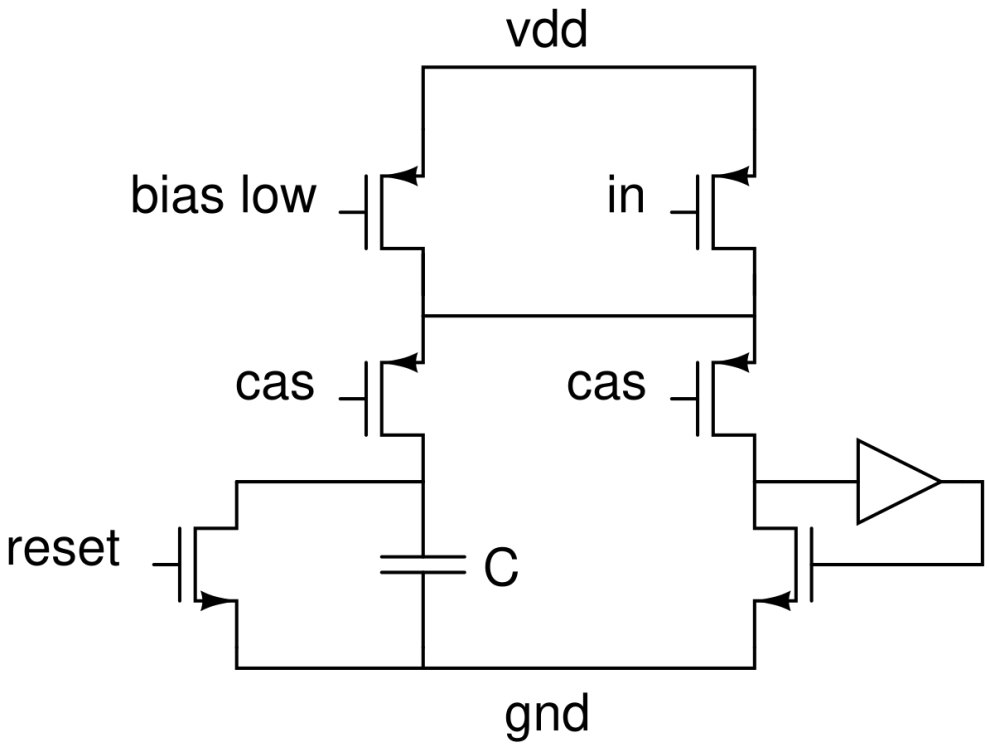
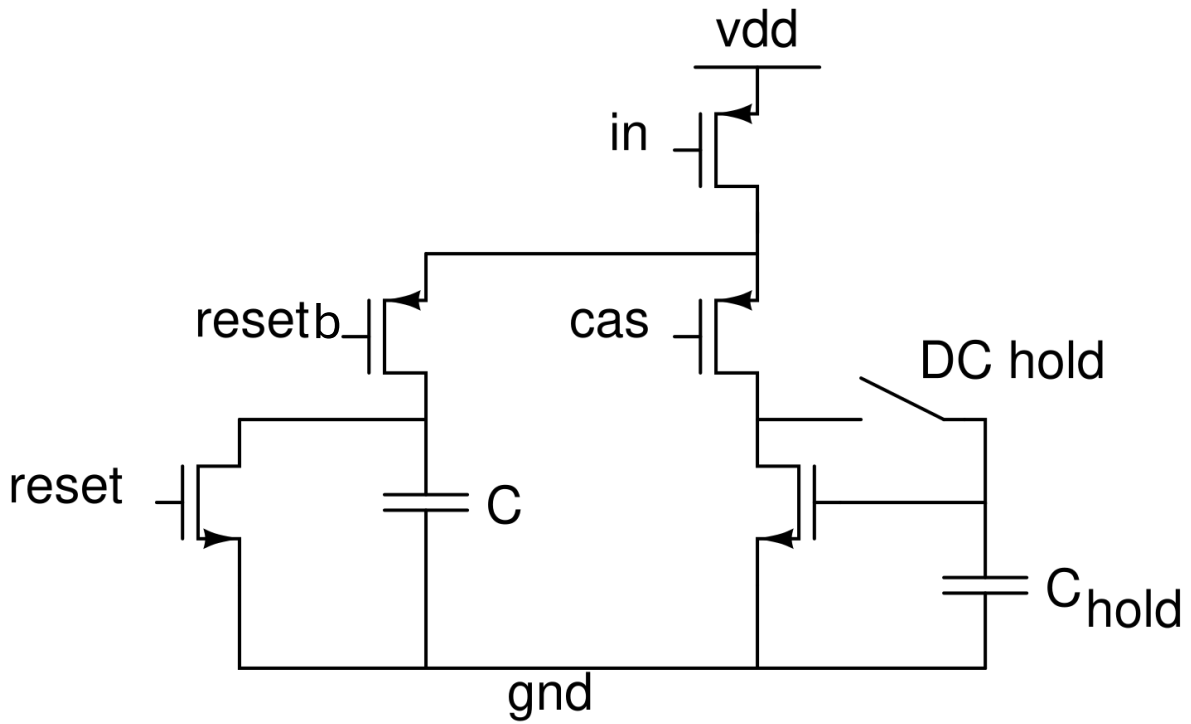
Continuous Time



Discrete Time



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