Progress of the GRAIN Working group

Conveners: Lea Di Noto – Univ. and INFN Genova
Alessandro Montanari- INFN Bologna

SAND Technical meeting,
Oct, 22th 2024

Overview

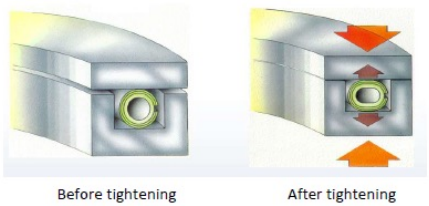
- This talk will cover the main progress in:

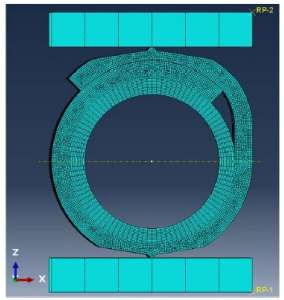
  - Mechanics

  - ASIC design

Inner Vessel

- Helicoflex simulation completed
  - Not reusable
  - Cost of 1 gasket ~ 5000 Euro

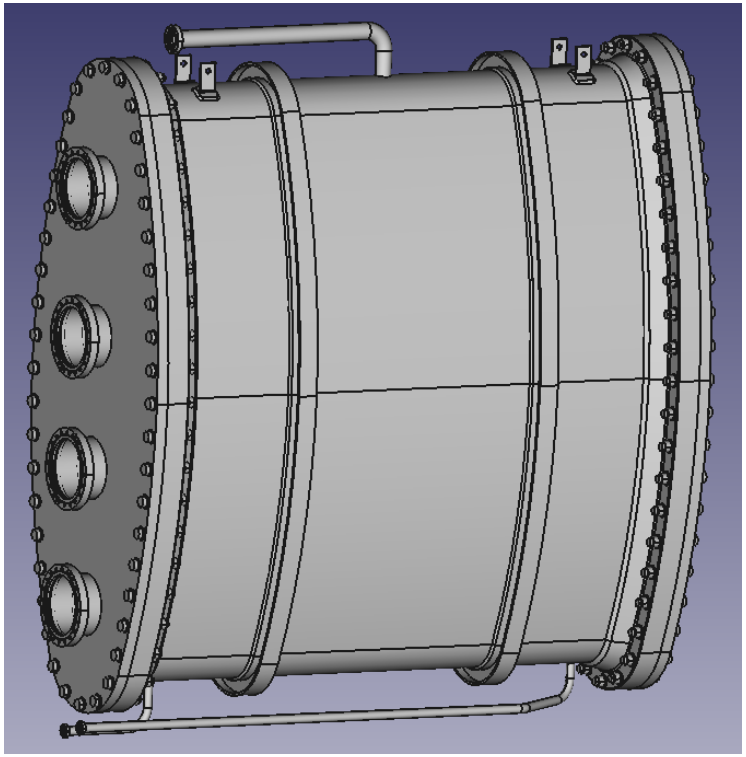




- Full vessel simulation and certification by end of the year

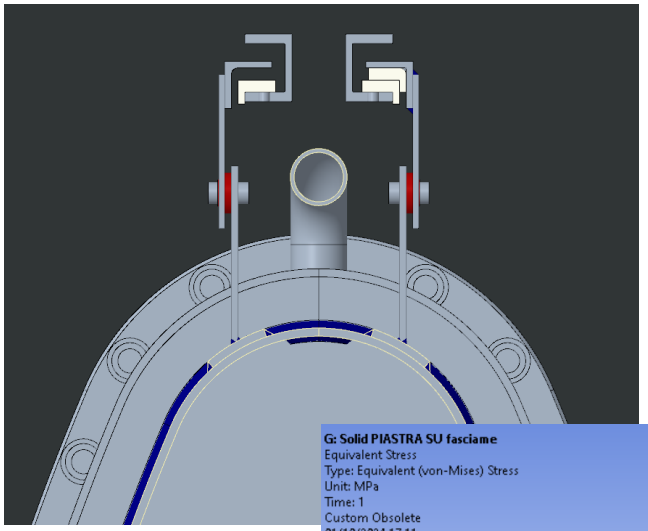
- Companies have been contacted at Big Science Business Forum – Trieste:
  - Simic
  - Mori Meccanica
  - Cryoservice

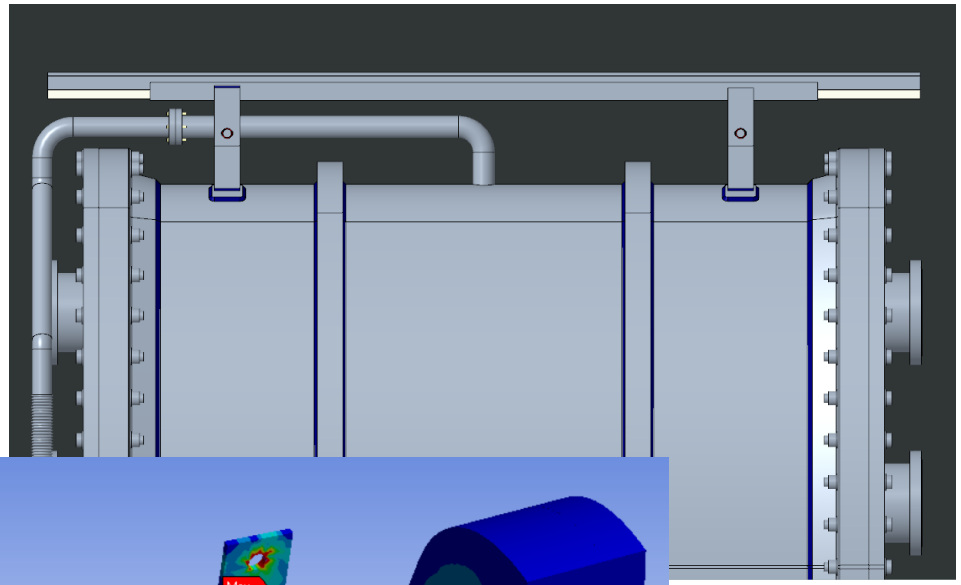
- Tender: beginning of 2025

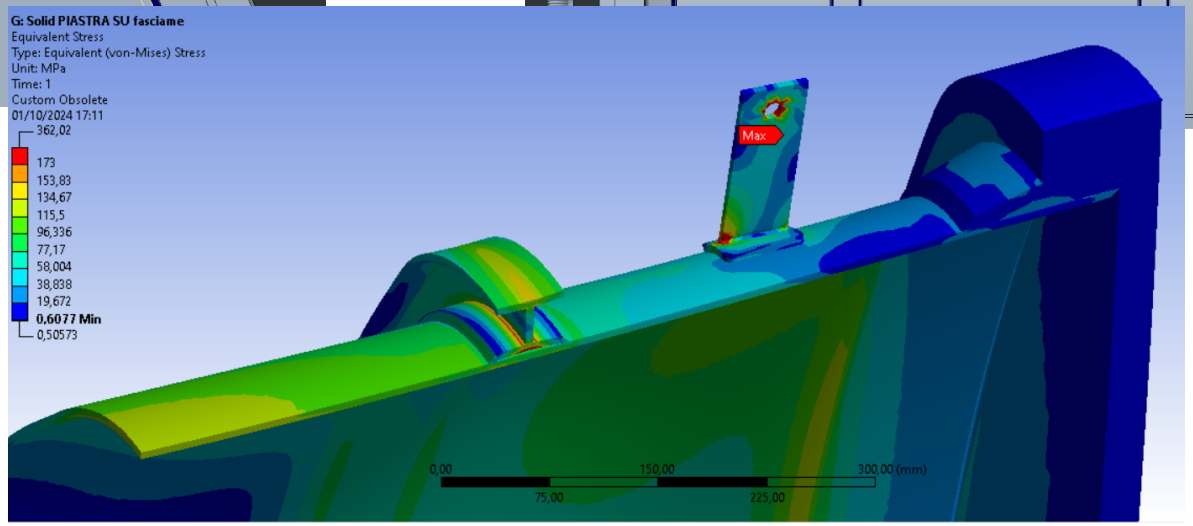


Sliding system

- Preliminary design, to be used also in final experiment

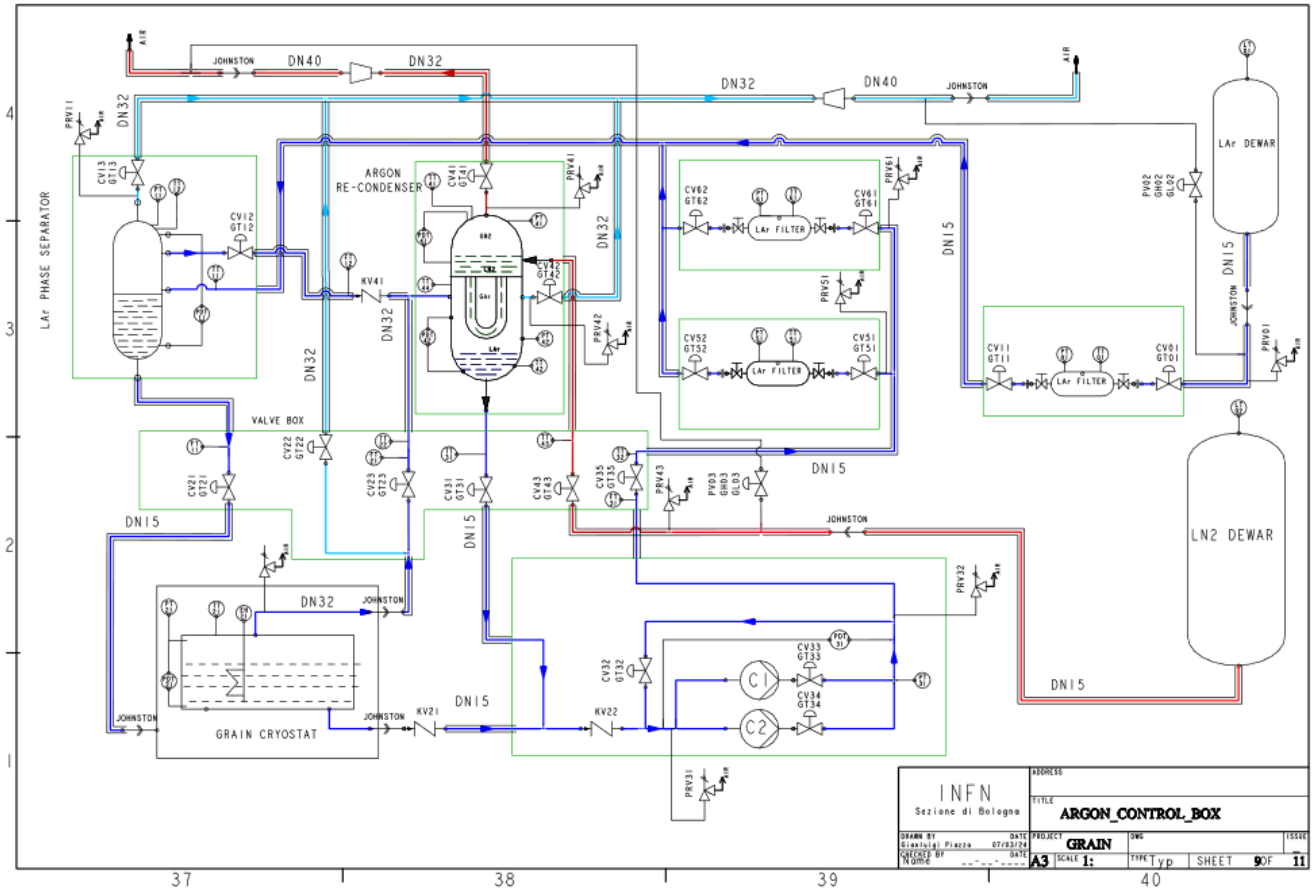






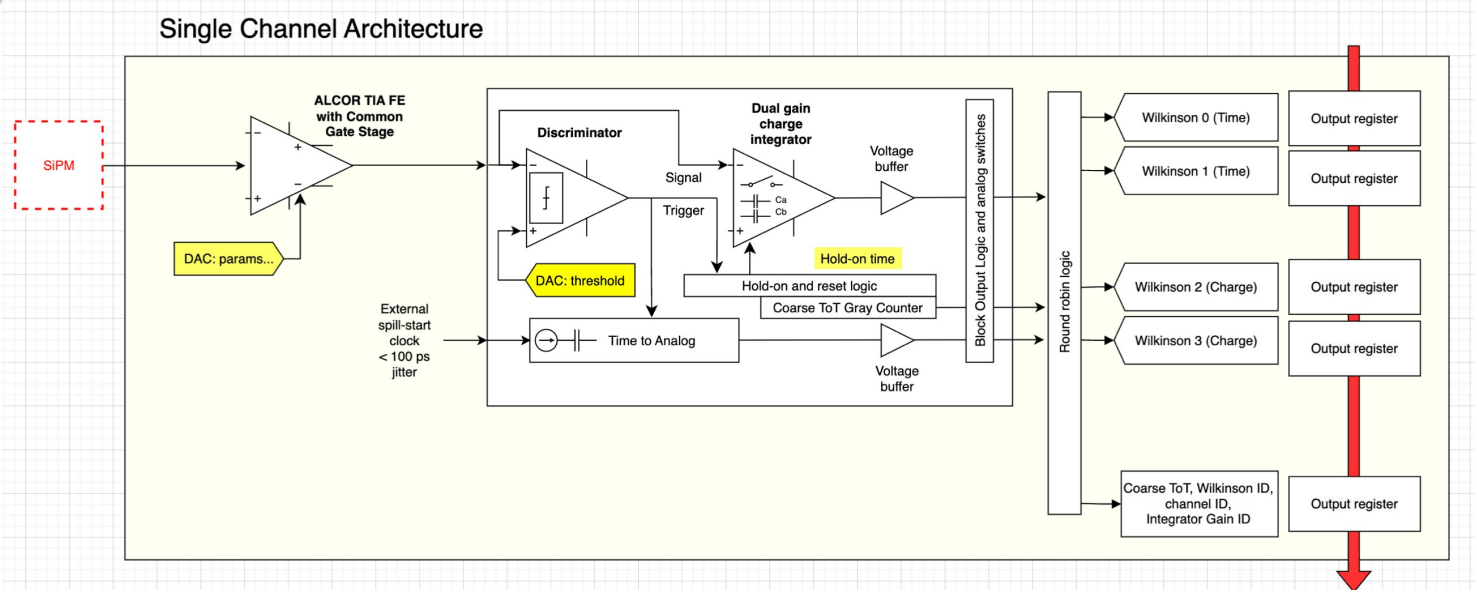
Cryogenic System

- Draft design ready
- Met companies at BSBF- Trieste and Market Survey started:
  - Cryotec (IT), SIMIC (IT), DEMACO (NL)



ASIC design

Proposed Pixel Readout Chain [from this talk by To]



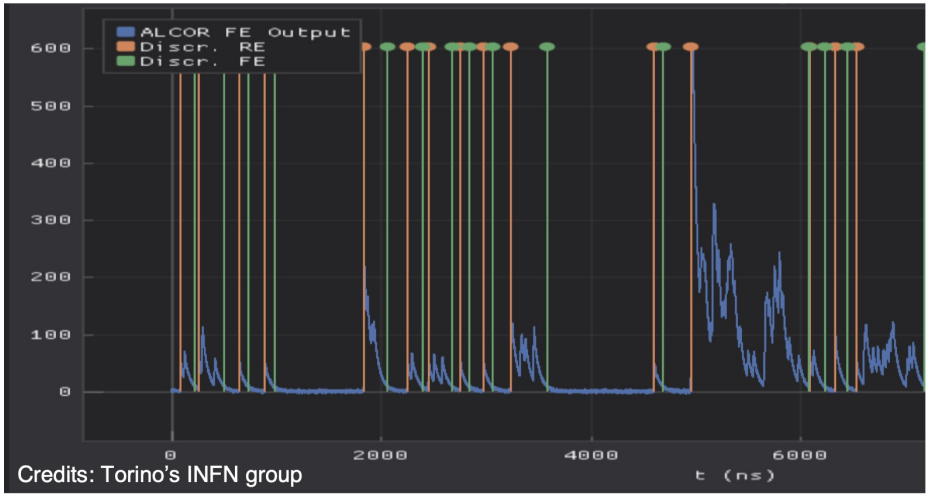
Power consumption < 5 mW/ch

Architecture with 2 integrators for each channel

- For each integration window we record:
  - Time with O(100 ps) resolution for rising edge on a 0.5 pe threshold,
  - Time with O(2 ns) resolution for falling edge
  - Integrated charge

ASIC design validation

- Torino group developed a **dedicated python code** for simulating
  - single photon waveform
  - electronics response



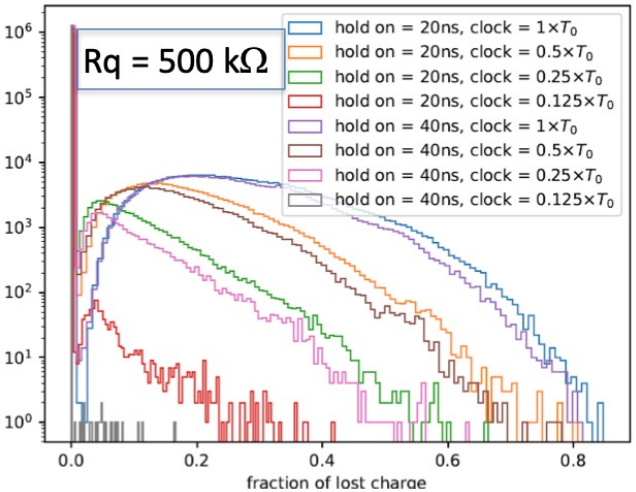
- **Parameters under validation:**
  - ADC dead and conversion time
  - dynamic range for each channel (maximum number of photons in each window)
  - Front-End saturation (maximum number of photons piled up within 10-20 ns)

for different SiPM parameters (quenching resistor, SiPM size, ..)

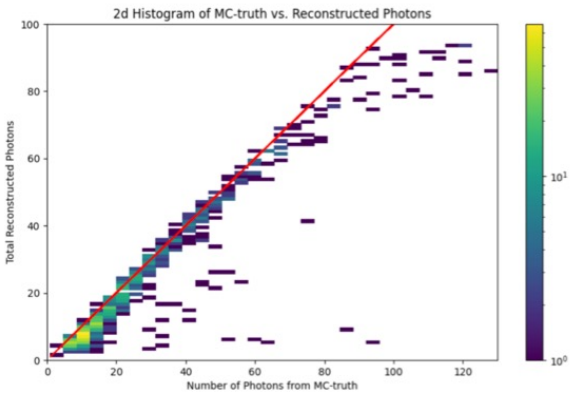
ASIC validation: first conclusions

- Parameters under validation:
  - ADC dead and conversion time → we need a faster ADC (x4)

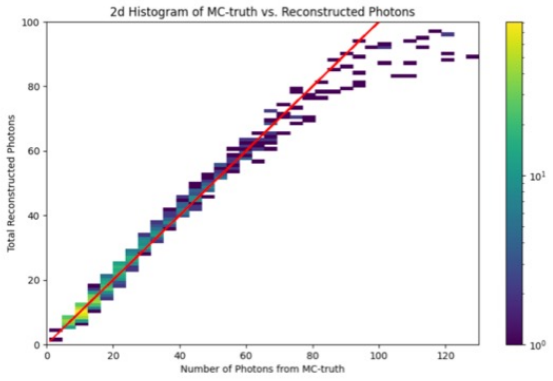
with coded mask



with lenses



Clock period = 3.333 ns

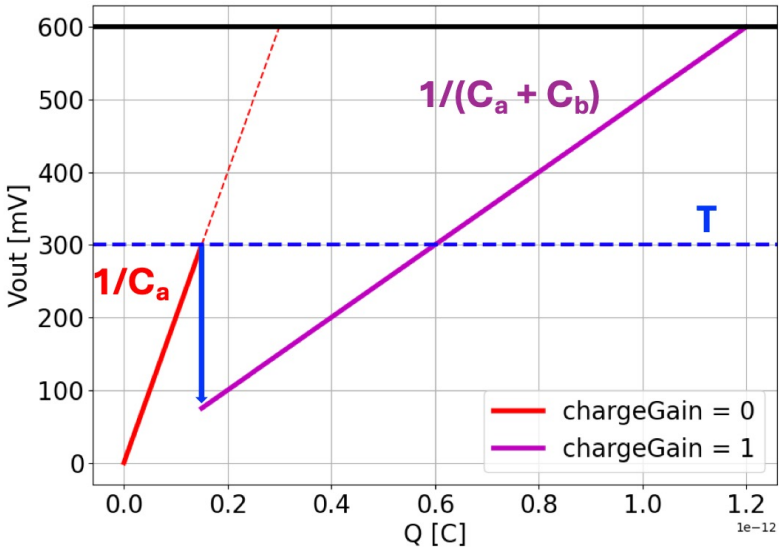


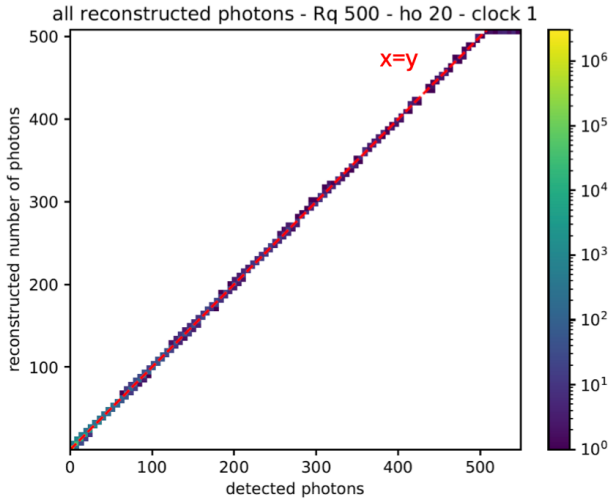
¼ Clock period = 0.833 ns

From here

ASIC validation: first conclusions

- Parameters under validation:
  - Dynamic range for each channel →two gains for integrators (up to few hundreds photons)





  - Front-End saturation (maximum number of photons piled-up within 10-20 ns)
    - to be investigated soon

ASIC design: current activities

Ongoing Activities: Pixel Design

S. Durando

Integrator Design:

- Transistor level design in Virtuoso
  - Current mirror based
  - DC current compensation
  - Two gains
- First simulation analyses soon

ADC Design Improvements :

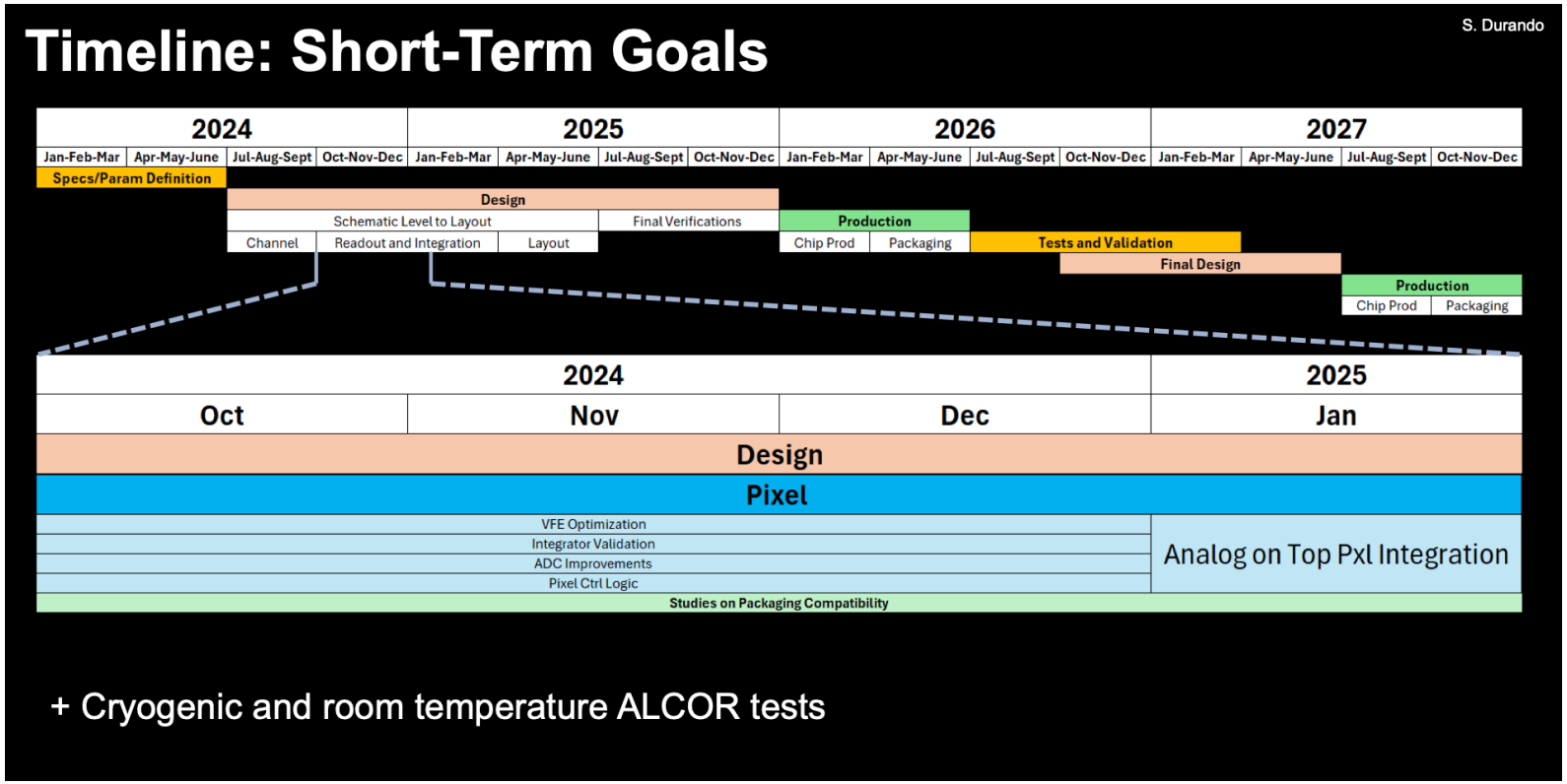
- Backward compatibility
- New SAR-based conversion algorithm
  - Faster conversion
  - Control logic and current injection improvements
- Block ready for integration expected by the beginning of December

VFE Optimization :

- ALCOR Cryogenic tests and simulations showed:
  - Vth and R variations impact mostly the TIA and the DACs
- Optimization
  - TIA and DACs design optimization
  - Configurable resistor arrays and current correction

Pixel

ASIC design: timeline



- By ≈ April : 2 x 2 Pixels Matrix Prototype
  - No real production
  - Case study for optimizing the full integration flow

Detector readout design

TASK	Design	Test
Test Mock up	Bologna	
ASIC	Torino	
SiPM characterization	-	NOA?
ASIC Test Board	To/Ge/Bo	
ASIC Test Daq	To/Ge/Bo	
GCB_L	Ge/Bo	
GCB_M	Bo/Ge	
GCIB+connectivity	Bologna	Ge
SiPM calib in GRAIN		
GWIB Hardware	Genova	Bo
GWIB Analog mezz.	Bologna	Ge
GWIB Firmware	Genova	Bo
Power+bias	Genova	Bo
Timing master IT	Bologna	
DUNE DAQ in IT	Genova	

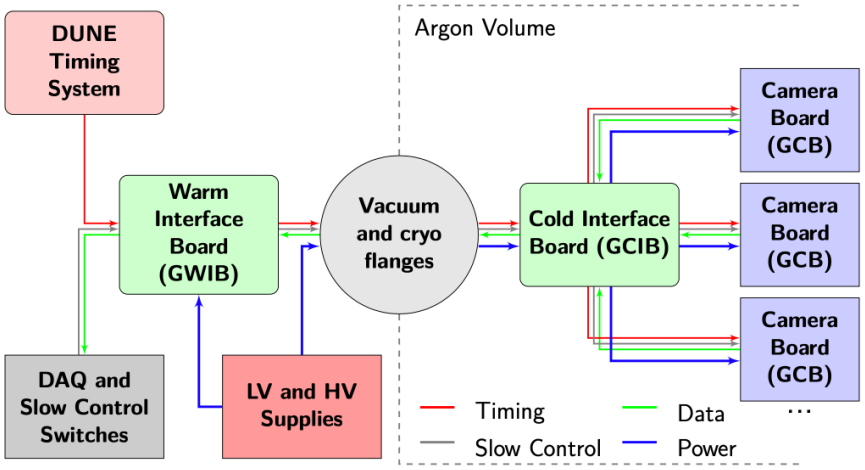
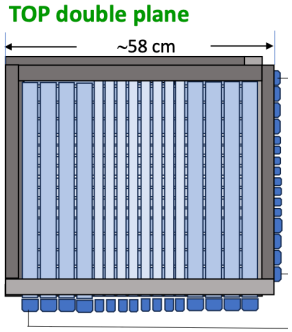
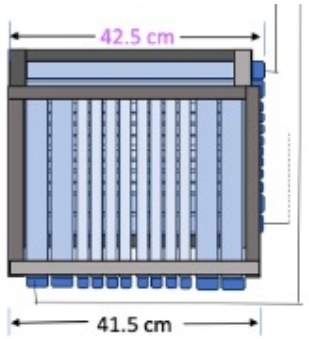


Figure 1.5: Block diagram of the GRAIN electronic system.

After the meeting on 16-10-2024 among GE and BO groups

CRT for ARTIC installed at Ge!





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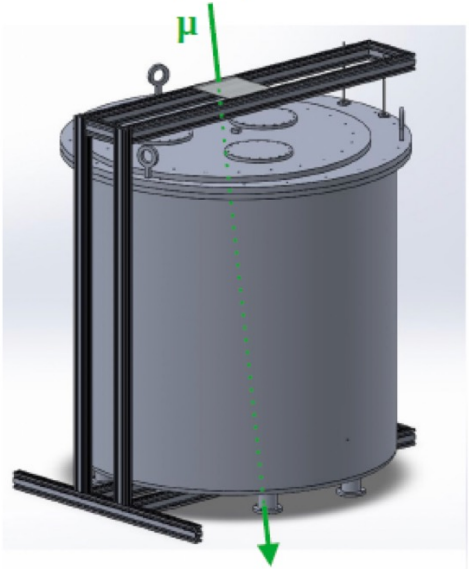
CRT GOALS:

- Trigger for the LAr acquisition (fourfold coincidence)
- Two-view tracking to help the LAr event reconstruction



Trigger condition: Fourfold coincidence

Conclusions

Many important activities are in progress :

- Mechanical design for vessels
- Cryogenics design and refurbishing in Legnaro

- ASIC design with Torino group

- Test with prototypes
  → finally started
  → CRT installed

Tests of prototypes in ARTIC

- Mechanics completed