# Smart-Pixel TPC

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# Motivation (I)

- Some **current/future HEP exp.** target for discovery & precision.
  → bigger detector
  → high-intensity beam

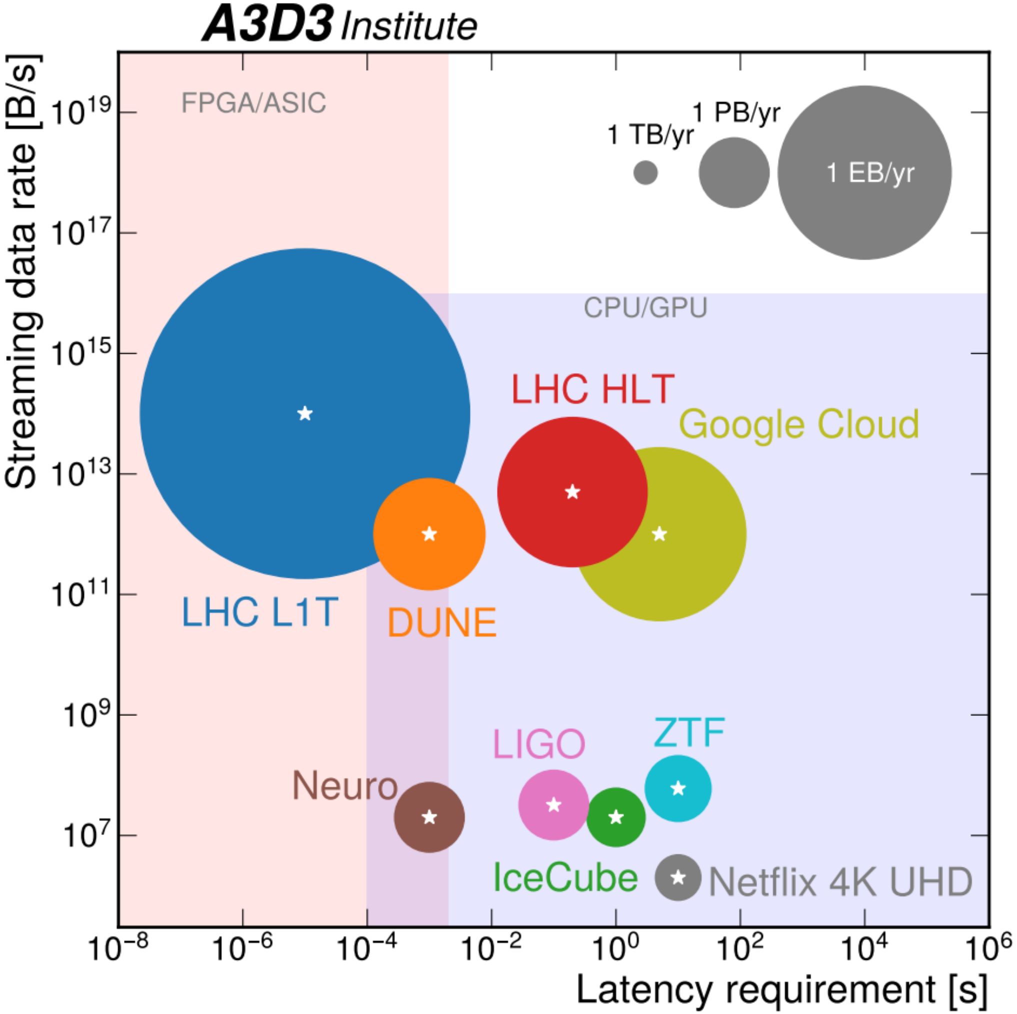
(HL-)LHC, DUNE

➡ Demand more **"resources"**

- Computing (storage, processors)
- Materials (channels, cables, etc)
- Energy (electricity)

➡ Will increase project/research **"budget"**

# Motivation (II)




→ We expect high raw data volumes for (HL-)LHC and DUNE.

❑ DUNE: arXiv:2203.16255

- ~ TB/sec → ~32 EB/year
- 100 % livetime (for Supernova)
- > ~ 20 years of operation

❑ DUNE's cap for computing: ~ 30 PB/year

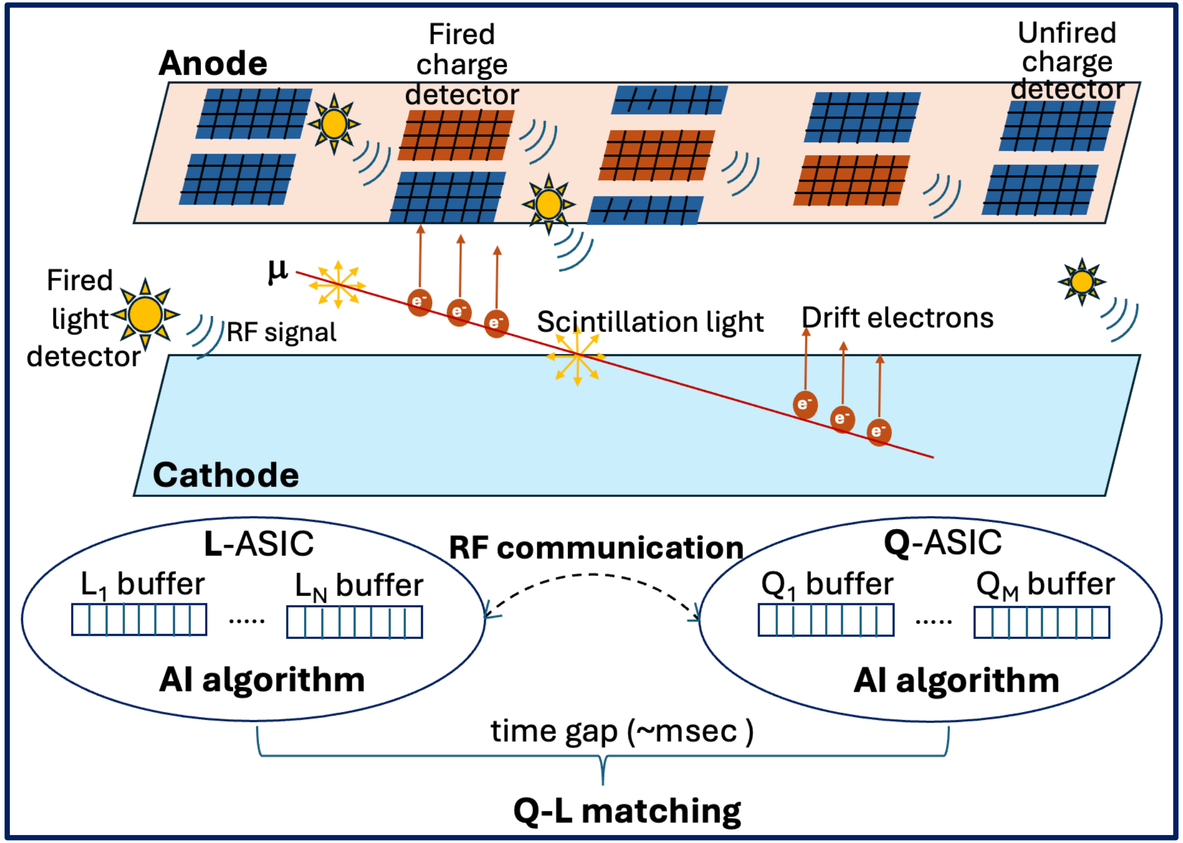
**→ 3 orders of magnitude reduction is needed.**

# Proposed Solution

- ❑ AI/ML "*in-situ*" → Reducing computing resources
  - Reducing raw data volume by applying AI/ML "*in-situ*"
  - Use **all subdetector info "*in-situ*"** to increase S/B
    - → **Unique & Challenging**
- ❑ RF network → Reducing use of materials
  - Essential for subdetector communication
  - Enabling cable-free detector
- ❑ Cryo dSiPM → Saving project budget
  - ~10% that of commercial SiPM

# AI/ML "*in-situ*" in LArTPC

## Smart-Pixel TPC: Charge (Q) + Light (L) pixel detectors




- ❑ Q-L matching "*in-situ*"
- ❑ Pattern recognition "*in-situ*"
  - Time
  - Space
  - Deposited charge & light

→ RF network among all subdetector components are essential.

# Test of RF Device(s) at LAr

❑ RF communication between Q & L detectors is essential for raw data reduction.

- We will start with a commercial RF device(s) to test it at LArTPC.
  ex) LoRa
  low power, cheap

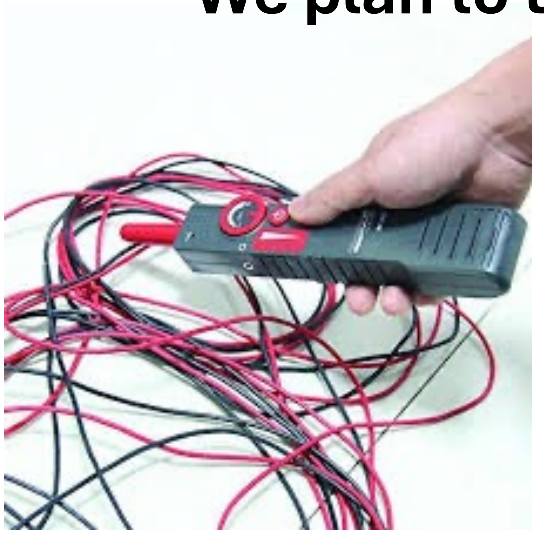
- Through tests in LAr,
  the device could be optimized to work properly in Cryo temperature.

# RF Communication

❑ Not only RF communication between sub-detectors, we can consider sending out raw data over RF network.

→ This will allow us to build a cable-free detector.

**We plan to test this during our R&D.**



Here, imagine DUNE detector w/ & w/o cables.

# Alternative Light Pixel Detector

SPAD: Single Photon Avalanche Diode

❑ Cryo dSiPM

→ Currently under-development
by Fermilab, EPFL, and Global Foundry

- Pros:
  -- Cheaper (~10% of commercial SiPMs)

- Cons:
  -- High dark count rate (→ need to measure it in LAr)
  -- Need VUV wavelength shifter

# Key Technologies in this R&D

- AI/ML on Chip (ASICs)
  → Reduce raw data volume "*in-situ*"
- RF Network
  -- Communication between Q & L detector
  → essential for Q-L matching "*in-situ*"
  -- Raw Data transfer
  → cable-free detector
- Digital CryoSPAD
  -- Alternative to commercial SiPMs
  -- not required for this R&D (but helps reduce budget)

} Application to any other experiments

# AI/ML Model to Hardware

## Model Building

AI/ML model

+ Simulated data

## HW-Aware Test

To optimize the model for given HW constraints (memory, speed, power,..)

Model Optimization (for resources)

+ Quantization
+ Pruning

## Model Translation

Co-design model (physicist, AI expert, HW engineer)

HLS4ML (SW → HW)

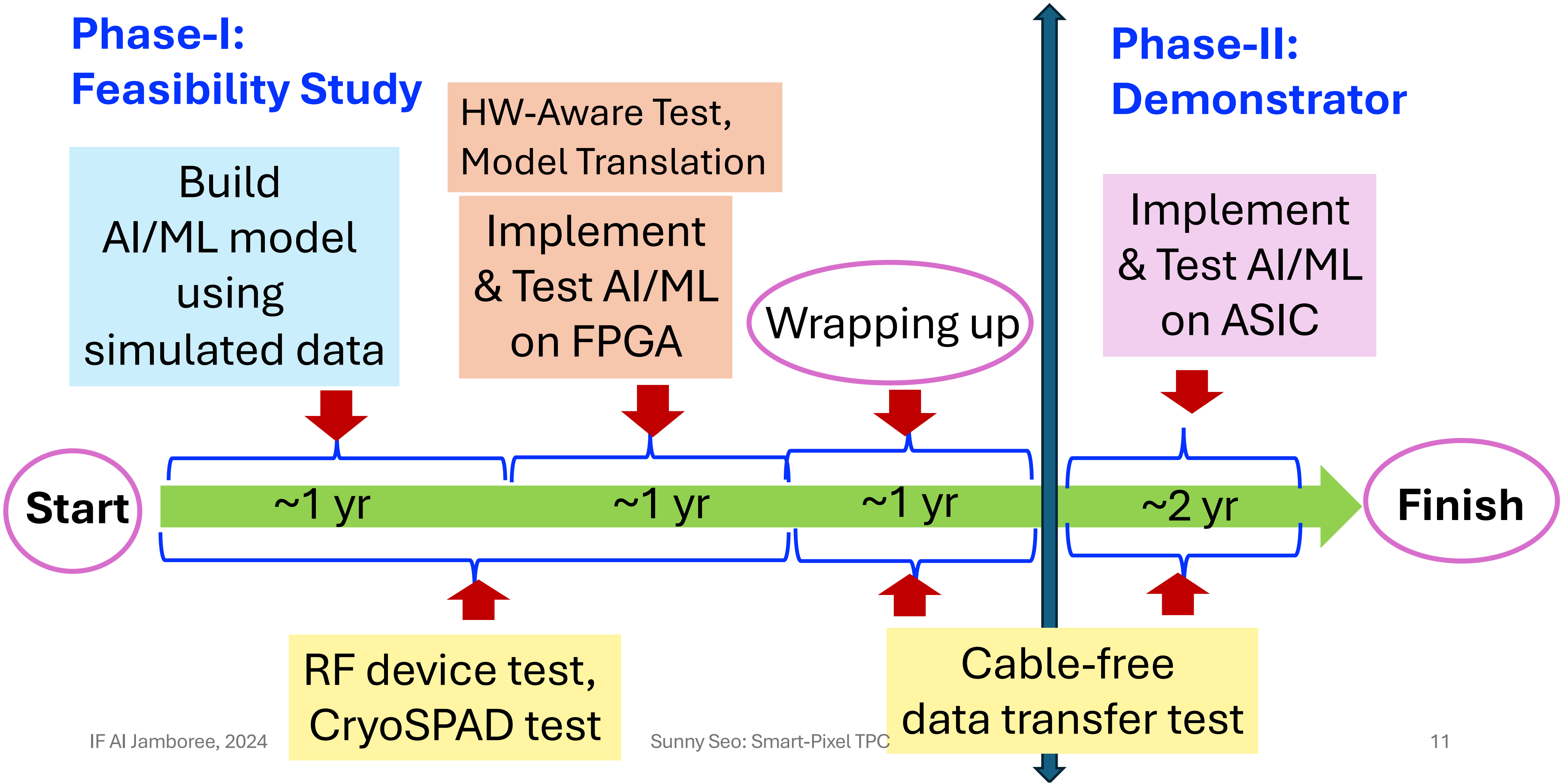
+ Optimization
+ Profiling
+ Tuning

## HW Implementation

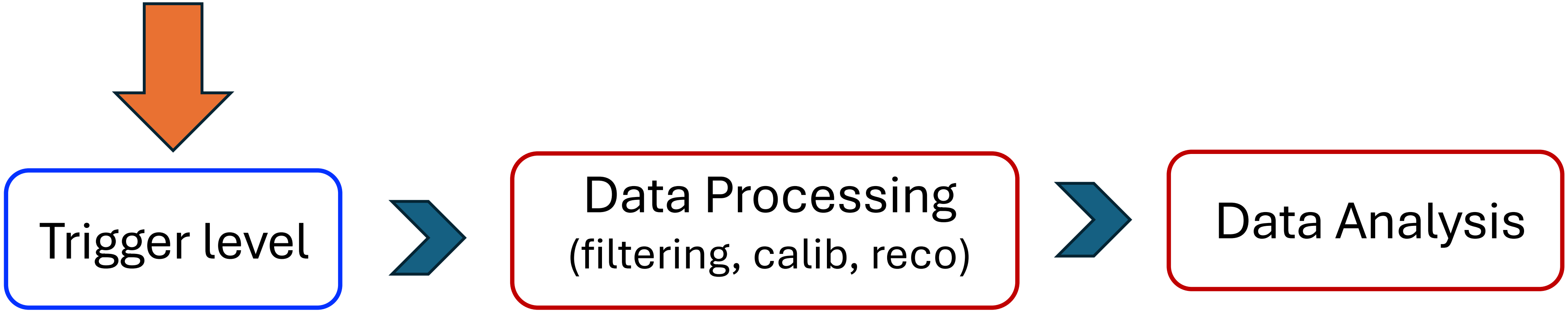
AI/ML on FPGA, ASIC

HLS =high level synthesis

# Timeline of “Smart-Pixel TPC” R&D



# AI/ML Start-to-End




Real-time anomaly detection

* new physics search
* Checking data quality
* monitoring detector