

# GCB Mock up design status

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# The purpose of LNL tests as I see it

- TDR text section 1.1.3.5 (written by me yesterday)

5 **LNL Prototype** The LNL facility will host the prototype inner vessel of the GRAIN cryostat,  
6 together with the cryogenic system (described in Section 1.1.8). The majority of the components  
7 of the latter will then be taken to Fermilab for use in SAND. In order to validate all the practical  
8 aspects of the cryostat and imaging readout system, a first prototyping step will consist in equipping  
9 the cryostat with a mechanical and thermal mock-up of the cameras, with a complete set of the  
10 power and signal cabling that will be required in the actual detector. The mock-up cameras will  
11 feature resistive loads equivalent to the planned ASIC and will allow to study thermal fluxes and  
12 techniques to mitigate the formation of bubbles in the LAr.

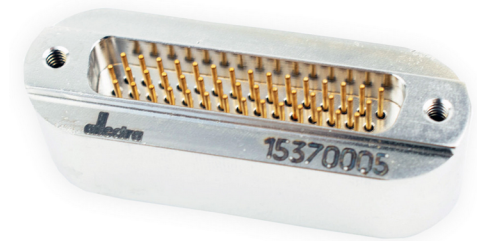
## and section 1.1.9.1 (written by ????? maybe also me...)

5 **1.1.9.1 Electronics Thermo-Mechanical Mock-Up Testing**

6 With the development of the readout ASIC (Sec. 1.1.4.2) on the critical path, it is especially  
7 useful to validate in advance all other open design choices on the readout system. These include  
8 in particular the choice of connectivity and cabling arrangements inside the cryostat and the  
9 solutions to mitigate the thermal load and the bubble formation caused by the electronics and  
10 the cables. The circuit boards for the GCB and GCIB, as well as all their components, will be  
11 validated in a large scale integration test. The boards used for the test, which are currently under  
12 development, will be mechanically identical to the respective final designs, and will host all the  
13 required components and connectors, except for the ASIC, which will be represented by resistors  
14 dissipating equivalent power over a similar surface area.

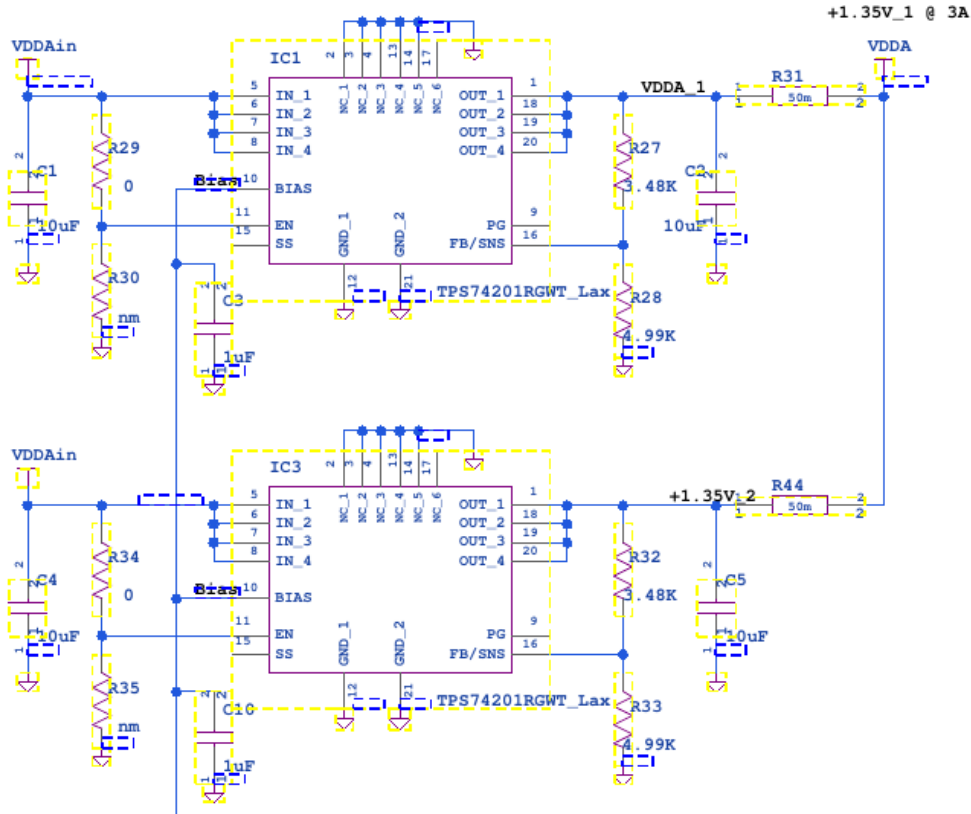
# The (first?) mock-up: main objectives

- Test LDO regulators for ASIC power
- Test power dissipation using equivalent resistors
  - Test LDO response to rapid change in load (ASIC power gating)
- Test LVDS 1:2 buffers
  - These would be used by the GCIB if necessary
- Test signal quality using D-Sub HD connectors
  - Available as cryo/vacuum compatible parts
  - 44 or 78 pin
  - Pinout TBD



# Schematic design: LDOs

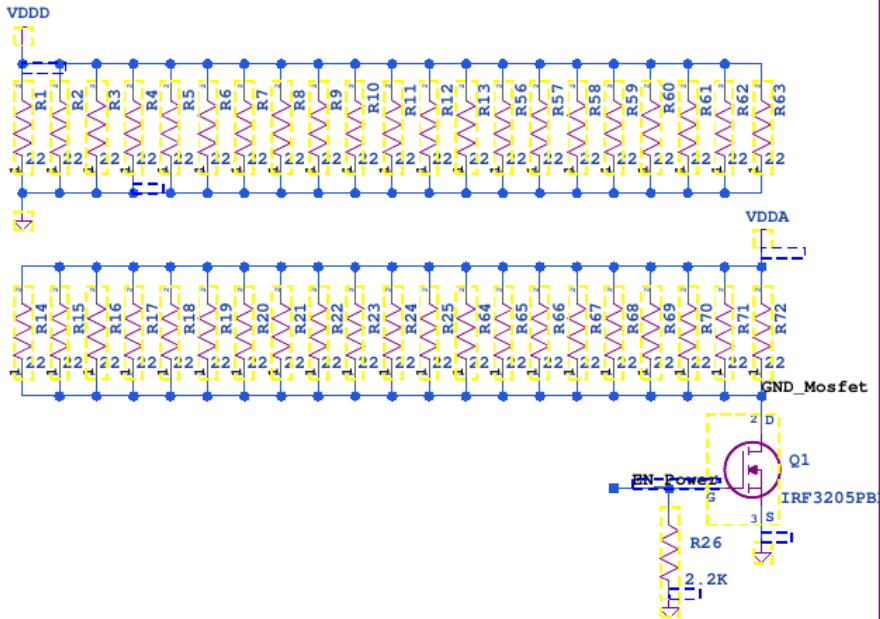
- TPS74201



- Known to work in cryo
  - Iout max 1.5A
  - Vout 0.8 to 3.6V
  - Dropout < 100mV
- VddA: 2x LDOs @ 1.35V
- VddD: 2x LDOs @ 1.35V
- VddIO: 1x LDO @ 2.5V
  - Also used by LVDS buffer
- Do we need to sequence them?

# Schematic design: “ASIC”

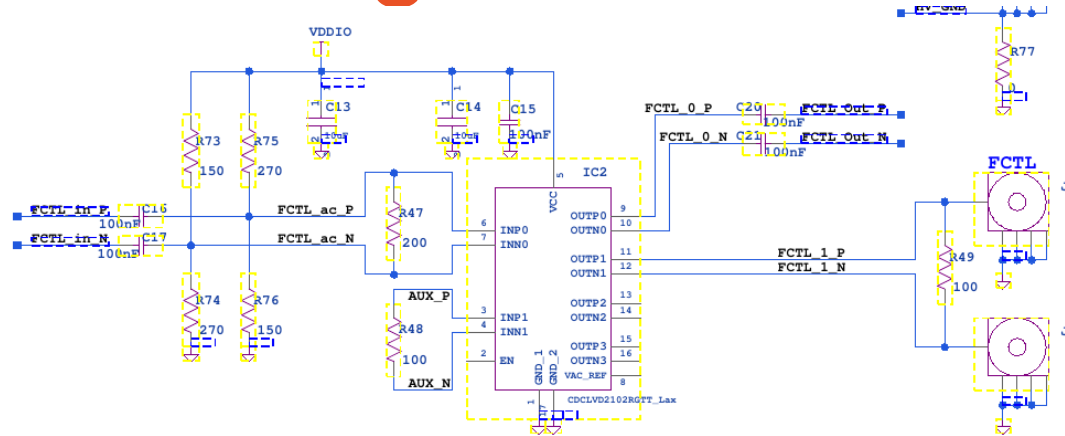
- Two sets of resistors in parallel
  - Default is ~1 Ohm per set
  - Set powered by VddD is always on, draws ~2 W
  - Set powered by VddA is enabled by mosfet, draws 2W when on
  - Layout and size matches ASIC size very roughly



# Schematic Design: “ASIC” I/O

- Clock @ 312.5 MHz: one LVDS pair
- Data out @ 312.5 Mbps SDR (or 625 Mbps DDR): one LVDS pair
- Fast control line, sync to main clock: one LVDS pair
  - Configurable via “SPI” as reset/sync/gate
- Analog probe output:
  - @**TO**: single ended or differential? We can buffer it outside ASIC if necessary to drive 50 Ohm over a few meters
- Slow control: @**TO**: SPI like in ALCOR? Something else?
  - If SPI, Do we want a differential clock? Do we need a Select/Reset?

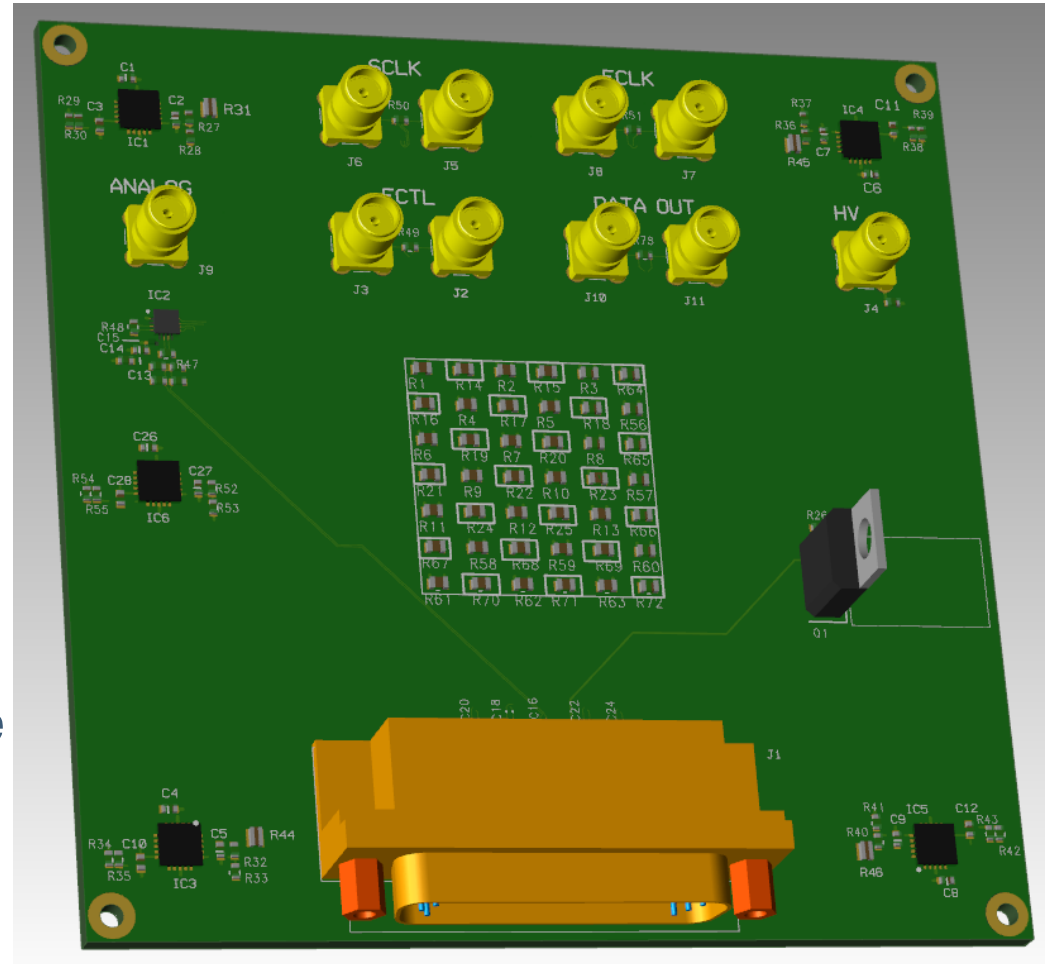
# Schematic design: LVDS



- LVDS buffer meant primarily for GCIB not GCB. Might as well...
  - CDCLVD2102 similar to model that is known to work in cryo
  - Allows us to test LVDS signals coming from GCB, not just going there
  - Various LVDS pairs in and out from D-sub HD to SMA
  - AC is ok for clock and data, testing pulldown termination for ctrl line

# Layout draft

- The mock-up is sized like a real GCB
- Excess number of layers, to spread heat from the central region (would be needed for routing in the actual GCB)
- Mock connection via the D-Sub, test via SMA
- More test points TBD





# Status and plans

- We started a bit early with this, compared to the plan
- Need some info from ASIC design group to proceed
  - Not urgent, but it is blocking. An estimate is good enough
- For the cable tests, we have procured some actual cryo D-sub both 44 and 78 pins
- We are considering using a kapton flex as a cable in both vacuum and LAr
  - A bit more expensive and stiff, but higher performance
  - May also need one custom connector (machined from PEEK)