Problems wire bonding ColdADC & COLDATA

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ColdADC & COLDATA

- Our Front End MotherBoards (FEMBs) use 3 ASICs:
  - LArASIC – 16 channel Amplifier/shaper
  - ColdADC – 16 channel ADC
  - COLDATA – Control and data concentrator

- LArASIC is implemented in TSMC 180nm CMOS
- ColdADC & COLDATA are implemented in TSMC 65nm CMOS and are being fabricated on a shared wafer.
  - Each reticle contains 1 COLDATA + 3 ColdADCs

ColdADC/COLDATA production

- Two lots of 25 wafers were ordered in August 2023
- Production was started at TSMC in October 2023
- 50 wafers were received at CERN on November 24, 2023.
- They were shipped to FNAL and received on Jan 29, 2024.
- After the PO for packaging was placed, they were shipped to ASE in Taiwan, leaving FNAL on Feb 29, 2024.

Timeline – March-April 2024

- March 22, 2024 – Confirmation that lots NBMY62.00 & NBNA38.00 were received by ASE in Taiwan.
- April 22, 2024 – Defects observed on incoming wafers.
  - “operators observed glassivation issue”

    There are risks with using these wafers and we require waiver that we are ISE/ASE is not liable for any yield issues or quality issues with the assembly of these wafers.

    It has risk to taping BG tape non-sticking on wafer edge due to uneven surface.

    It has risk to encountering wafer crack and bond pad contamination during grinding process.
- Contacted Kostas Kloukinas (CERN)
  - He had not seen similar damage before, and he forwarded my email to IMEC with the request to contact TSMC for advice.
  - We gave the OK for ASE to thin one set of 25 wafers.

Backgrinding

- Backgrinding of the 1st lot of 25 wafers went well; we released the 2nd lot and all wafers were thinned without problem.

Feedback from TSMC (via Kostas from IMEC)

- TSMC examined the images and observed delamination affected only non-functional devices. “The wafers will not have been shipped if they did not comply with TSMC WAT (Wafer Acceptance Test). This delamination should not affect the other (fully processed) die on the wafer.”

May 2024

- Wire bond pitting observed on wafers of lot NBMY62.00
- “Issue occurs randomly on all wafers.”
- Samples failed wire pull / ball shear tests

ASE confidential picture & table removed

“Clarifications”

- “Wire bond pitting” was observed by ASE for one of the two lots at the inspection station after wafer thinning & singulation. This was the first microscopic inspection done by ASE. One wafer from the lot was inspected and 25 COLDATA chips selected for wire bond testing. All 25 failed.
- In response to questions, ASE inspected 50 COLDATA chips from another wafer; the same “wire bond pitting” problem was found on all 50 chips.
- ASE reiterated that the “wire bond pitting” problem was not seen on the first lot of 25 wafers, which were at that time further along in the packaging process.
- ASE suggested that we reject this lot of 25 wafers. Kostas asked for a descriptive report that could be sent to TSMC. ASE sent a pdf file with essentially the same (ambiguously worded) information sent earlier.
- IMEC asked for a phone conference with ASE. ASE agreed after some delay. I scheduled a Zoom call for 00:30 June 25 (Chicago time); 22:30 (California time); 13:30 June 25 (Taiwan time); 07:30 June 25 (Central European time)

Conference call: IMEC/ASE/FNAL

- I was the only one on the call with video enabled.
- A number of ASE engineers attended from a conference room.
- Sai Krishna Gadde (IMEC) led the call with a number of questions,including:
  - Can we get more microscopic images from random locations?
  - What is the size of the bond pad pits?
    - ASE process engineer Jaimie shared his screen showing a bond pad or pads
  - Sai stated that TSMC would fail a wafer if bond pad pits > 3 microns diameter are observed, or if pits that merge are observed.
  - Sai asked if ASE had seen this sort of issue before
    - The answer was they would need to check
  - Sai asked if ASE could modify the bond settings for deep bonding of copper bonds?
    - The answer was yes, but this would take some time
  - Sai said that gold wire bonding would be preferable. He also asked if microscopic inspection could be performed before any processing in the future. There was no response from ASE on either point.
  - ASE agreed to provide more microscope photos and to propose a plan.

Additional photos from ASE (1/3)

- ASE confidential picture of COLDATA “bond pad pits” removed

From ASE (2/3)

- ASE confidential picture of ColdADC “bond pad pits” removed

From ASE (3/3)

- ASE confidential picture of ColdADC and COLDATA “bond pad pits” removed

ASE Plan

- Details of ASE plan for optimization of copper wire bonding parameters removed

We agreed to an additional $5k engineering charge.

Result of tests with “deeper” copper wire bonds – August 25, 2024

- Bonds using cell 1 parameters failed pull tests
- Bonds using cell 2 and cell 2 parameters passed the pull tests, but caused “cratering” and also caused the bond pads to crack.
- Sai (IMEC) said that they were “looking into the report from ASE and trying to understand the root cause of the pad crack issues. However, the bond pad pits are within the TSMC outgoing specifications, so we cannot expect any support from them on this matter.”
  - In response to a question from Cheng-Ju, Sai said that he did not have authority to share TSMC’s outgoing specifications.

Next – email to ASE on Sept 27, 2024

Hi Yen,

I appreciate your patience with regard to the problems that have arisen with our chips from batch #NBMY62.00. I have recently received more information from TSMC by way of IMEC and CERN. The IMEC team reports “new feedback from TSMC in which their OQA team deems the features in the provided pictures to be hillocks, not pits.” That is, TSMC believes the spots visible on the bond pads are raised features, caused by thermal cycling of the aluminum under compression. TSMC told IMEC that they (TSMC) have previously performed wire bond tests on bond pads with hillocks, with satisfactory results. The TSMC tests were done using gold ball bonds. I am interested in your reaction to this information from TSMC. Do you agree that the features you have observed on our chips are consistent will pad hillocks (as opposed to pits in the pads)? Also, is ASE able and willing to do gold wire bonding, either for sample chips from this batch of wafers or for a future batch of wafers? Is there a reason to prefer copper wire bonding over gold?

We are still exploring whether TSMC will consider accepting an RMA of this wafer lot, or part of the lot. I would appreciate it if you would continue to hold the wafers while this is sorted out.

Best wishes,

David

ASE reply

- “For TSMC term about the issue, we did not conduct further analysis since the issue was observed before assembly process.”

- After some discussion, they agreed to try gold wire bonding (for another $5k engineering charge) … and we agreed to this. The change order to the PO was issued on Oct. 28.

Summary from Kostas dated Nov 10

- TSMC and IMEC physical analysis team reviewed the reports from the packaging vendors that we have provided
- and they provided the following feedback.

1. The report of TSMC that what is seen on the bond pads is **not pitting, but hillocks.** This is typical for this technology since the aluminum is deposited on top of copper, while most of the production of the assembly houses are pure aluminum. So the bond pads in case of aluminum on copper look totally different to what these assembly houses are used to see. The issue of hillocks on top of aluminum bond pads is reported in many projects imec has with copper metallization. **When the optical inspection issue is "hillock" this is a pure cosmetic issue and can cannot cause any wire bonding issue.**

2. The recommendation is to use gold wire bonding. Gold wire bonding has a much wider wire bond process window, and requires a lower amount of energy to wire bond. ASE using copper wire bonding is clearly hitting bond pad cratering limit. Therefore **with less bond energy one will not hit the cratering limit.**

Gold wire bonding results from ASE (Nov 18)

- All gold wire bonding parameters yield good bonds that satisfy all criteria.

ASE confidential information from gold wire bond testing removed.

ASE confidential information from gold wire bond testing removed.

Conclusion

- We will have ASE use gold wire bonds & cell M parameters for the problematic batch of 25 wafers.
- We estimate this will add ~$38k to the cost of packaging.
- We anticipate fabricating one more batch of 25 wafers in the near future. This will yield enough chips for both FD1 and FD2.
- For the new batch of wafers, we intend to ask ASE to perform a microscopic inspection before wafer thinning.
- Our preference is to use gold wire bonding for this batch of wafers whether or not blemishes are observed on the bond pads.