FSD Run 1 Outcomes — Charge Readout

Summary of FSD resources

	Materials [k$]	Technical Staff [hours]	Scientific Staff [hours]
Procurement/production	>83		20
Component assembly, QA/QC	>40		200
FSD integration/testing*	2		72

*Through warm commissioning

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Technical specifications

- Validated
  - Pixel noise: ~500 electrons (realized); <1000 electrons (requirement)
  - Bad pixel fraction: 0.55% (realized); <5% (requirement)
  - Bad ASIC fraction: 0.74% (realized); <3% (requirement)
  - Pixel tile leakage: <1 electron / reset (realized); <<1,000 electrons / reset (requirement)
- Outstanding
  - Pixel data loss fraction: <0.1% (requirement)
  - Pixel efficiency: >95% for >¼ MIP track traversing full pixel pitch (requirement)
  - Pixel charge resolution: <3% σ_Q/Q (requirement)

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Risks

- PCB flatness after cryocyling [closed] - no PCB warpage observed with cryocycling
- Insufficient quality control of off-shore produced PCBs [reduced]
- Cabling compatibility [closed] - no evidence of LAr purity comprise with cabling
- Full-tile triggering instability [closed] - no evidence of occurrence at FSD

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Aspects of the design

- Closed
  - Anode tile PCB scaling x1.6
  - PACMAN hardware scaling x1.25 and optimization
  - Full size feedthrough production
  - Cabling performance in LAr
  - Calibration fiber interfacing
  - Data transmission over full length cables
- Open
  - LArPix ASIC migration to 130 nm → LArPix-v3 operation at FSD run 2
  - LArPix ASIC LSB reduction → LArPix-v3 operation at FSD run 2
  - Incorporation of timing endpoint → timing master integration at FSD run 2
  - Anode geometry optimization →SingleCube operations Spring 2025