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Interconnect activities at ORNL

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U.S. DEPARTMENT OF ENERGY

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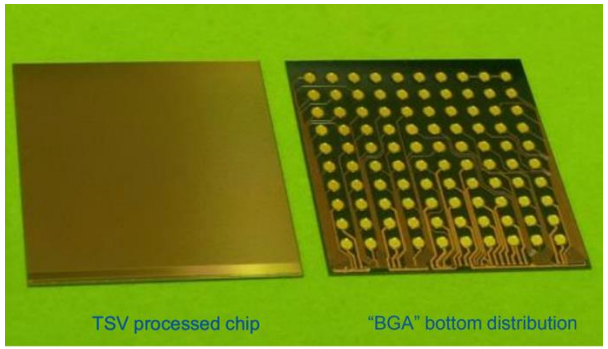
Outline

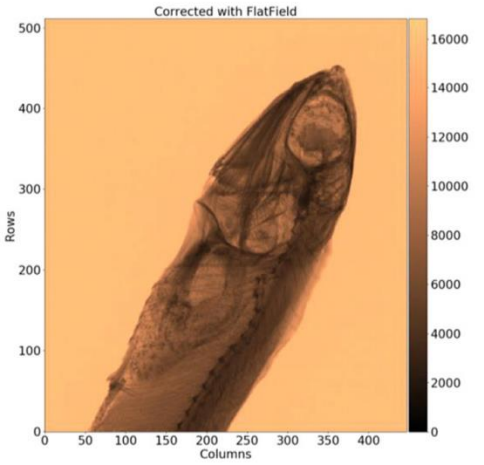
- Timepix4 TSV and Large Sensors development
- 3D-PDC and die-to-die eutectic bonding for 3D integration
- Anisotropic conductive glue for low-cost bonding
- Gold stud bumps for low-cost bonding
- Single die processing for bump deposition at ORNL

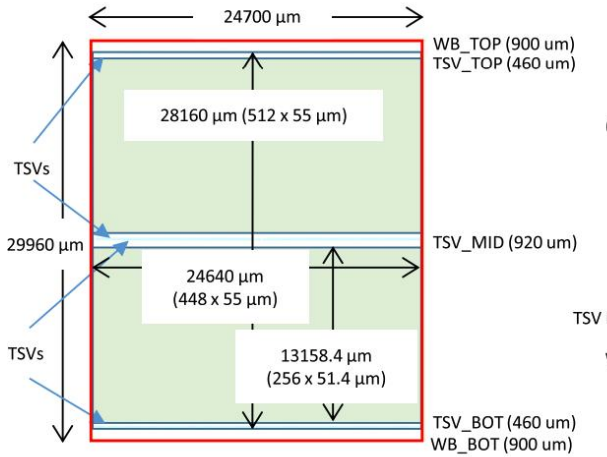
Timepix4 ASIC

- 55 x 55 µm^2 pixels
- 448 x 512 pixel matrix, 24.7 x 30 mm
- ToT (16 bit counter,~1.5 keV) and ToA(<200 ps)
- ~3.6Mhz/mm^2/s hit rate capability
- ~800e threshold
- **4 side buttable using TSV connections**
  - Pixel Layout fits 55x51 µm^2, Bump pad deported via top metal layer

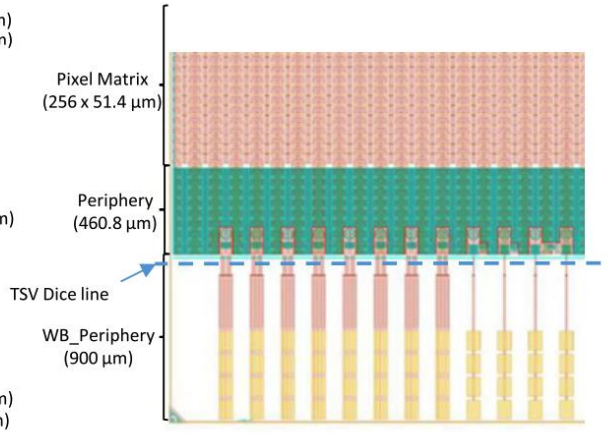


Medipix3RX with TSV





(a)



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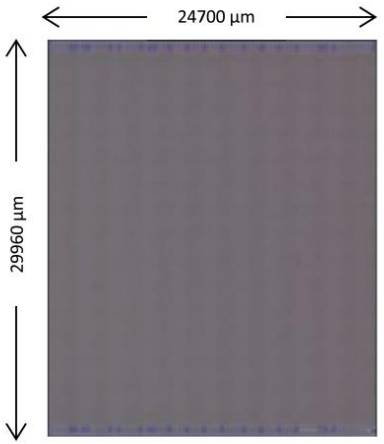

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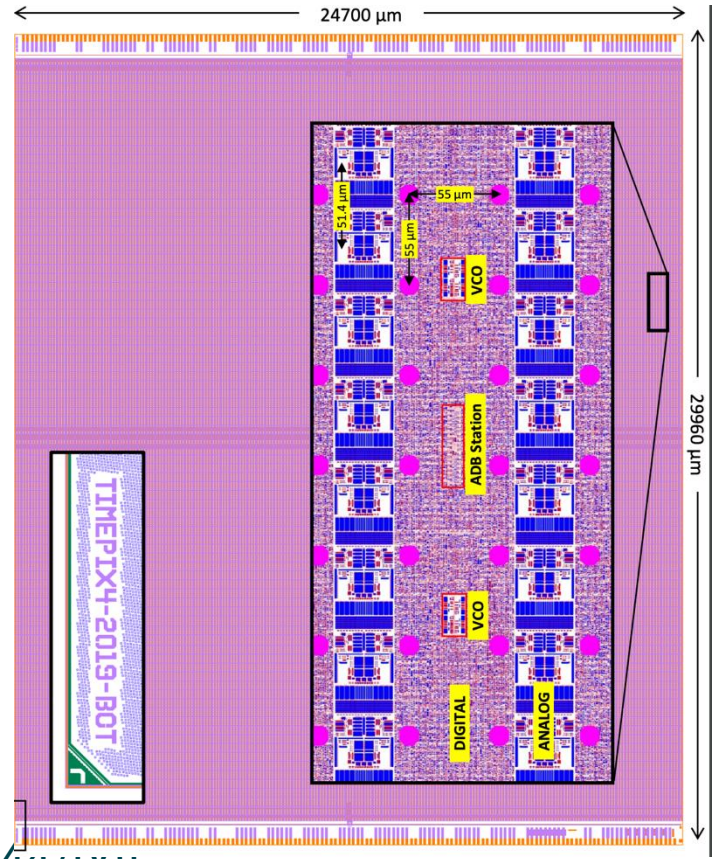
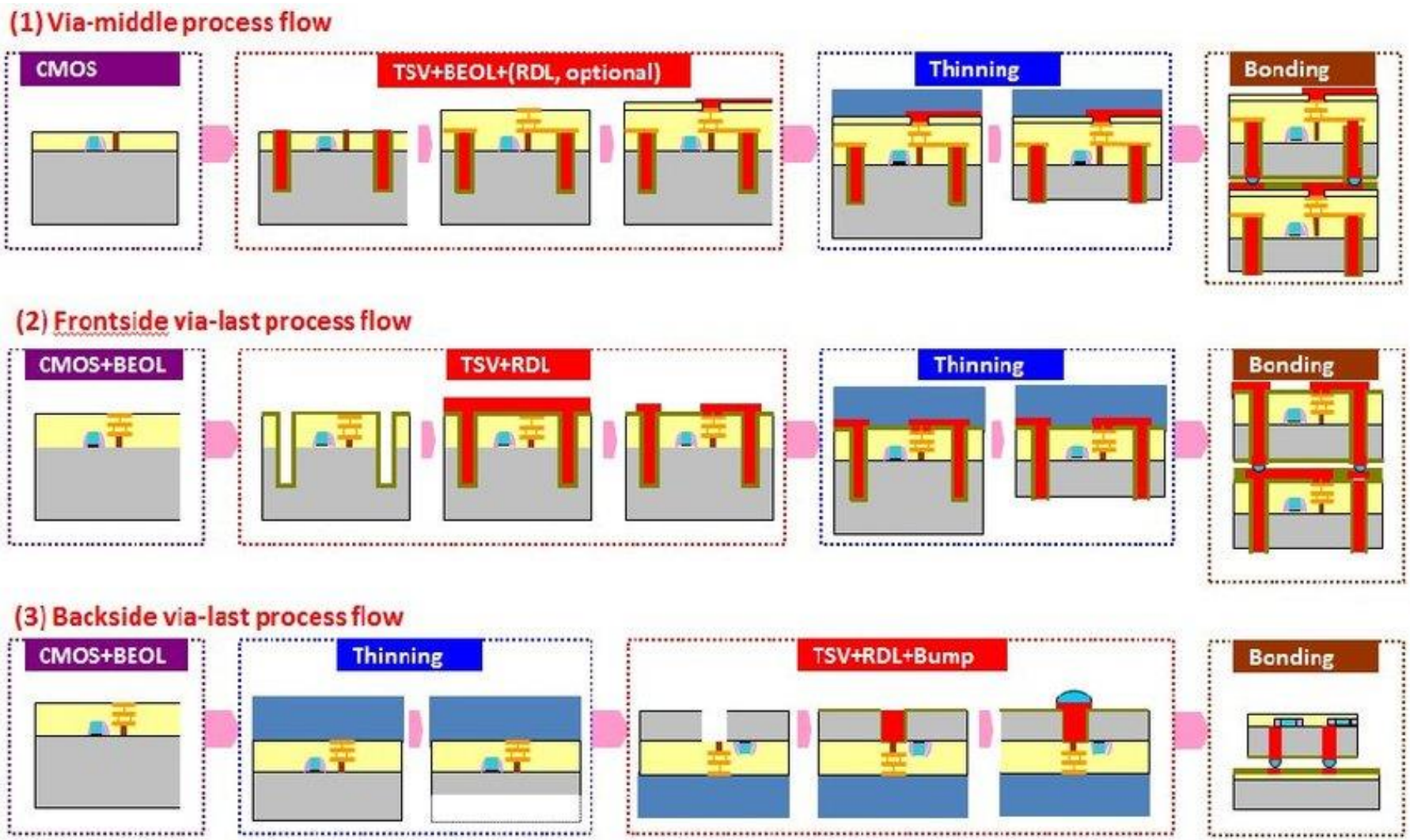


https://iopscience.iop.org/article/10.1088/1748-0221/17/01/C01044/pdf

Through-Silicon-Vias processing



The Medipix/Timepix collaboration has a long history of R&D on via-last processing of large ASICs

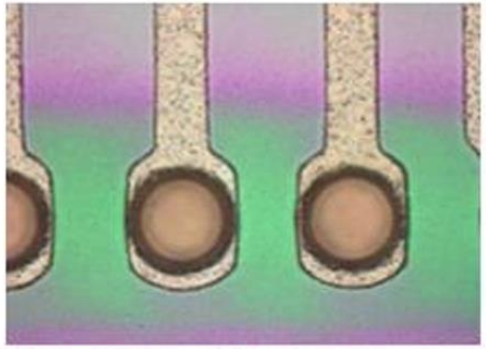
- First trials with CEA-LETI with Medipix3 wafers with good results
- This drove the decision to make Timepix4 a TSV read ASIC

New Challenges brought by 65nm technology and beyond -> 12” wafers

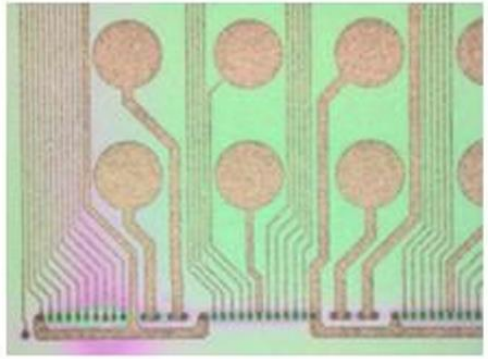
- CEA, IZM not able to process 12”, must rely on coring wafer
- The collaboration is seeking partners to process full wafers

TSV Medipix3RX

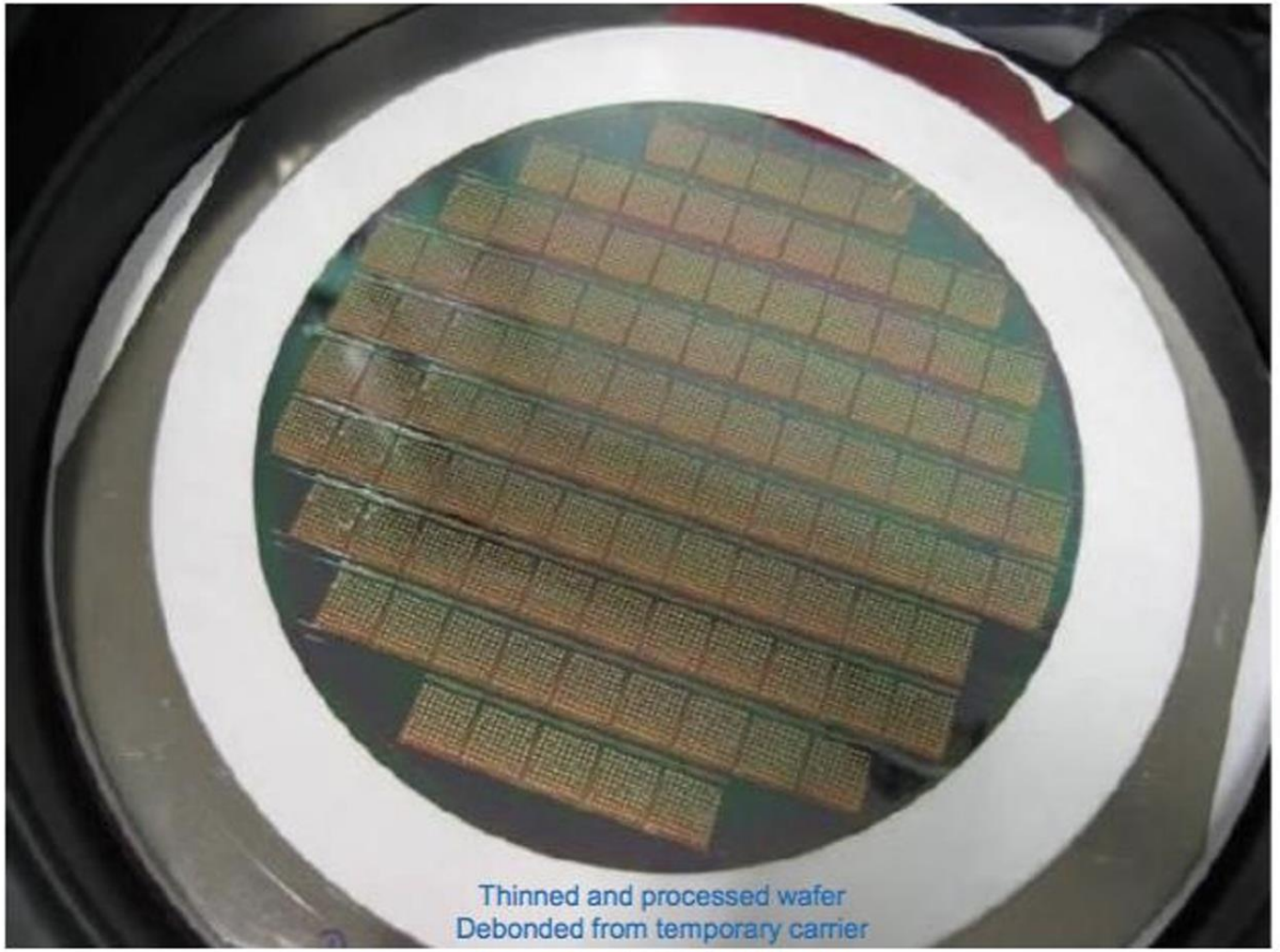
- Second run processed 6 wafers of Medipix3RX
- TSV yield ~ 70% to 80%



Through Silicon Vias diameter 60 µm
Wafer thinned to 110-120 µm



Redistribution layer
Back side of Medipix3 chip



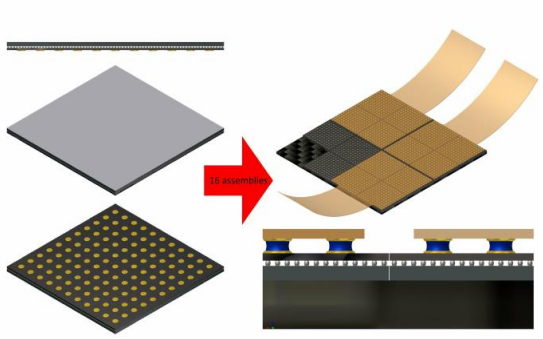
Thinned and processed wafer
Debonded from temporary carrier

Images courtesy of CEA LETI

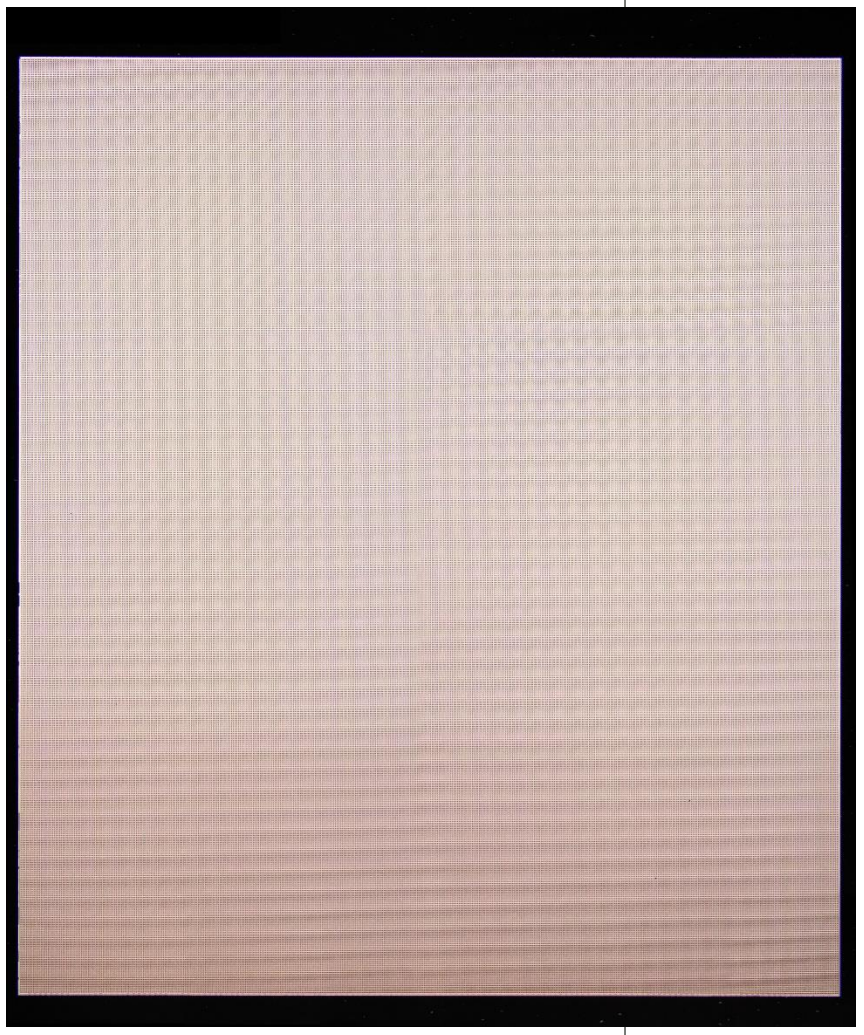
A Timepix4 with TSV

ORNL is investing 75k in processing of 12” wafers with IZM Berlin, securing 2-3 wafers (~70 chips)

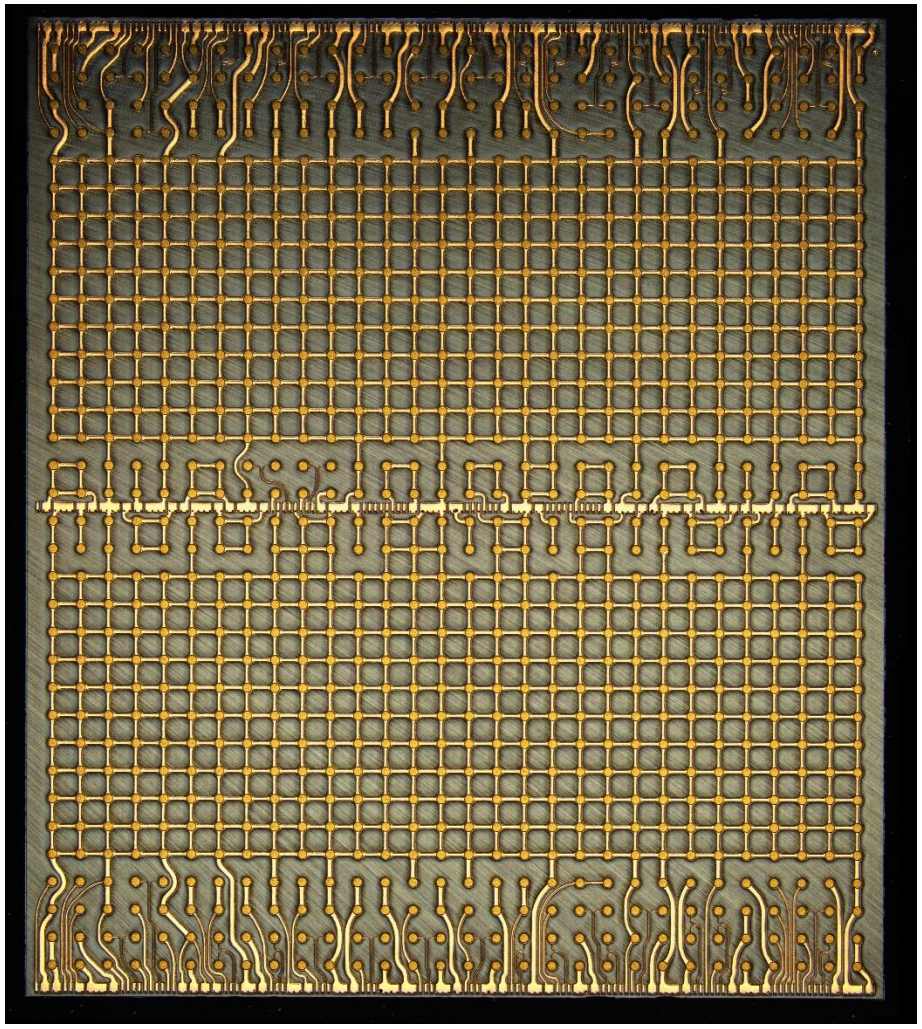
- TSV processing essential for large area tiling
- We plan on developing integration methodology using ACP/ACF or bumps that is ultimately wire-bond less



Pixel side



Back side

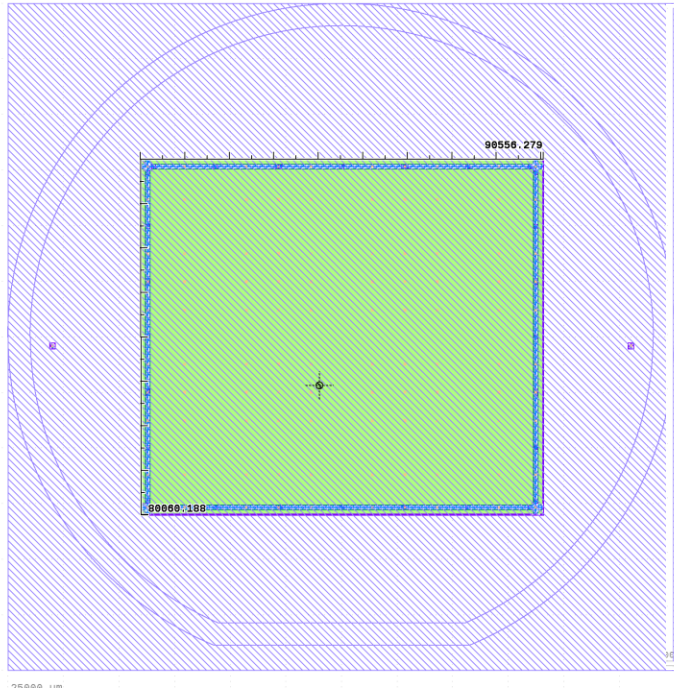


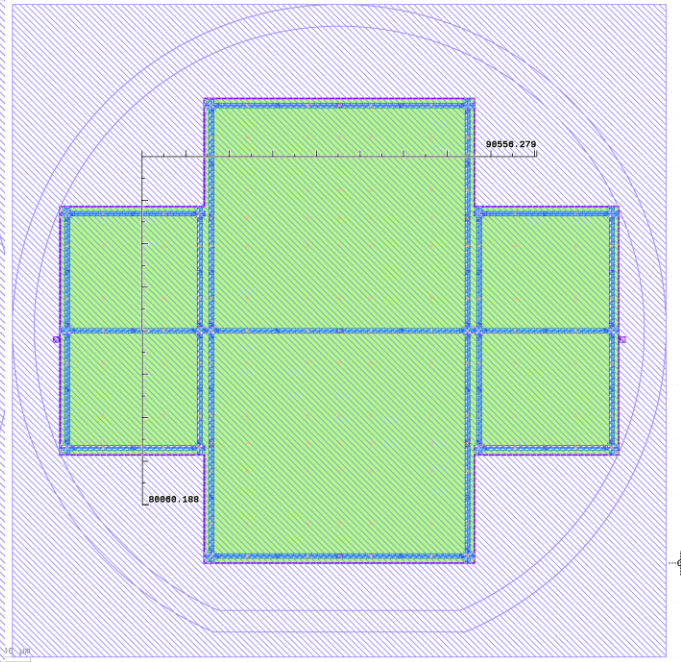
https://indico.cern.ch/event/1439336/contributions/6261676/attachments/2978870/5244628/drd3_extra_results.pdf

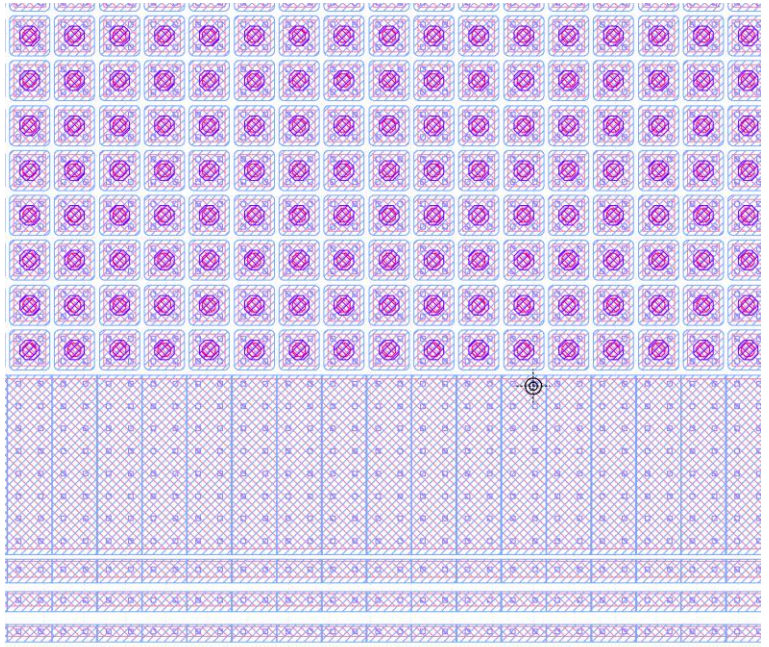
Sensor production

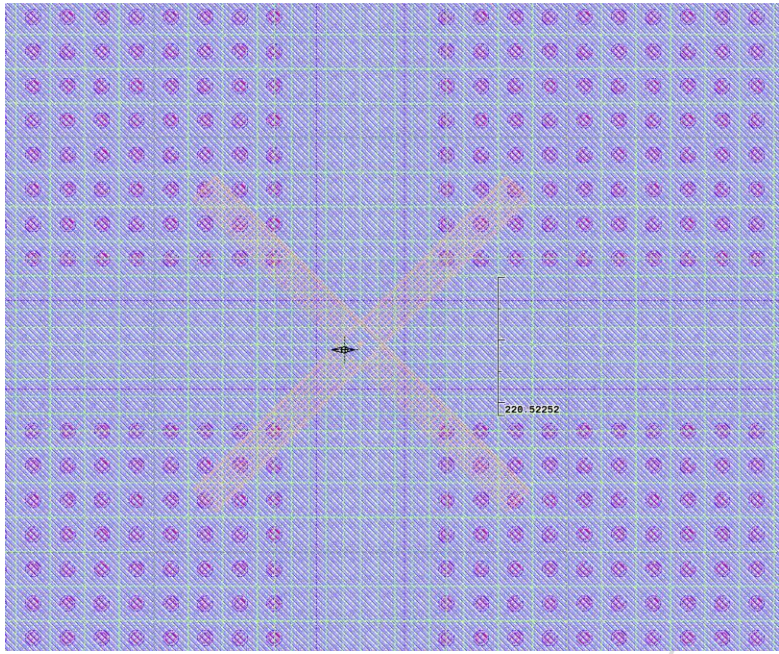
- Timepix4 with TSV allows for the seamless tiling of ASIC on a large sensor, eliminating large gaps and keeping the ASIC in the acceptance

- we are working in partnership with Advafab, ORNL is financing the production of sensors exploiting the TSV
  - Production of Thick (1 mm), and Thin(250 µm) bumped sensors with Thin Entrance Window
    - **Single ASIC for prototyping**
    - **2x2 or Quad sensors (5x5 cm^2)**
    - **3x3 or Nonuplet sensor (7.5x7.5cm^2)**
  - Flip-chipping of TSV ASICs to sensors. (10x singles, 6x quad, 9x nonuplets)





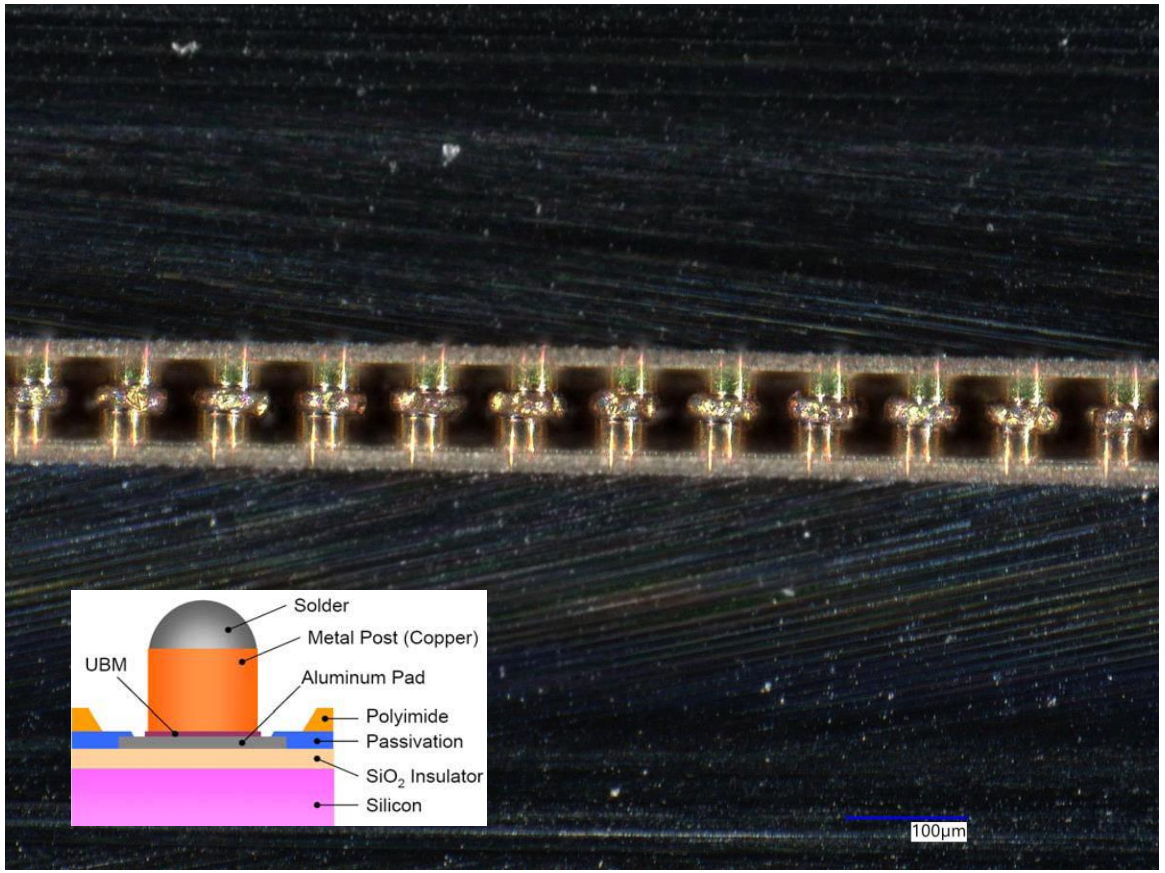


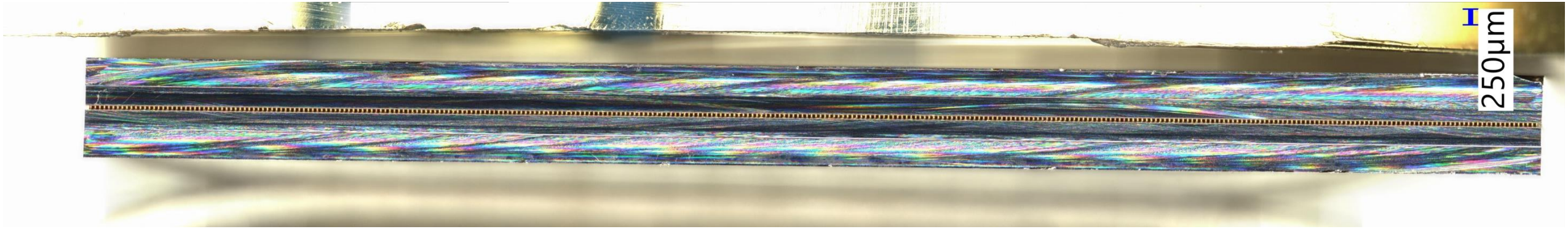


Copper Pillars trials

- FC150 Flip-Chip bonder installed and commissioned at ORNL
- We repeated the trials with Medipix4 ASICs performed at the Flip-Chip vendor
- Medipix4 processed with **Copper pillars by Winstech** in Taiwan
  - Promising low-cost process on 300mm wafers
  - First trial have excellent yield <1um height uniformity

- We bonded two Medipix4 together
  - Not the intended use but 1-on-1 bonding facilitate things
  - Focus on optimizing temperature and force parameters during bonding
  - First optical inspection show excellent parallelism
  - Small slip in alignment, observed on previous sample, need better heating during contact





https://indico.cern.ch/event/1439336/contributions/6261676/attachments/2978870/5244628/drd3_extra_results.pdf

Other 3D Integration project at ORNL

University of Sherbrook and ORNL are working together with Teledyne DALSA on the fabrication of 3D integrated Photon-Digital-Counter (PDC)

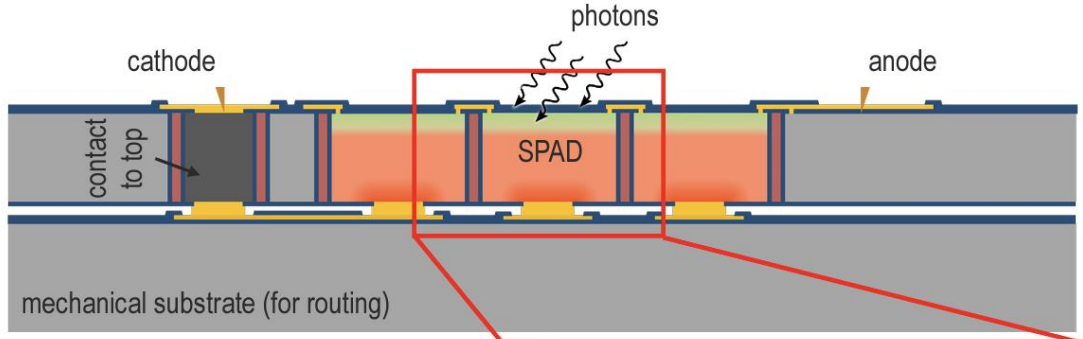
- Project relies on TSV processing of the SPAD wafer and eutectic Al-Ge Wafer to Wafer bonding for interconnection to the ASIC

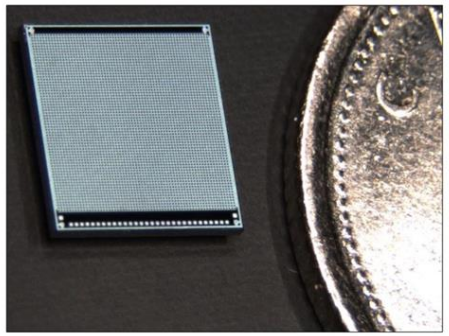
The Next generation of PDC hope to rely on the 65nm process with 300mm wafers

- SPAD wafers on 6 inches
- Need to core down wafer to do bonding

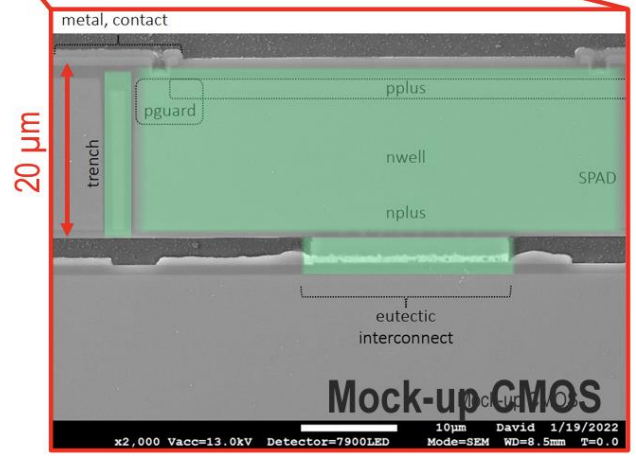
ORNL and UdS will investigate together the possibility of doing die to die bonding in ORNL FC150

- Flip-Chip bonder well within specs for this bonding
- Must verify effect of oxidation on bonds
- We may need to develop a etching process as well to pre-treat the dies before bonding





3D SPAD array
(canadian 10¢ for reference)



SEM cross section image

S. A. Charlebois[1], S. Martel[2], L. Fabris[4], F. Retière[3], J.-F. Pratte[1]

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Anisotropic conductive glues

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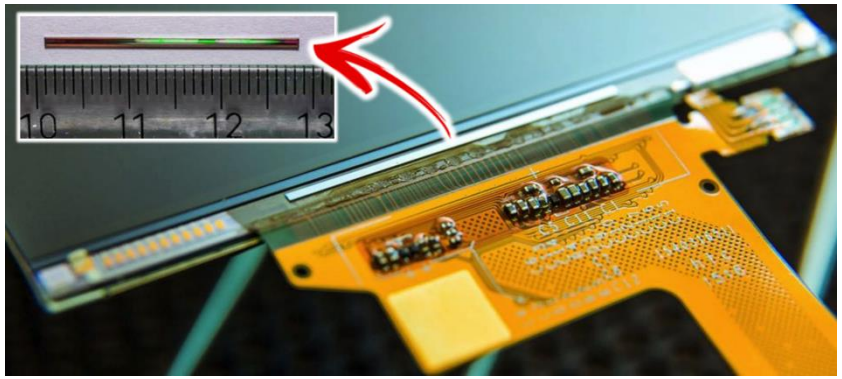
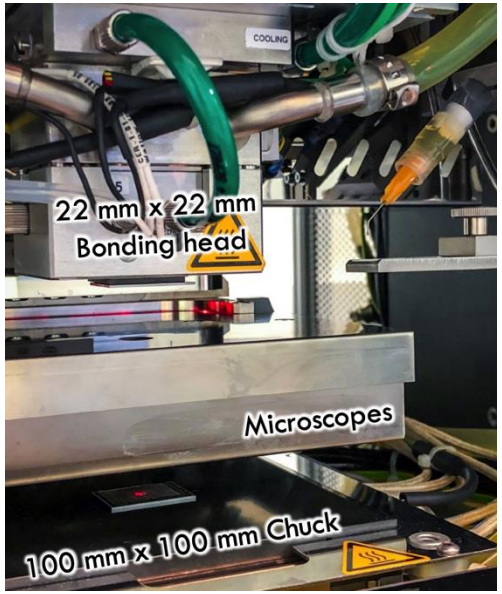
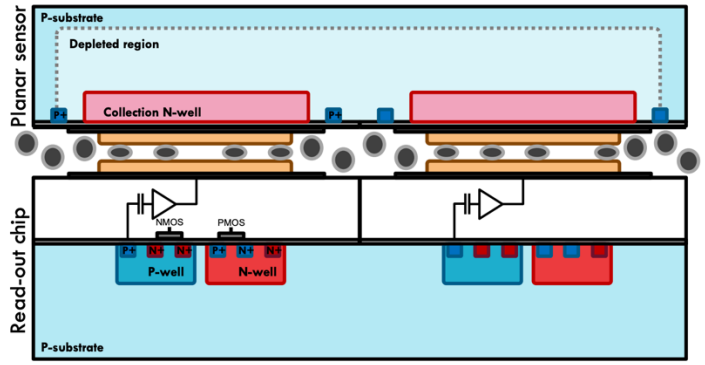
Anisotropic Conductive Films (ACF)

ACF is a technology developed for the LCD Display industry to connect drivers to each pixel row. Next step in the industry is µLED, which are driven individually and can measure as little as 15x15µm^2. Medipix and CLIC have been working with industry partners to adapt this process to pixel sensors

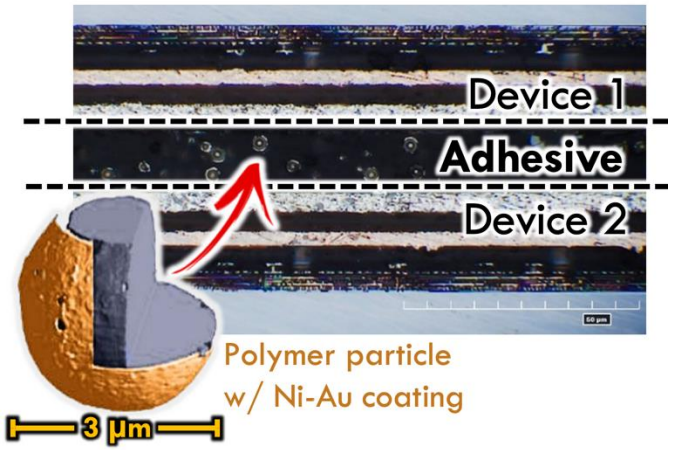
- Low cost, no lithography involved
- Wafer processing for pillar (ENIG) can be done in house with modest equipment







Bonding cross-section



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FC150 Flip-Chip bonder

FC150 Automatic Flip-Chip Bonder

± 1 µm post-bond accuracy and 20 µradian leveling

Up to 150 mm substrate and chip bonding for chip-to-chip and chip-to-wafer bonding

Bonding force up to 2000 N and temperature up to 400 $°C$

Active leveling using laser alignment and auto-collimation

Fully automated bonding process capable

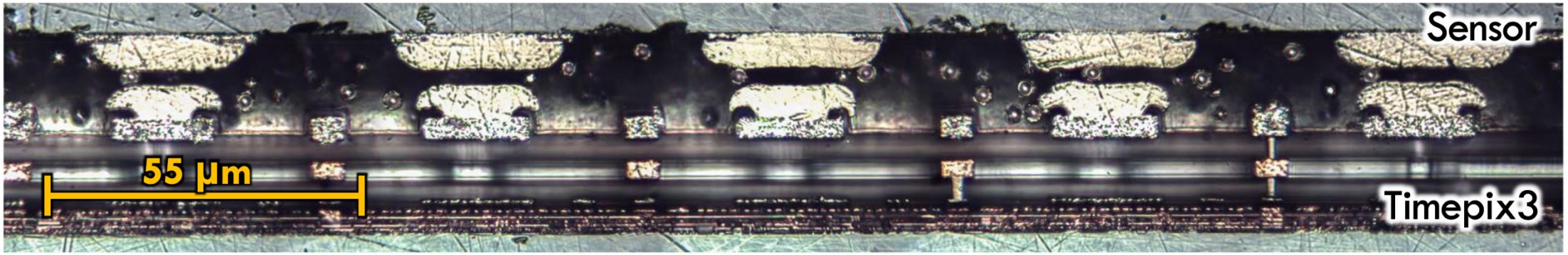
High-precision fluid dispenser integrated for accurate fluid application during bonding

$2M investment from ORNL on prober and flip-chip lab

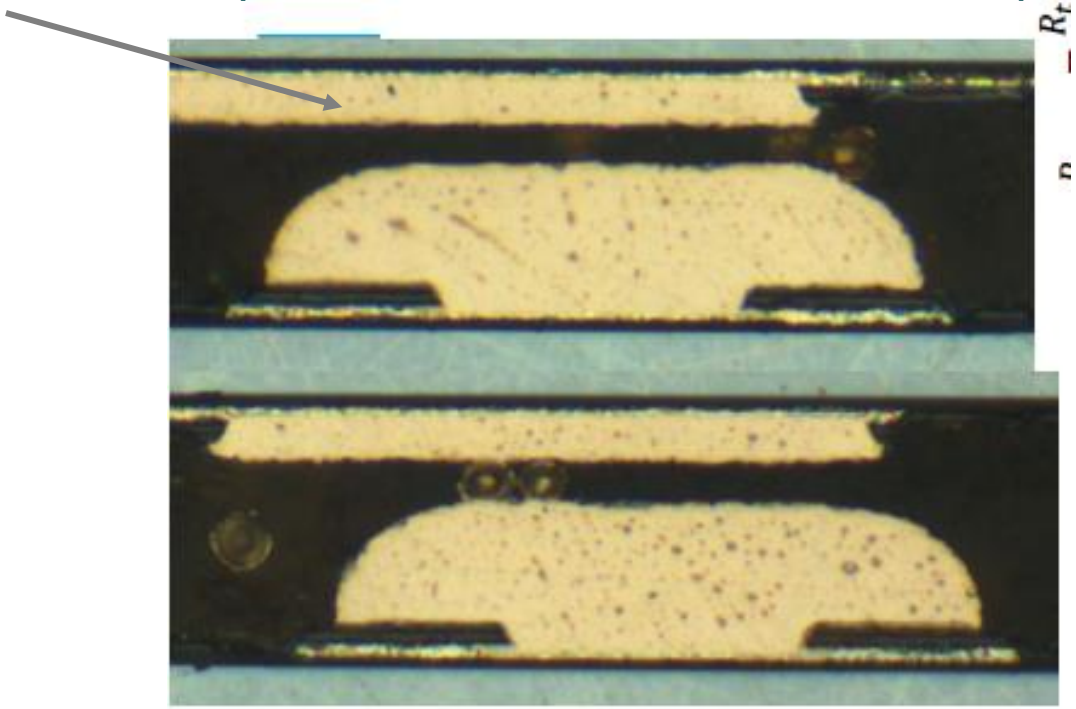
ACF results

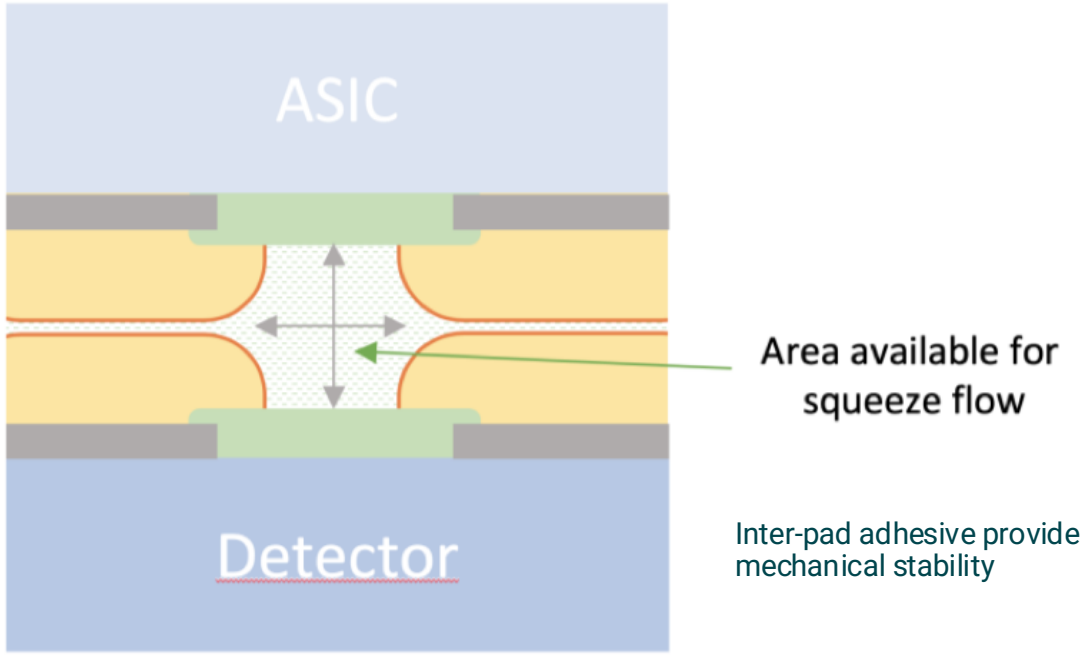
Ahmet Lale, DRD 3 Collaboration meeting, https://indico.cern.ch/event/1439336/contributions/6242532/

Timepix3-ACF-sensor assembly cross-section



Pads can be planarized via Chemical-Mechanical polishing





Inter-pad adhesive provide mechanical stability

Figure 9: Bump height and available area for squeeze film flow

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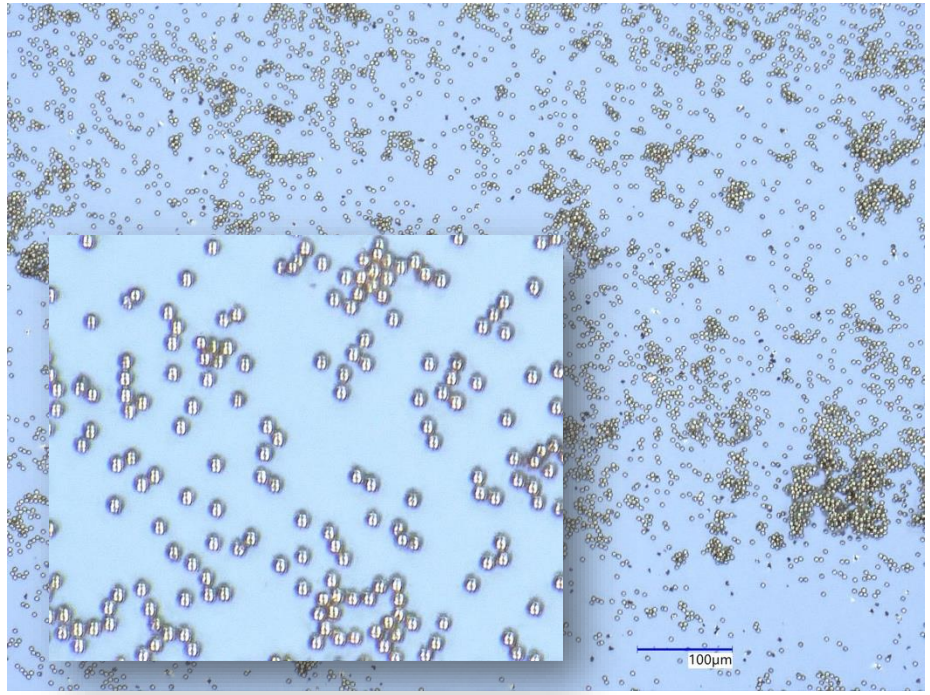
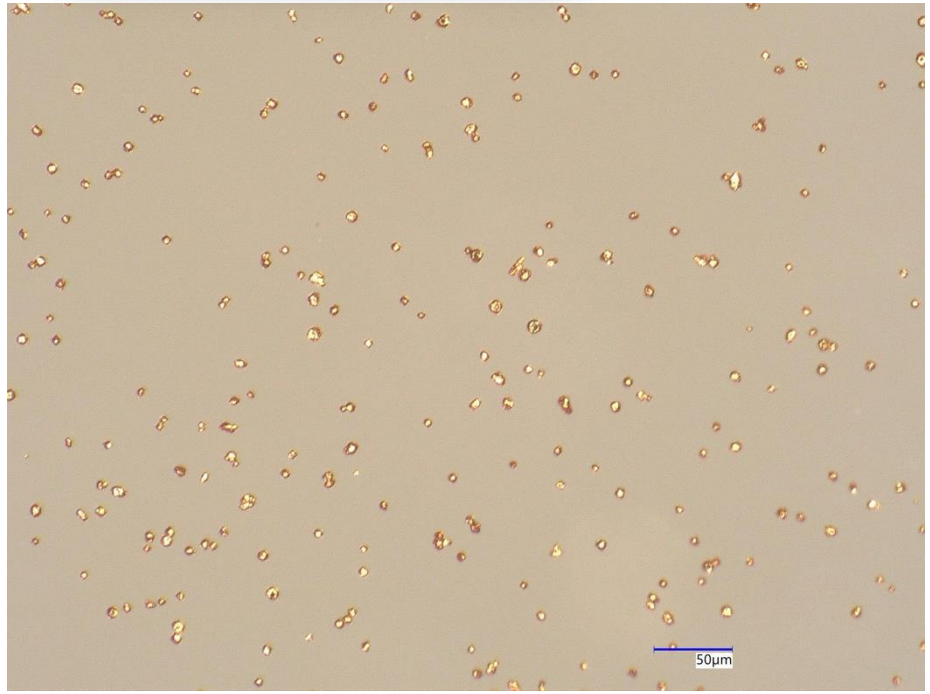
ACP Fabrication at ORNL

- We have started using ACP from various manufacturer to evaluate achievable pitch and reliability, handling, throughput etc.
- A much cheaper and efficient solution is to mix and fabricate our own ACP from particles from various vendors
- We can select the most appropriate matrix glue for our application, for example for radiation hardness
- Give access to more glues that have short lifetime for example





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Gold stud bonding

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Gold stud bonding

Gold stud bonding is a low-cost method for bonding dies with moderate pitch (> 100 µm)

A gold pillar, which is essentially the first end of a gold ball bond, is deposited and cut short on the pad

This pillar can be further planarized by pressing against a surface, or used as is.

The bonding can be done in a flip-chip with heat and force, applying a non-conductive underfill glue to provide mechanical adhesion

Gold stud bumping at ORNL

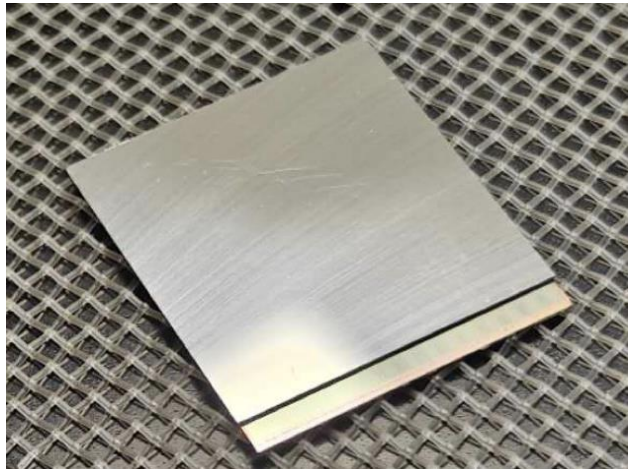
Gold-stud hybridisation of ALTIROC3/A and LGAD sensors

- Using ALTIROC3/A ASICs and LGAD sensors from ATLAS High-Granularity Timing Detector (HGTD) to develop new in-house bonding process for sensor and ASIC qualification
- Single and stacked double gold studs used for the connections between the chips, epoxy underfill for bonding
- Used for radiation-hardness qualification of LGAD sensors
- Low temperature process (60°C) to avoid uncontrolled annealing

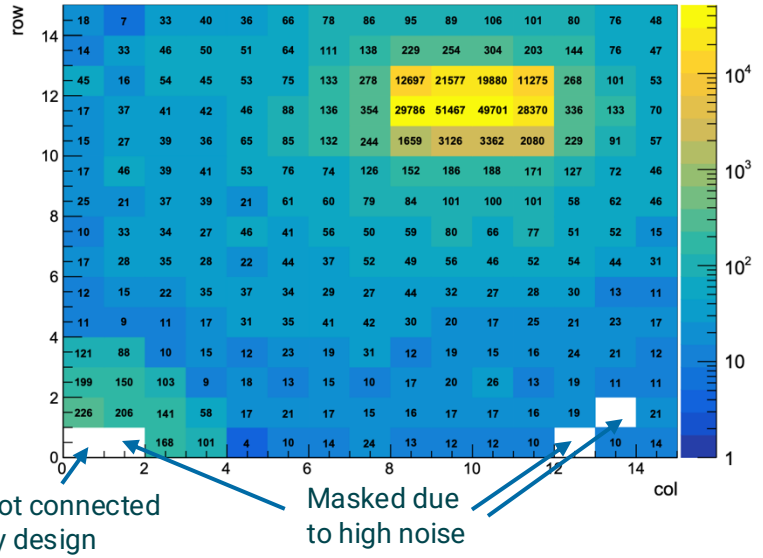
Gold studs are deposited one by one

https://www.youtube.com/watch?v=ICRDBpmev4o&t=42s&ab_channel=TPT-Wirebonder

ALTIROC/LGAD Hybrid
Flip-chip done with NCP (Araldite 2011)



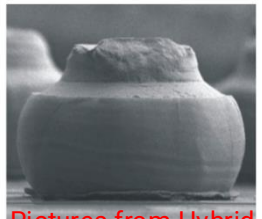
Test-beam occupancy map of ALTIROC with double gold studs + irradiated LGAD sensor

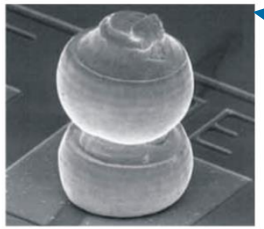


Confirmation of good inter-connection with occupancy map (≈ 100%)

Stacked Gold studs

Gold stud





Pictures from Hybrid SA

Preferred this solution to increase the gap between ASIC and sensor from 20 µm to 35 µm and thereby decrease coupling between them

- High connection yield, reproducibility, low temperature process
- Only for large pitch (>100µm), large pads (>80µm) chips

Ahmet Lale, DRD 3 Collaboration meeting,
https://indico.cern.ch/event/1439336/contributions/6242532/

Conclusion and perspective

- ORNL is working on developing bonding techniques for our sensor and module assembly needs
- There is a big gap in the industry when it comes to prototyping and small volumes, where it is hard to find ways to progress and obtain integrated modules
- We need partners in developing the best glues, particles, bump deposition process
- We need to develop capabilities for die-to-die bonding to empower R&D and fill the gap in this industry and provide solution for many detector systems