DAPHNE updates

Francesco Terranova on behalf of the DAPHNE developers
Univ. of Milano Bicocca and INFN

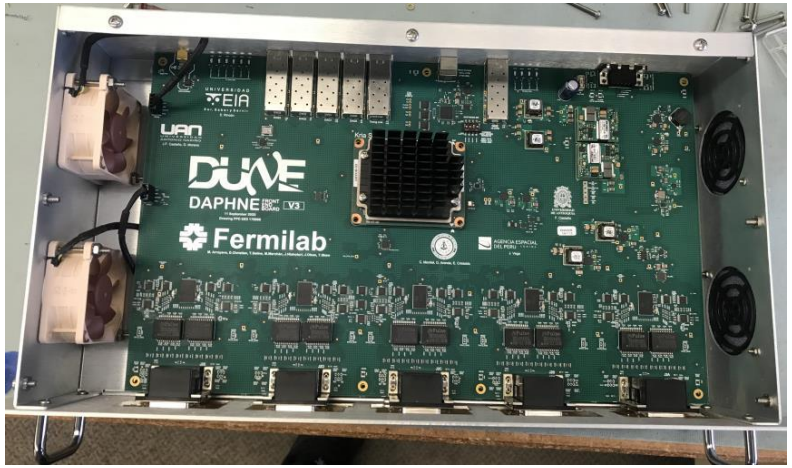
Consortium meeting

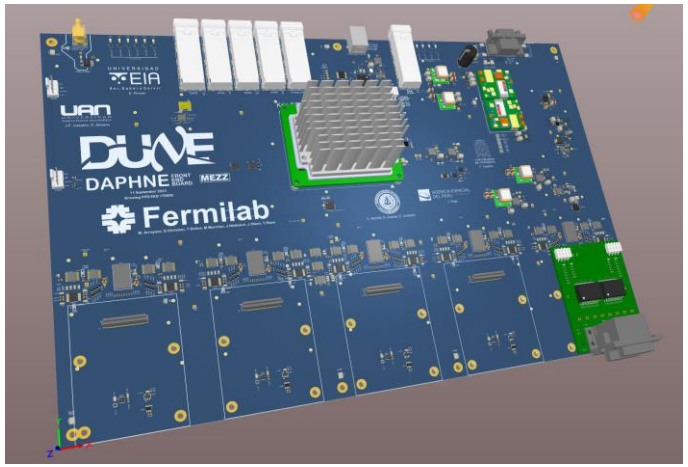
Dec 9, 2024

DAPHNE

The DAPHNE board is located outside the cryostat. It provides:

- Second stage signal amplification and shaping
- Signal digitization through a commercial 14-bit ADC and signal conditioning (AFE) operating at 62.5 Msps
- Onboard signal filtering, self-trigger algorithms, and dispatching of high-level information for trigger primitives in the event header
- DAQ interface using a 10 Gb/s ethernet link (final version: DAPHNE v3). It was a 4.8 Gb/s interfaced with FELIX in the previous version, now superseded





The DAPHNE pathway (Sep 2024)

At the last Collaboration Meeting we devised an integrated strategy to bring DAPHNE to PRR level for both the Horizontal (HD) and Vertical Drift (VD) detectors.

- DAPHNE v3 will provide all digital features of DAPHNE for both HD and VD. It is thus a **general-purpose motherboard**
- The interface to the cold electronics employs **four mezzanines** (i.e. internal plug-in-board)
    - an HD mezzanine board hosting the transformers (or opamp) and the input connectors of cold electronics
    - a mezzanine board hosting the second-stage amplifier and double-to-single-ended converter for the Hamamatsu (HPK) and FBK membrane electronics
    - a mezzanine board hosting the Signal-over-Fiber (SoF) receiver and second-stage amplification for the cathode tiles

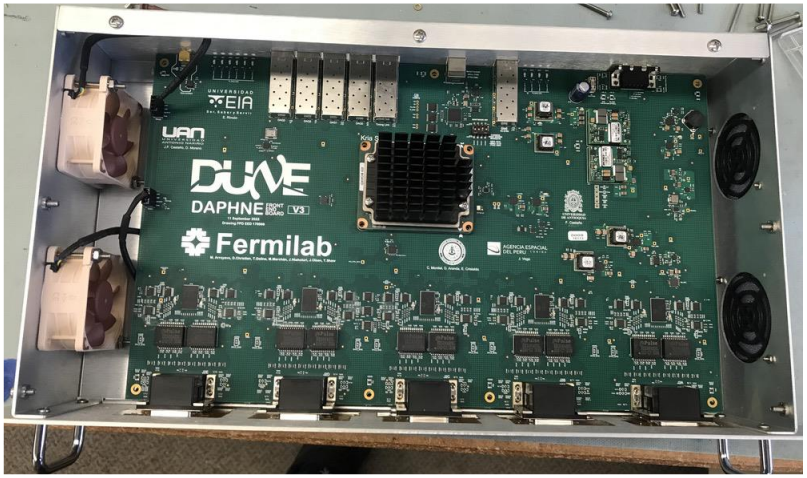
The advantage of the mezzanine approach is that it allows us to complete the development of the analog and digital parts in parallel using DAPHNE v2 and DAPHNE v3, respectively.

Task sharing

Development		
Item	**Main developer**	**Notes**
Motherboard (v3)	Fermilab	Support from INFN
Cathode mezzanine	France	Support from UCSB/FNAL/INFN
HD mezzanine	Italy	**NEW!** After the ProtoDUNE-HD test, we believe it can be used to replace the transformer and remove (<1%) the undershoot
HPK membrane mezzanine	UCSB/Fermilab	Cost covered by EU, as per MoU
FBK membrane mezzanine	Italy	
Firmware	Fermilab	Support from INFN and Spain on trigger algorithm and signal filtering (mostly for VD)
Trigger primitives	Spain	Support from INFN, Fermilab and DAQ
Support for installation and tests at CERN/labs and SURF	All	It includes also support from South America

Motherboard – DAPHNE v3 @CERN

- Two DAPHNE v3 has arrived at CERN in September and were tested in standalone mode with the DAQ



Team

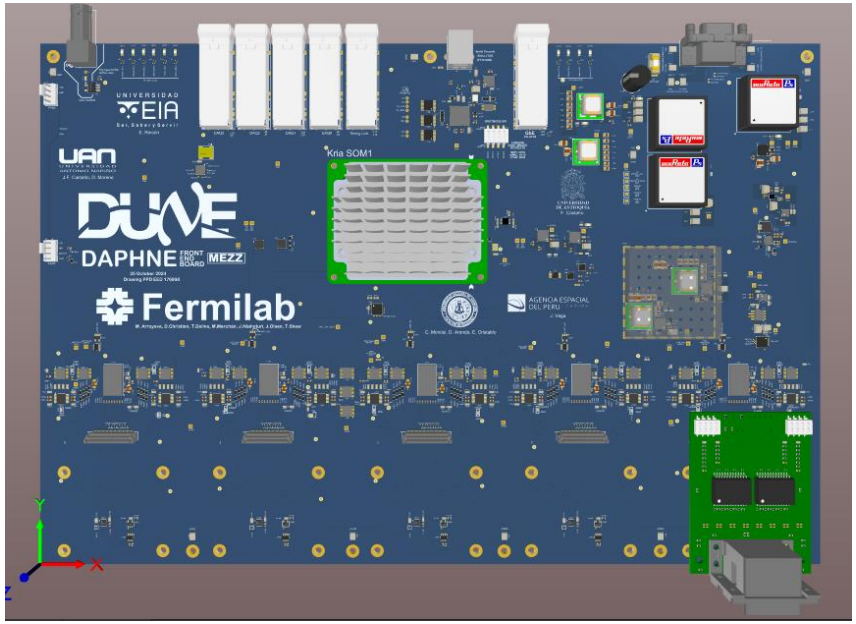
Board developers: J. Olsen, M. Marchan, T. Deline, J. Ntahoturi, T. Shaw, D. Christian (Fnal), P. Carniti (Mib),

Tests at CERN: M. Arroyave, T. Shaw (Fnal), E. Cristaldo (Mib)

- The analog part had still some production issues (immaterial for these tests).
- CERN Tests:
  - Timing fully commissioned.
  - Data senders under study due to clock instabilities.
  - Started working on the slow control configuration
  - Integration for the system in progress.

Motherboard– DAPHNE for ProtoDUNE-VD

We are producing a new 40-channel motherboard identical to DAPHNE v3 but without transformers. It provides power lines for the mezzanines. It will be available for the physics run of ProtoDUNE-VD and we usually call it “DAPHNE-VD” (even if it is an universal board)



Production status:

- Adjustments on the analog part embedded in the design
- Final design with power lines for mezzanine
- Production (12 boards)
- Tests at FNAL/CERN

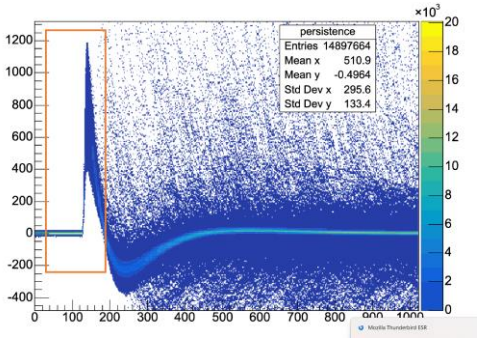
Mezzanines (I)

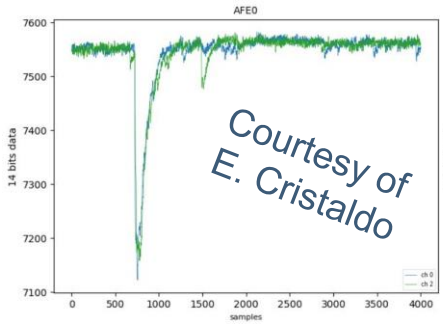
Mezzanine for FD1-HD and the FD2-VD FBK cold electronics: they are quite similar because they read the same cold amplifier (“HD-style”)

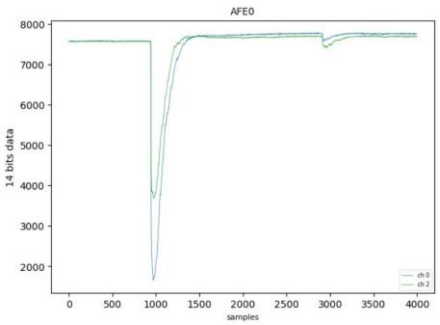
It has three stages:

- Differential to single-ended conversion (mandatory)
- Leading order undershoot compensation (mandatory)
- Second order (i.e. for the AFE) undershoot compensation (optional and maybe useful to be implemented in the motherboards)

This board was tested in ProtoDUNE-HD and offers a good signal response with negligible undershoot (<1%). Full analysis and comparison with standard transformer-based readout in progress.

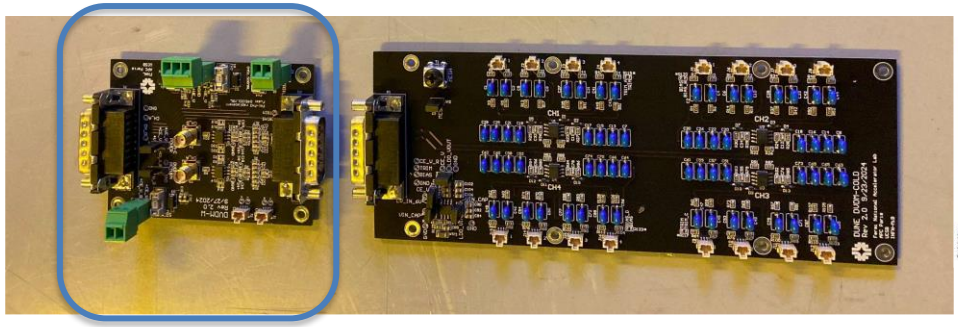


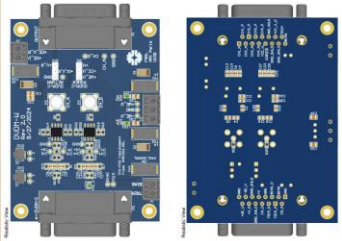




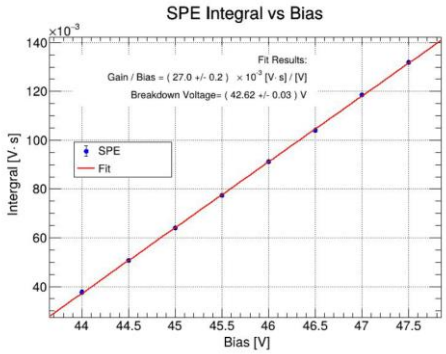
Mezzanines (II)

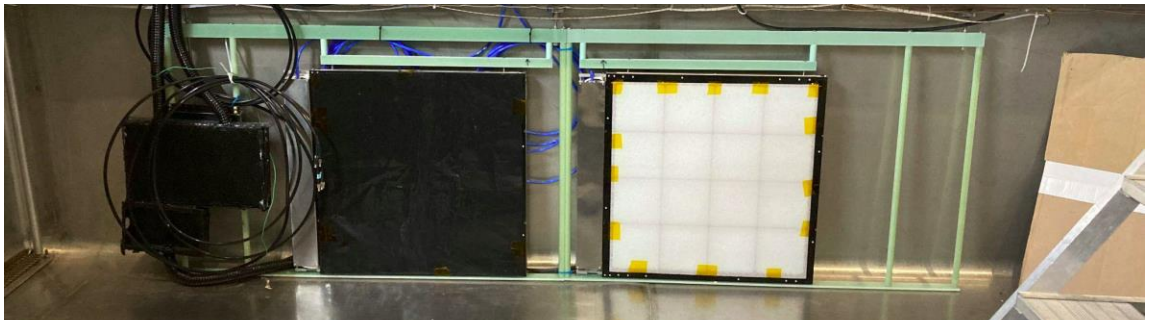
The mezzanine for the FD2-VD HPK cold electronics is now ready for test in the Coldbox and has been tested in the CERN test stand with membrane tiles equipped with HPK sensors.





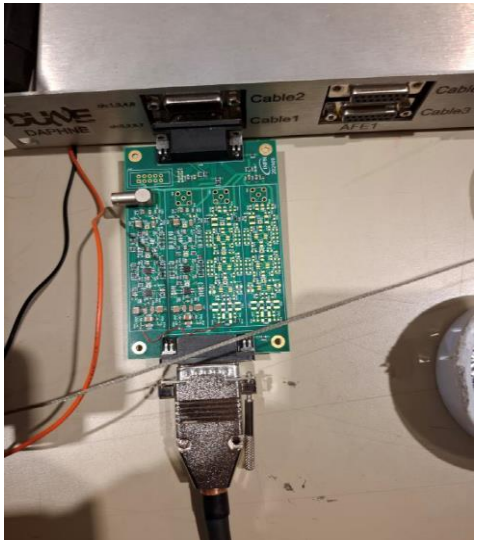
- It performs the double-to-single ended
- It may further benefit from the AFE undershoot compensator (under evaluation)

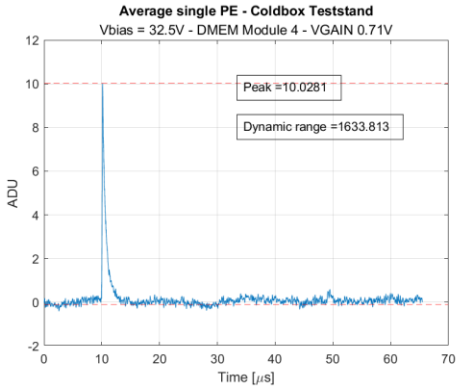


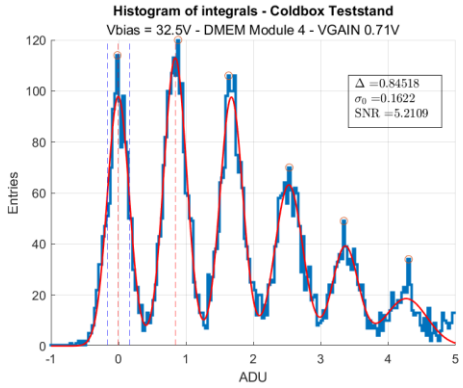


Cold box test of the mezzanines

The cold box that is going on right now is a good testbench for all the mezzanines, included the nearly-final version of the **SoF receiver** (8 channel). The only drawback is that the available DAPHNE is v2, and the mezzanines are external daughterboards with patched power lines







Status:

- Test of the tiles in the test-stand
- DAPHNE-v2 connected to DAQ
- Data taking: in progress

Trigger

An impressive amount of work done using ProtoDUNE-HD as testbench!

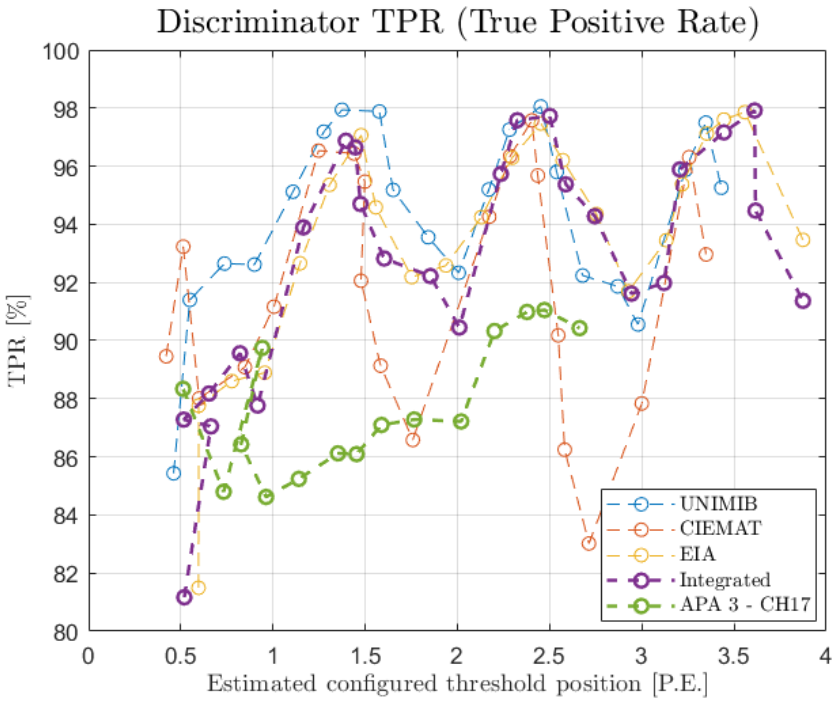
Task	Status	Notes
Development of self-trigger algorithms	Completed	3 types: CIEMAT, EIA, UniMiB
Test in labs and ProtoDUNE-HD	Completed	
Deployment of the final self-trigger algorithm (“Integrated”)	Completed	It merges features of the three algorithms
Test in ProtoDUNE-HD	Completed	(see next slides)
Header for trigger primitives	Completed	CIEMAT with support from Fermilab and Unimib
Implementation in DAPHNE V3	To be done	
Test in ProtoDUNE-VD	To be done	

Team: M. Arroyave, D. Ávila, E. Cristaldo, F. Galizzi, I. López de Rego, J. Soto

Trigger: what's next

Self-trigger at 1.5 p.e. is the default option for FD1-HD but not for FD2-VD, where we plan self-trigger at 0.5 p.e. plus a global high-level trigger based on primitive. In addition, there are a few issues to be solved.

In ProtoDUNE-HD, there is a single p.e. rate much higher than expectation. This is likely a local effect that won't be present at SURF. The "integrated" trigger algorithm suffers from this rate due to the undershoot. **This is why we are planning to remove the undershoot (i.e. the transformer) even in FD1-HD**



DAPHNE is already equipped with 0.5 p.e. triggering capability but the L2 trigger based on primitives is still work in progress and will be one of the main goal of the ProtoDUNE-VD run.

Conclusions

- In fall 2024, the Consortium decided a common strategy for DAPHNE in FD1-HD and FD2-VD, which is based on a universal motherboard (DAPHNE V3 with a new analog front end that removes the transformers and add power lines) plus four types of mezzanines (HD, VD-FBK, VD-HPK, VD-Cathode/SoF)
- The implementation of this strategy is now in full-swing and turned out to be very effective
- Universal motherboard:
  - DAPHNE V3 firmware and DAQ interface in good shape
  - DAPHNE for ProtoDUNE-VD will likely be the final version for FD1 and FD2
- Mezzanines:
  - The HD flavor was tested in ProtoDUNE-HD, together with the standard readout and results are very promising
  - The FBK and HPK VD flavors are ready and under test at the coldbox
  - The Cathode flavor is being tested with FBK tiles and will be tested with HPK tiles at the next cold box in 2025 and in ProtoDUNE-VD
- Final self-trigger algorithm tested in ProtoDUNE-HD

We are in good shape to match the DAPHNE PRR in summer 2025