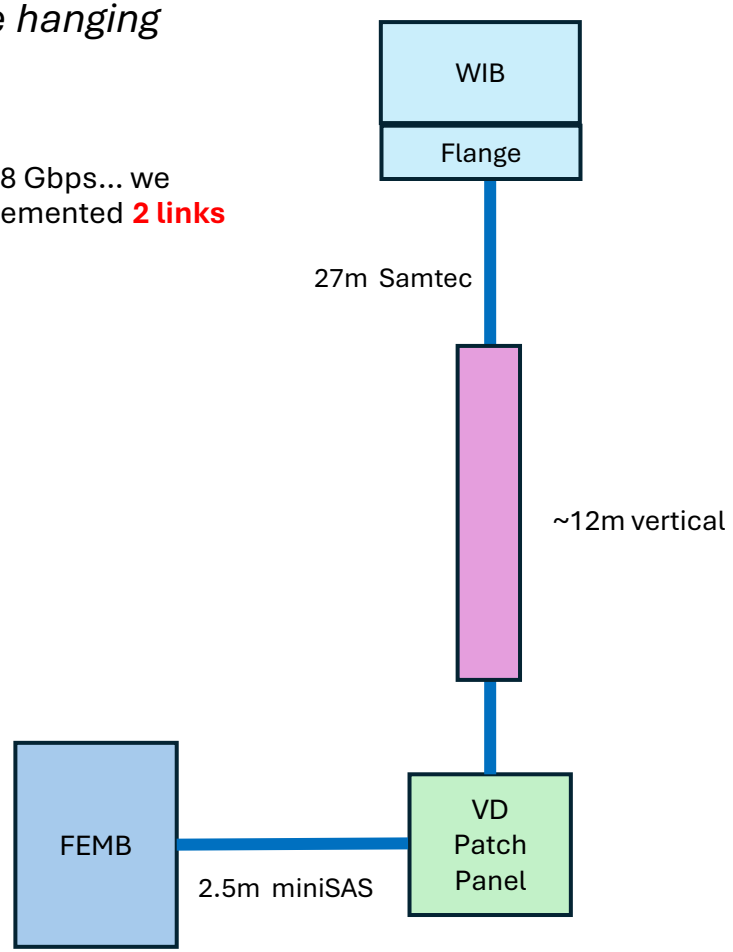
VD data cable BER test under Mechanical stress

Shanshan Gao on behalf of the BNL CE team

12/10/2024

Comment from The PDR of mechanical aspects of the CE (held in Feb. 2019)

- *Mechanical stresses on the CE twinax/clock cables can affect cable performance.*
  - *Tests should be done when the cables are constrained as expected, and when they are hanging unsupported for 12+ meters.*
  - *Tests should include a bit error rate test at 2.56Gbps.*
    - [At that point we had not decided on whether each COLDATA would have 1 link at 2.56 Gbps or 2 links at 1.28 Gbps… we subsequently modified the COLDATA design to use only one 62.5 MHz master clock & 512 ns/sample & implemented **2 links at 1.25 Gbps**.]

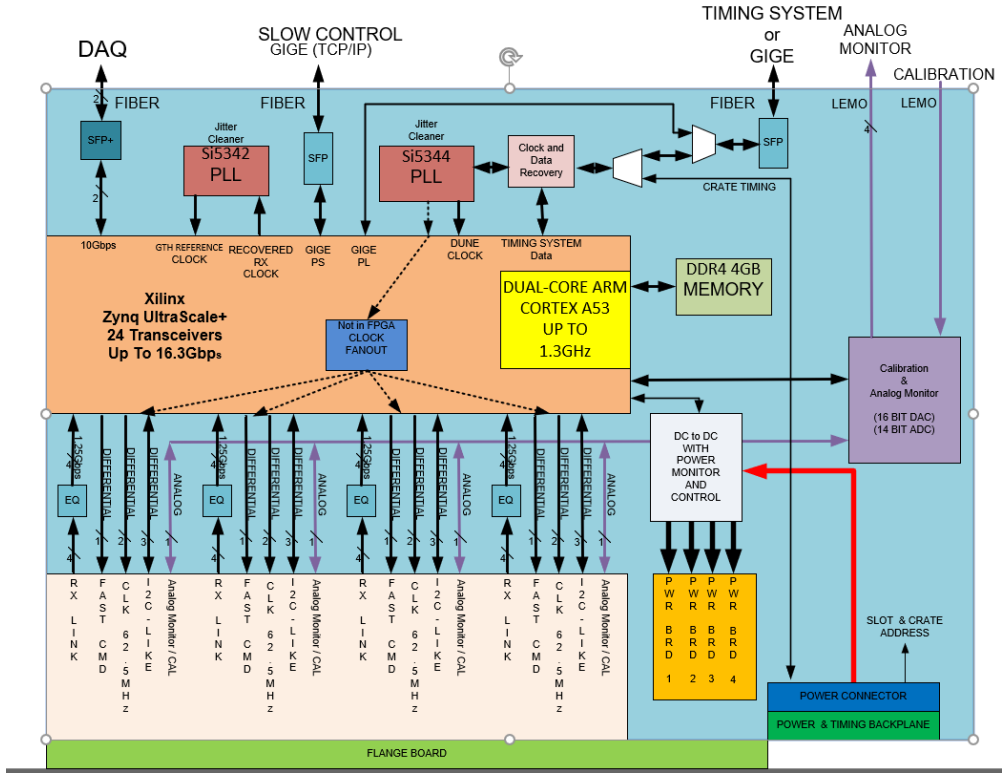


VD cable routing

- SAMTEC cables run from CE flanges to CRP patch panels. The cables are tied to the cable trays along the cryostat wall and laid down on the cryostat floor. When installing the bottom CRPs, the cables are then connected to CRP patch panels.
- The cables from bottom CRP are connected to the CE flanges and strain relieved on the CE cable brackets.

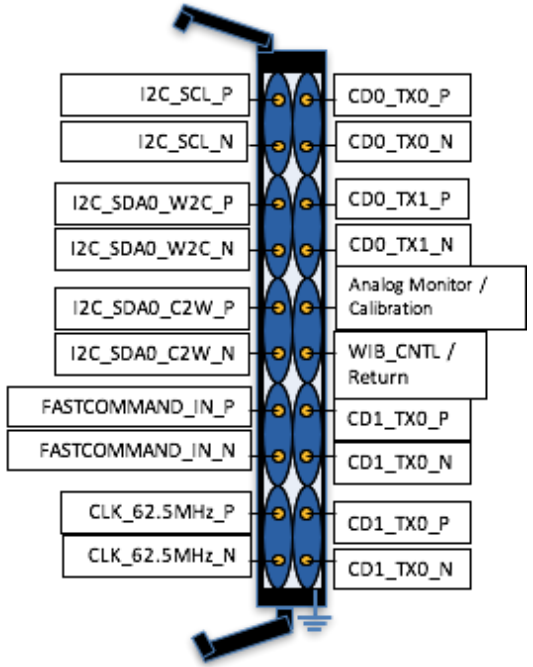
A test of data cable under stress was conducted at BNL.

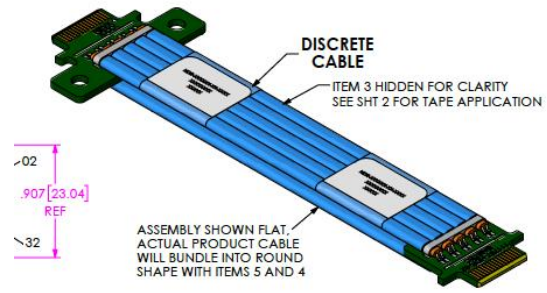
FEMB and WIB

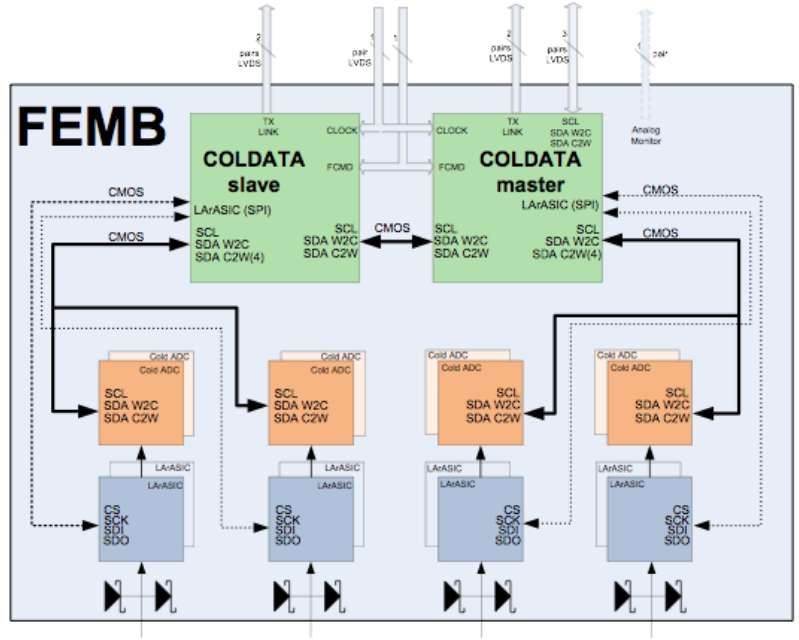


The FPGA receives data from 4 FEMBs through 1.25 Gb/s serial links with equalizer chips on board.

Signals over blue data cable





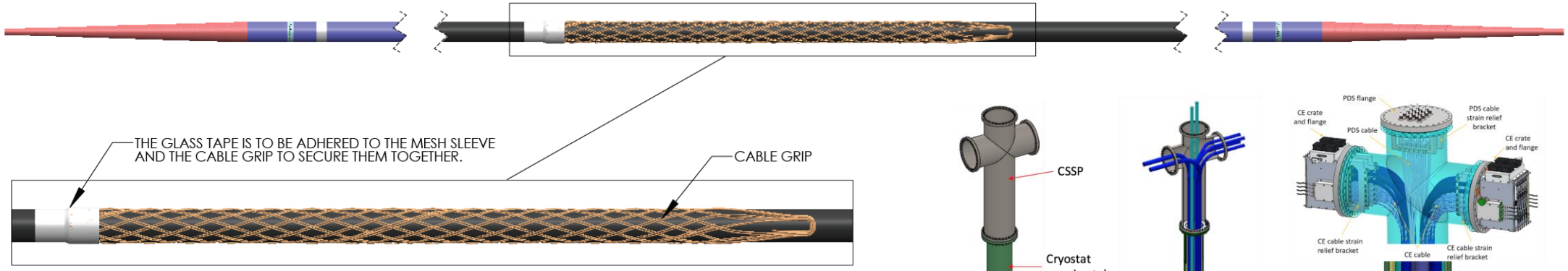


Signal name	Type	# of Pairs	IO Standard
4xData Links	Differential	4	LVDS
I2C_SCL	Differential	1	LVDS
I2C_SDA0_C2W	Differential	1	LVDS
I2C_SDA0_W2C	Differential	1	LVDS
FASTCOMMAND	Differential	1	LVDS
CLK_62.5MHz	Differential	1	LVDS
Analog Monitor / Calibration	Single ended	½	Analog
WIB_CNTL or GND	Single ended	½	1.8V CMOS or Return

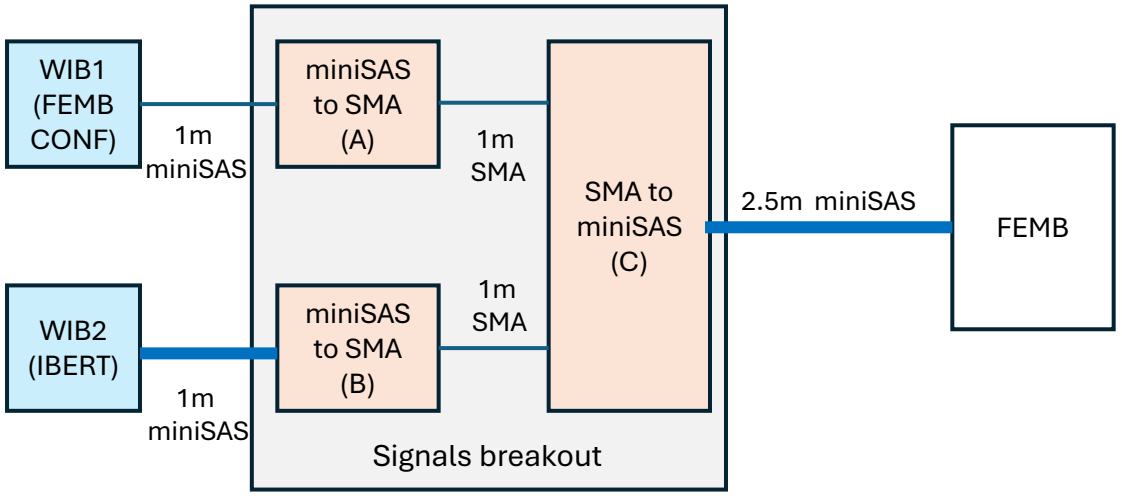
The weight of a 12-meter-long section of the cable bundle is approximately 40 kg. The cable bundle consists of 11 power cables, 11 data cables, and some SHV cables. The entire bundle is supported by a cable grip, which tightly holds the cables at the outer perimeter.

In a 2D close packing arrangement, about half of the cables will be positioned at the outer perimeter when 22 cables are grouped into a circular bundle. Assuming that 10 cables are directly gripped by the cable grip, each cable would bear an approximate load of 4 kg.

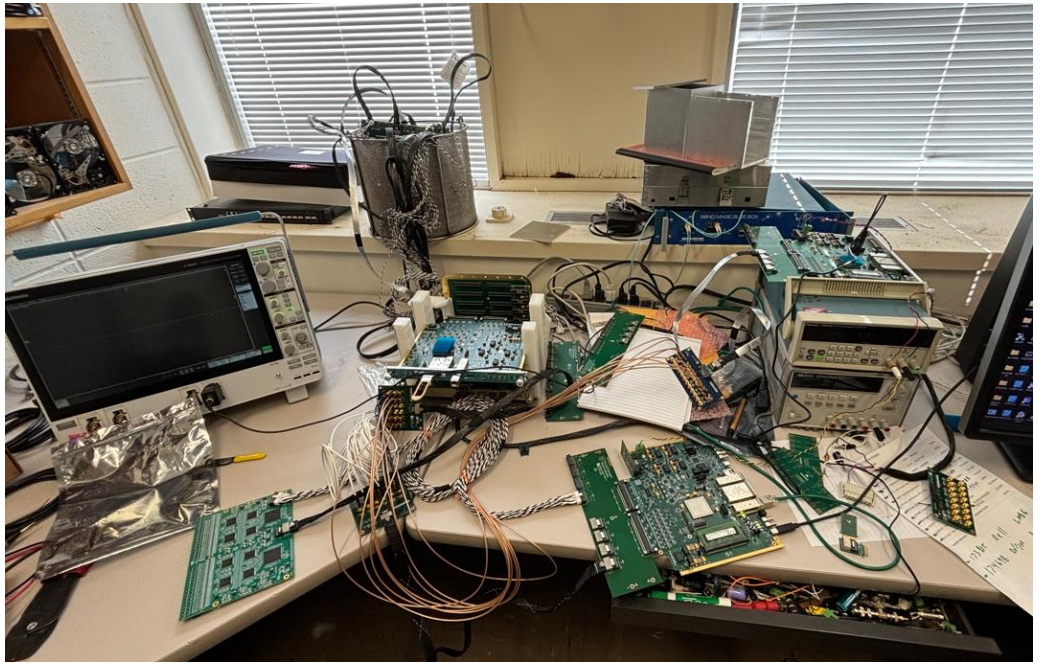
The additional 12 kg load applied during the cable test represents 30% of the total 40 kg weight of the cable bundle, which is three times the 4 kg load estimated for each cable.



Hardware setup (in Jack's room)

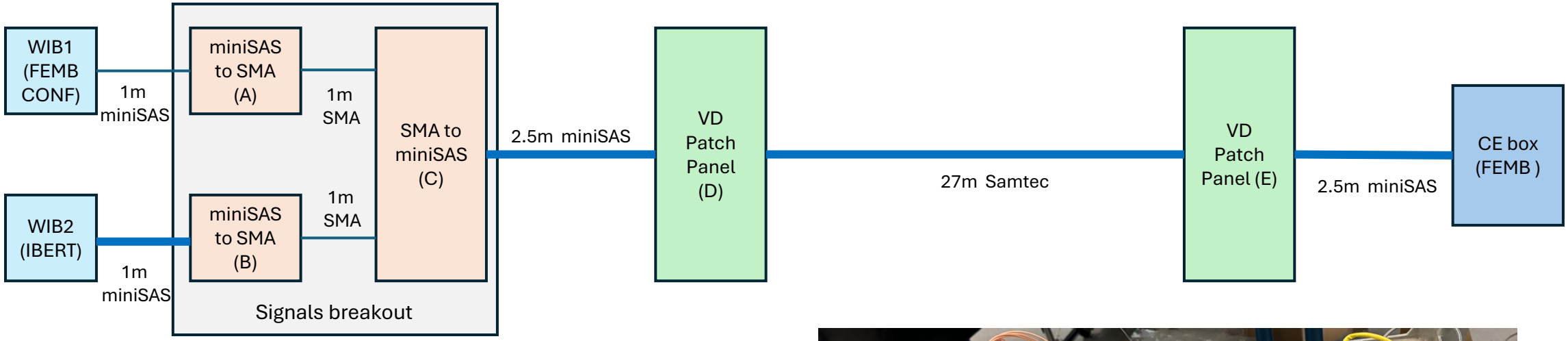


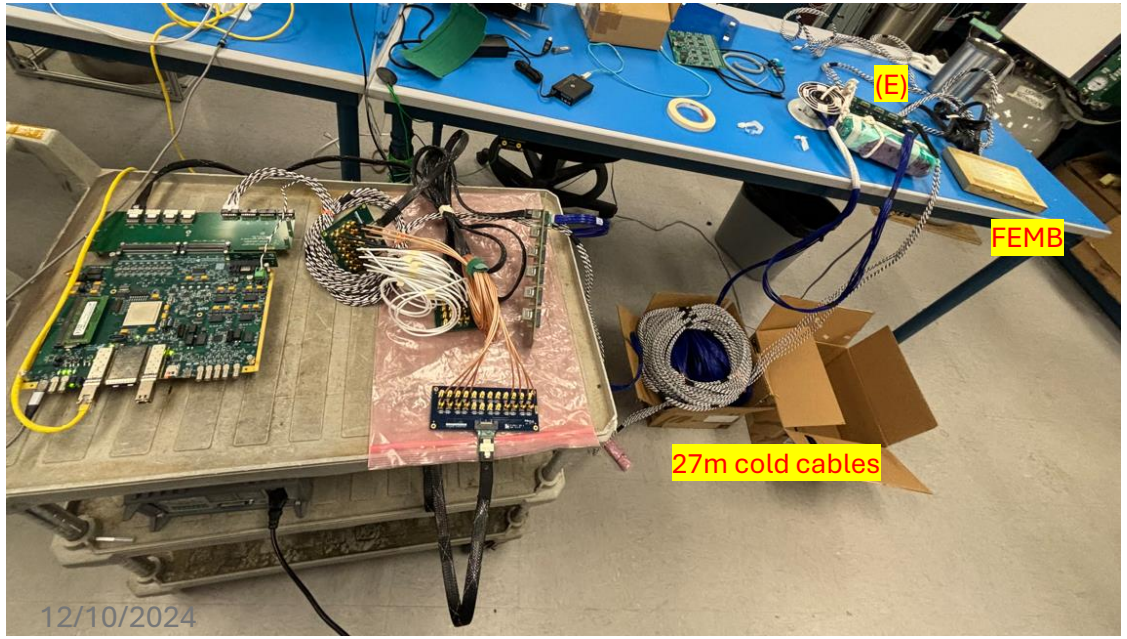
Note: both WIB1&WIB2 have a WIB adapter board

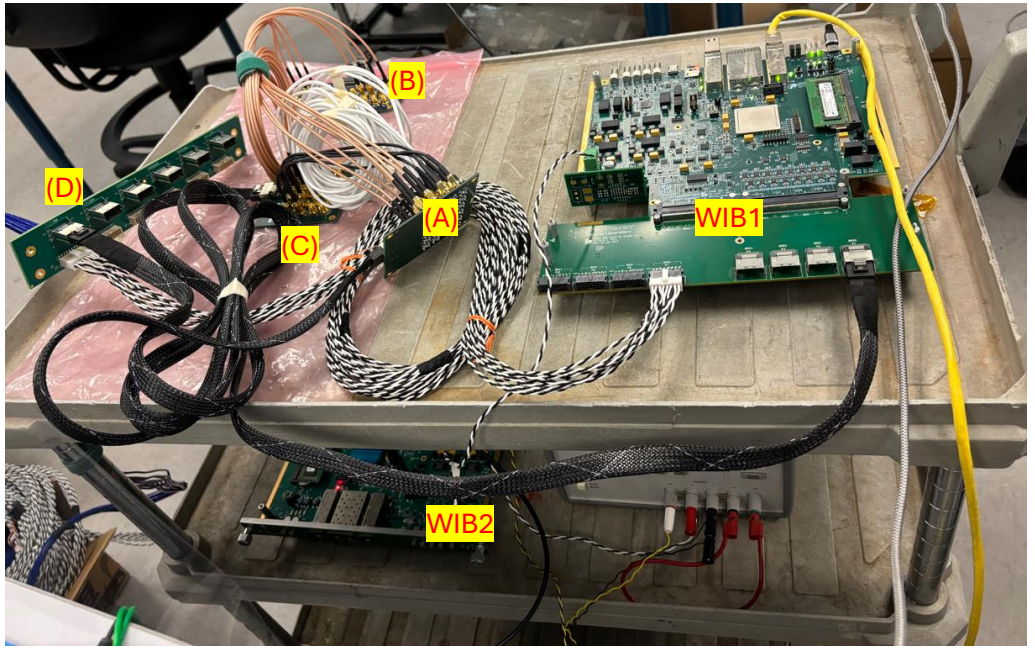


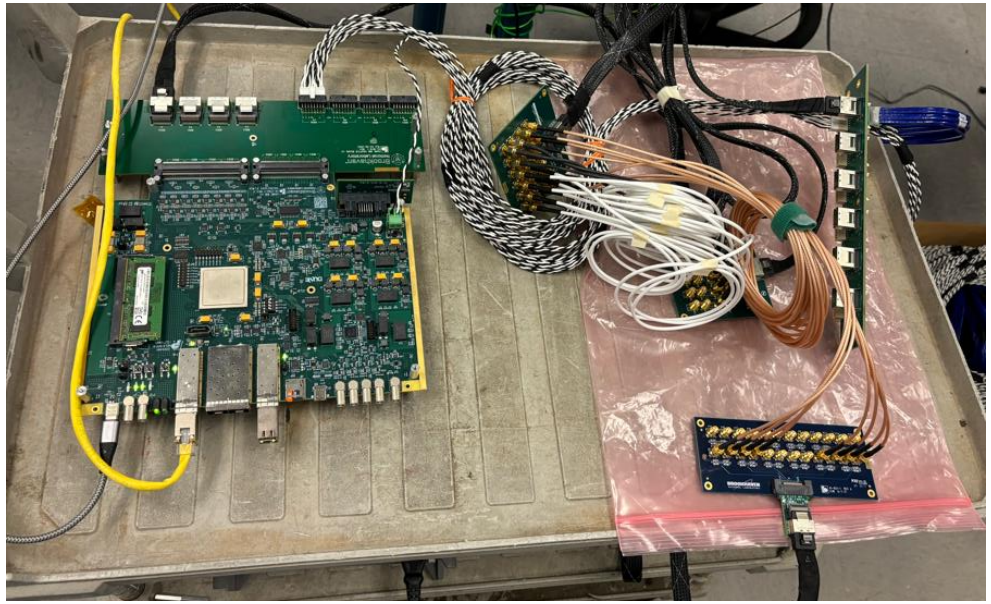
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Reset
Ungrouped Links (0)															
Link Group 0 (4)							Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	971 mV (11000)	☑	Inject	Reset
Link 0	MGT_X0Y12/TX	MGT_X0Y12/RX	1.251 Gbps	8.612E13	0E0	1.161E-14	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	971 mV (11000)	☑	Inject	Reset
Link 1	MGT_X0Y13/TX	MGT_X0Y13/RX	1.250 Gbps	8.612E13	0E0	1.161E-14	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	971 mV (11000)	☑	Inject	Reset
Link 2	MGT_X0Y14/TX	MGT_X0Y14/RX	1.250 Gbps	8.612E13	0E0	1.161E-14	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	971 mV (11000)	☑	Inject	Reset
Link 3	MGT_X0Y15/TX	MGT_X0Y15/RX	1.253 Gbps	8.612E13	0E0	1.161E-14	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	971 mV (11000)	☑	Inject	Reset

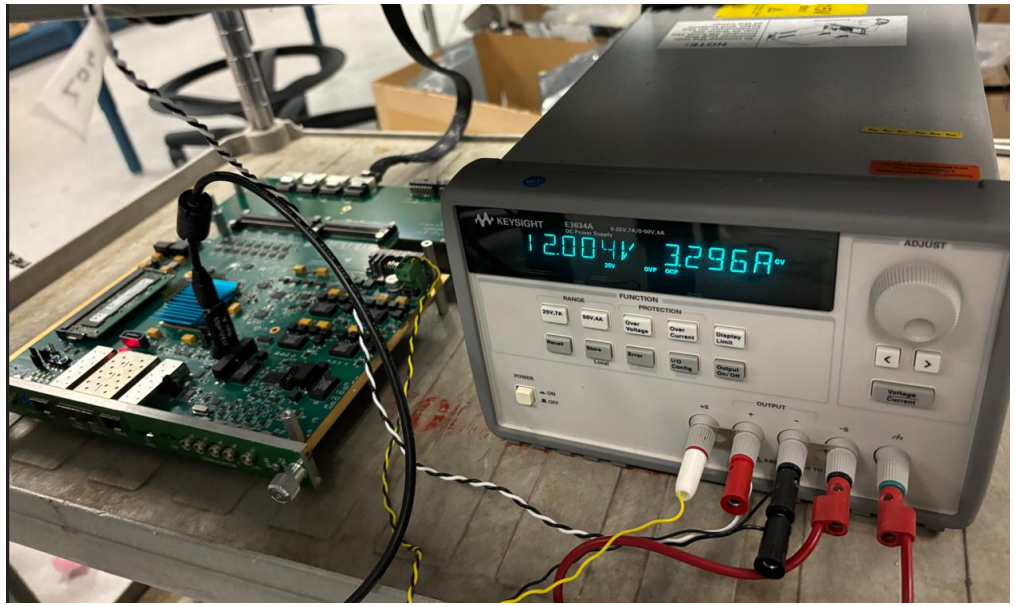
Final setup in room 1-216

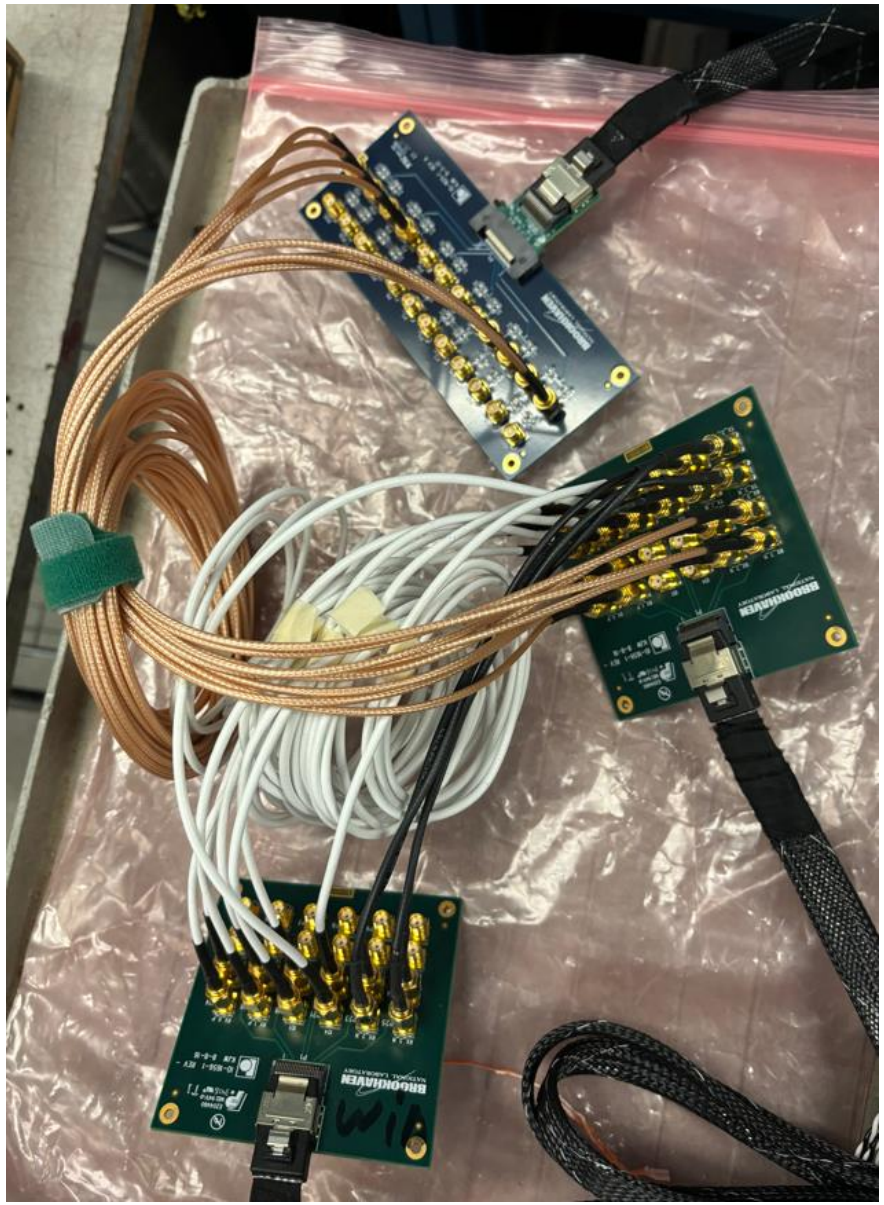









KEYSIGHT
E3634A
12.004V
3.296A
ADJUST
FUNCTION
OUTPUT


BROOKHAVEN

BER result from room 216 (BER < 1E-13)

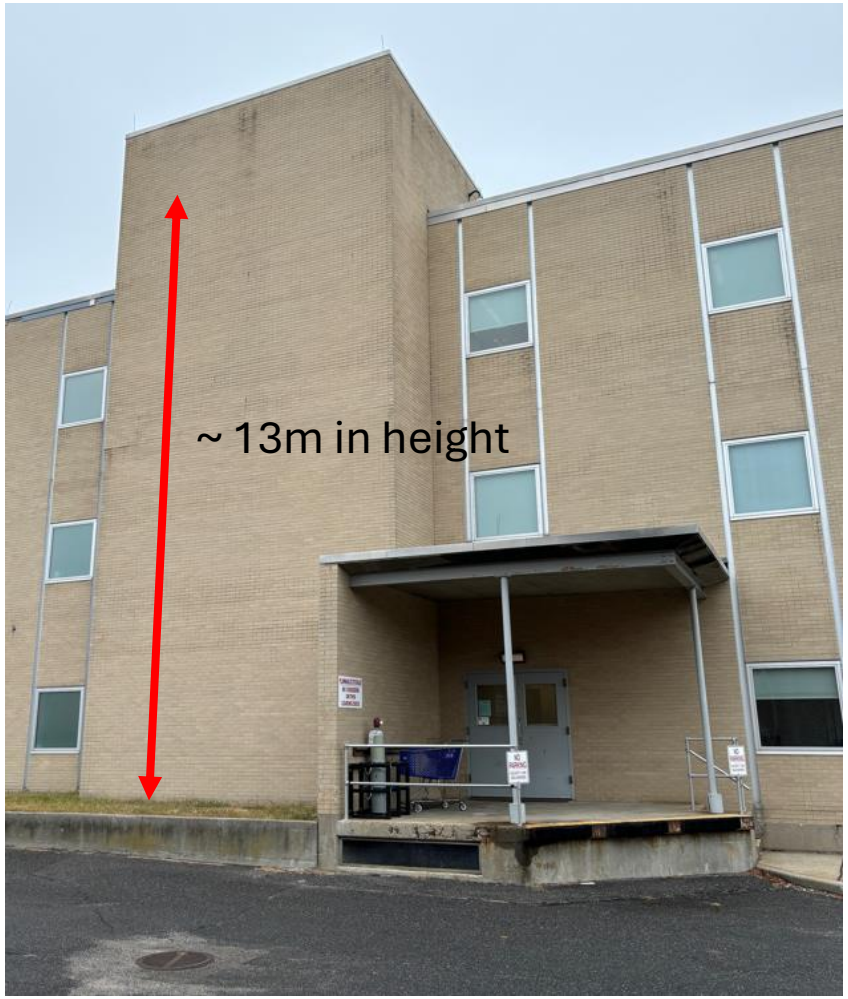
Tcl Console | Messages | **Serial I/O Links** | Serial I/O Scans

Name	TX	RX	Status	Bits	Errors	BER	BERT Re...	TX Pattern
Ungrouped Links (4)								
Link 0	MGT_X0Y12/TX	MGT_X0Y12/RX	1.251 Gbp	1.001E13	0E0	9.992E-14	Reset	PRBS 7-bit
Link 1	MGT_X0Y13/TX	MGT_X0Y13/RX	1.250 Gbp	1.001E13	0E0	9.992E-14	Reset	PRBS 7-bit
Link 2	MGT_X0Y14/TX	MGT_X0Y14/RX	1.247 Gbp	1.001E13	0E0	9.994E-14	Reset	PRBS 7-bit
Link 3	MGT_X0Y15/TX	MGT_X0Y15/RX	1.253 Gbp	1.001E13	0E0	9.988E-14	Reset	PRBS 7-bit

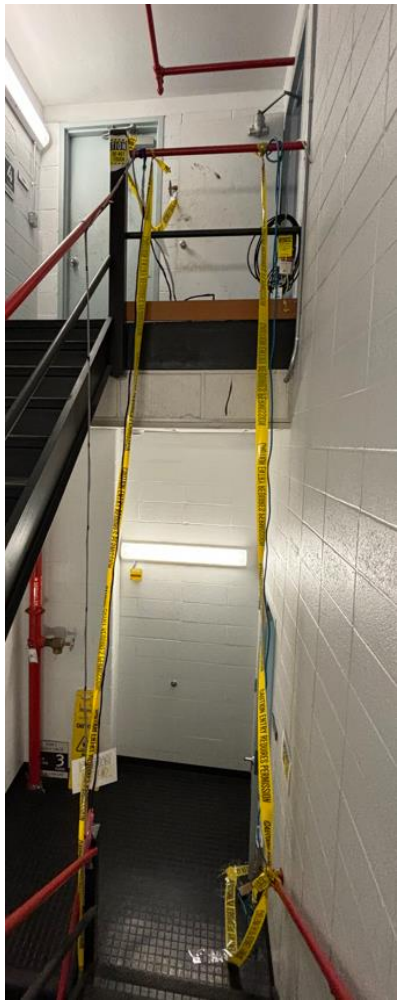
Tcl Console | Messages | **Serial I/O Links** | Serial I/O Scans

Name	TX	RX	Status	Bits	Errors	BER	BERT Re...	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enab...	Inject Er...	TX Reset	RX Reset	RX PLL Sta...	TX PLL Sta...	Loopback Mode
Ungrouped Links (4)																			
Link 0	MGT_X0Y12/TX	MGT_X0Y12/RX	1.251 Gbp	1.001E13	0E0	9.992E-14	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	971 mV (11000)	☑	Inject	Reset	Reset	Locked	Locked	None
Link 1	MGT_X0Y13/TX	MGT_X0Y13/RX	1.250 Gbp	1.001E13	0E0	9.992E-14	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	971 mV (11000)	☑	Inject	Reset	Reset	Locked	Locked	None
Link 2	MGT_X0Y14/TX	MGT_X0Y14/RX	1.247 Gbp	1.001E13	0E0	9.994E-14	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	971 mV (11000)	☑	Inject	Reset	Reset	Locked	Locked	None
Link 3	MGT_X0Y15/TX	MGT_X0Y15/RX	1.253 Gbp	1.001E13	0E0	9.988E-14	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	971 mV (11000)	☑	Inject	Reset	Reset	Locked	Locked	None

Location for this stress test



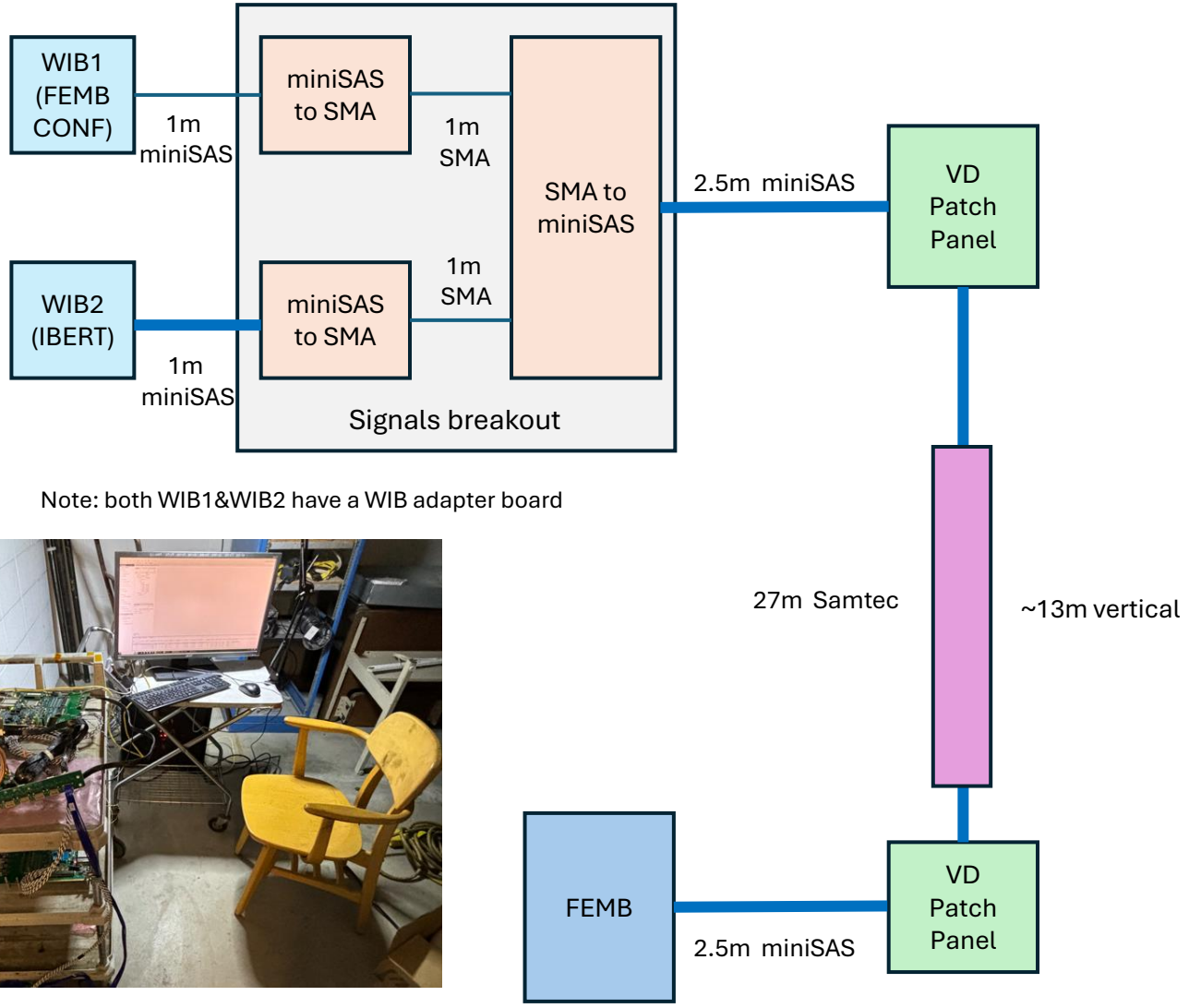
Building 510 at BNL



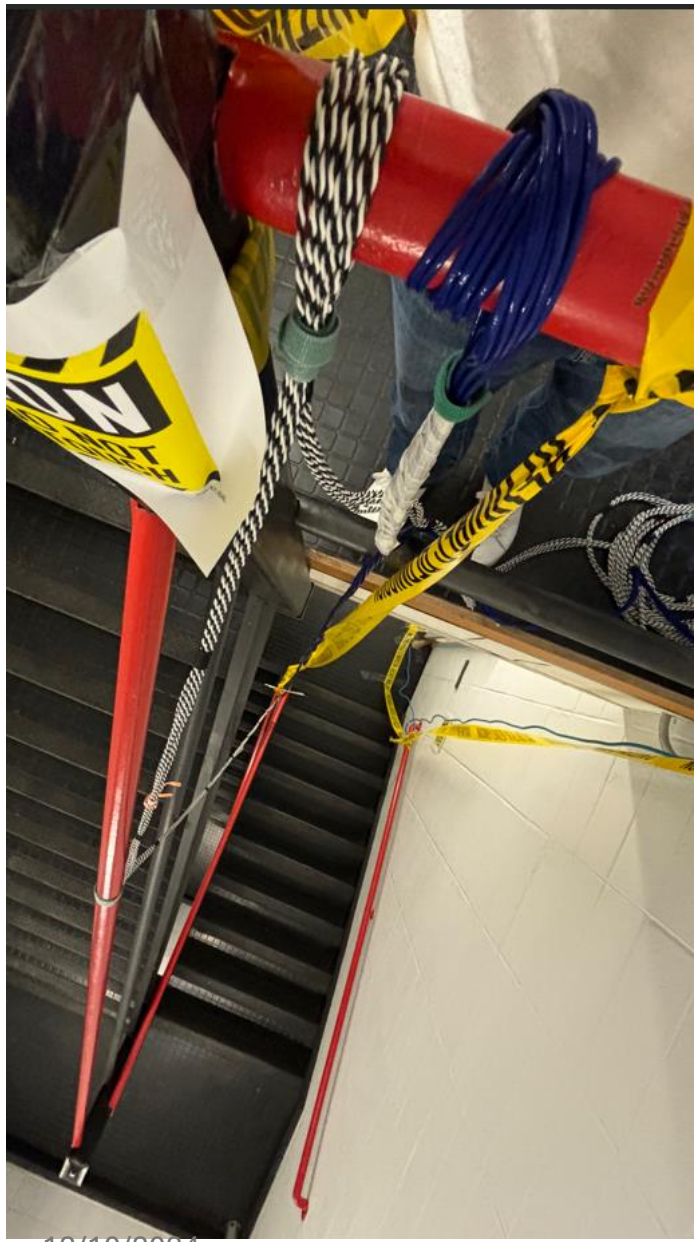
4th floor

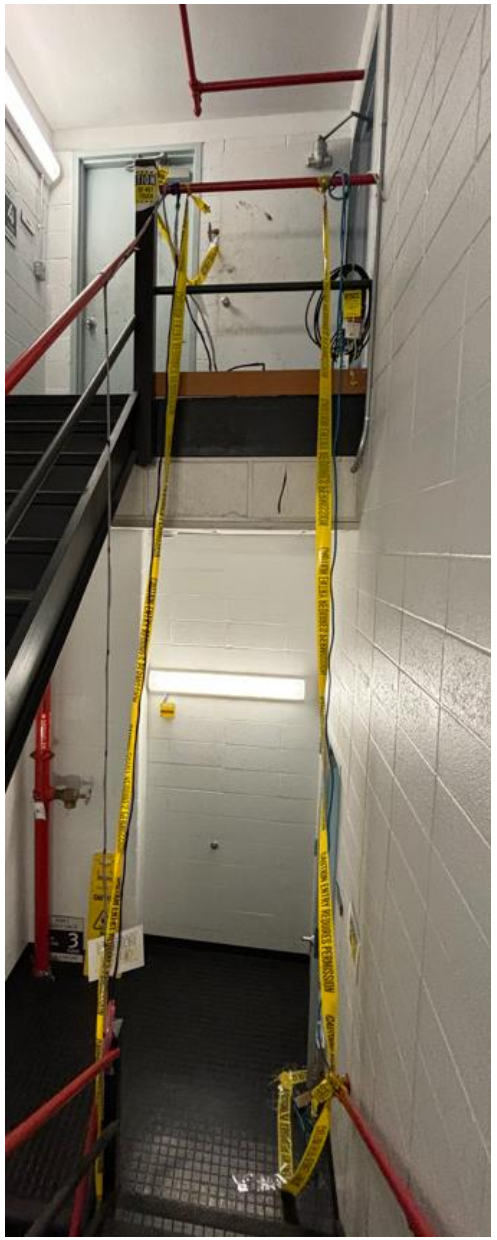
1st floor

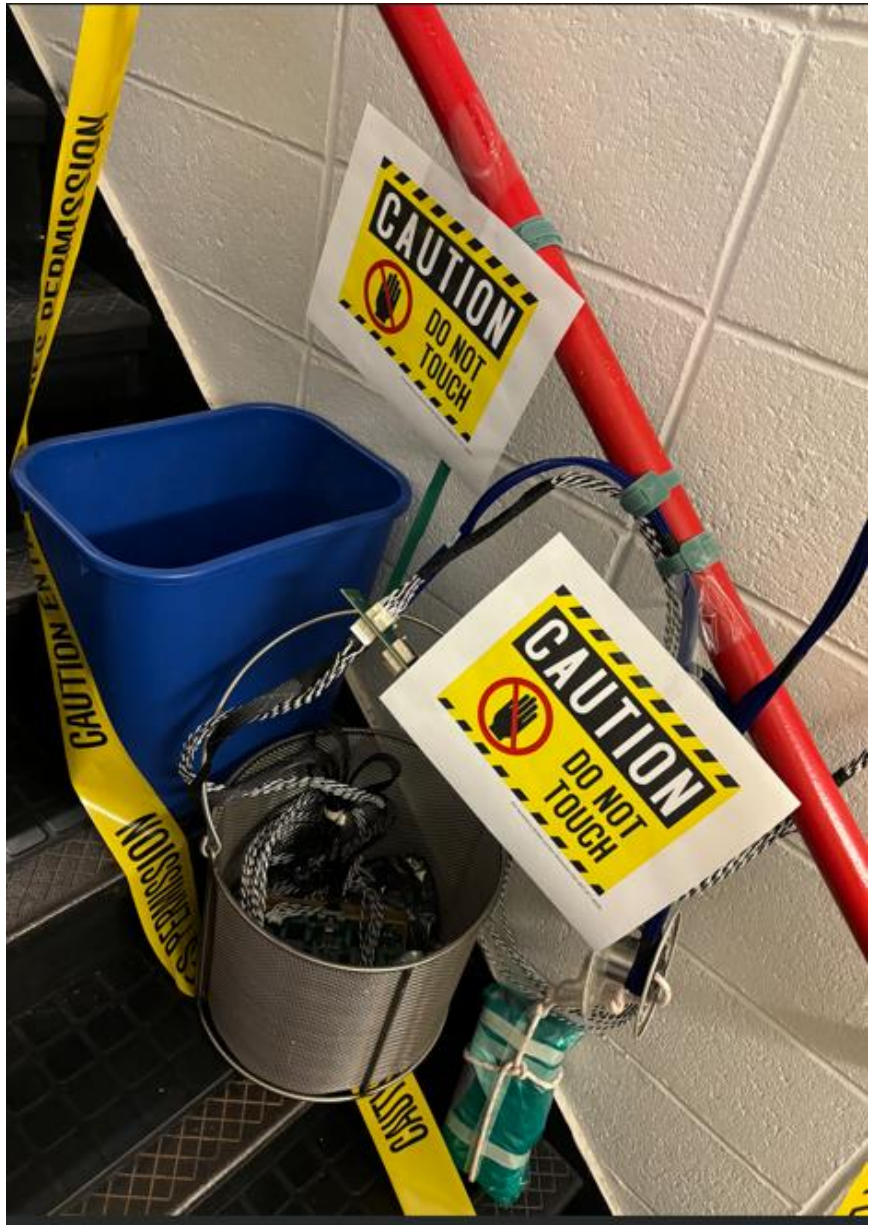
Setup with cables hanging unsupported 12+ meters



Note: both WIB1&WIB2 have a WIB adapter board



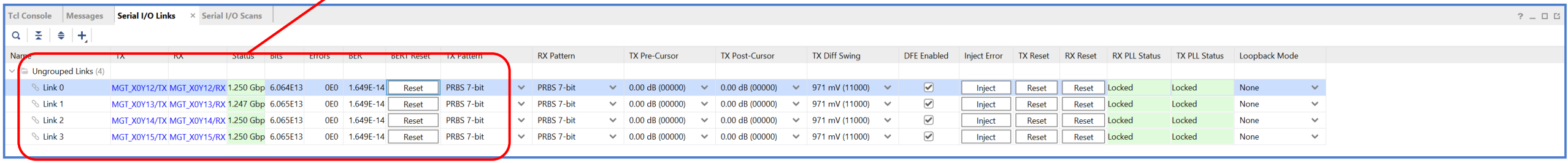



CAUTION
DO NOT TOUCH
CAUTION
DO NOT TOUCH

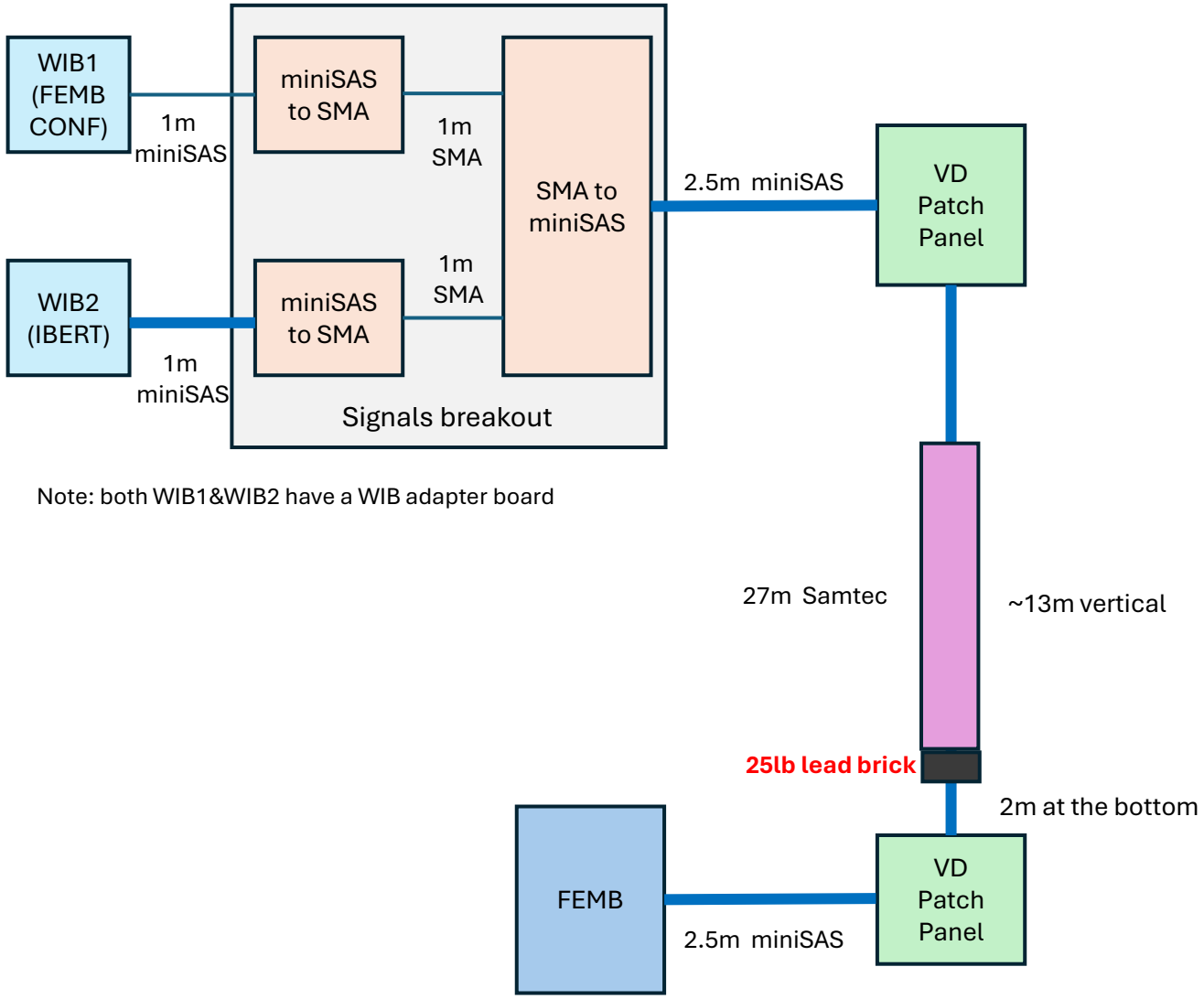
BER result (0 error bit, BER < 1.65E-14)

Tcl Console | Messages | **Serial I/O Links** | Serial I/O Scans

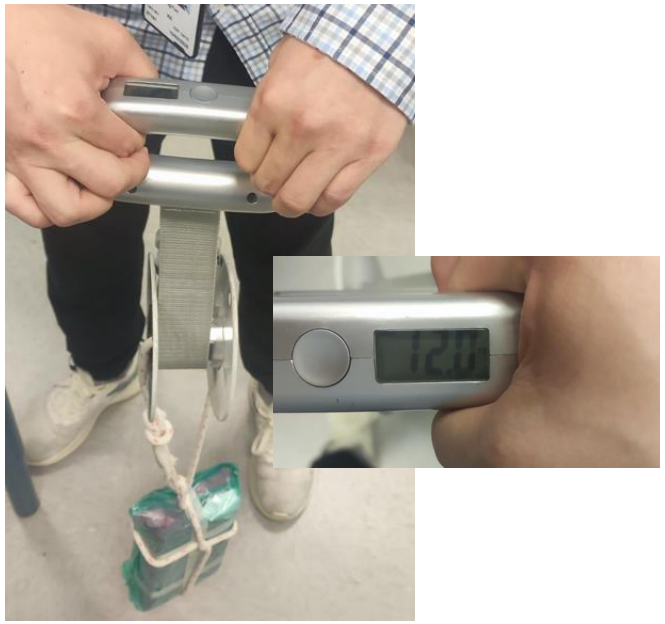
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern
Ungrouped Links (4)								
Link 0	MGT_X0Y12/TX	MGT_X0Y12/RX	1.250 Gbp	6.064E13	0E0	1.649E-14	Reset	PRBS 7-bit
Link 1	MGT_X0Y13/TX	MGT_X0Y13/RX	1.247 Gbp	6.065E13	0E0	1.649E-14	Reset	PRBS 7-bit
Link 2	MGT_X0Y14/TX	MGT_X0Y14/RX	1.250 Gbp	6.065E13	0E0	1.649E-14	Reset	PRBS 7-bit
Link 3	MGT_X0Y15/TX	MGT_X0Y15/RX	1.250 Gbp	6.065E13	0E0	1.649E-14	Reset	PRBS 7-bit



Setup with cables hanging with 12 kg load



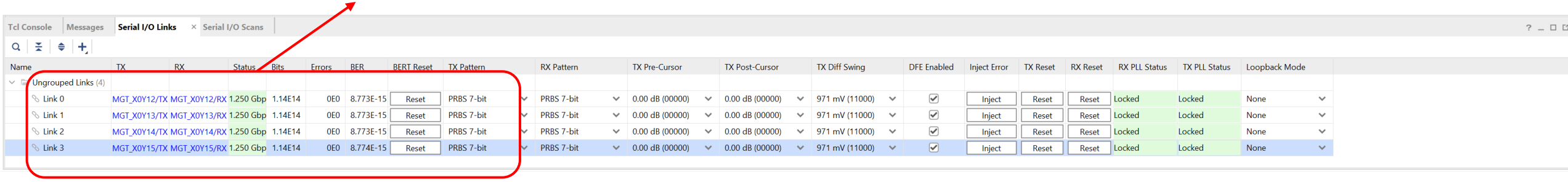
Note: both WIB1&WIB2 have a WIB adapter board



BER result (0 error, BER < 8.8E-15)

Tcl Console | Messages | **Serial I/O Links** | Serial I/O Scans

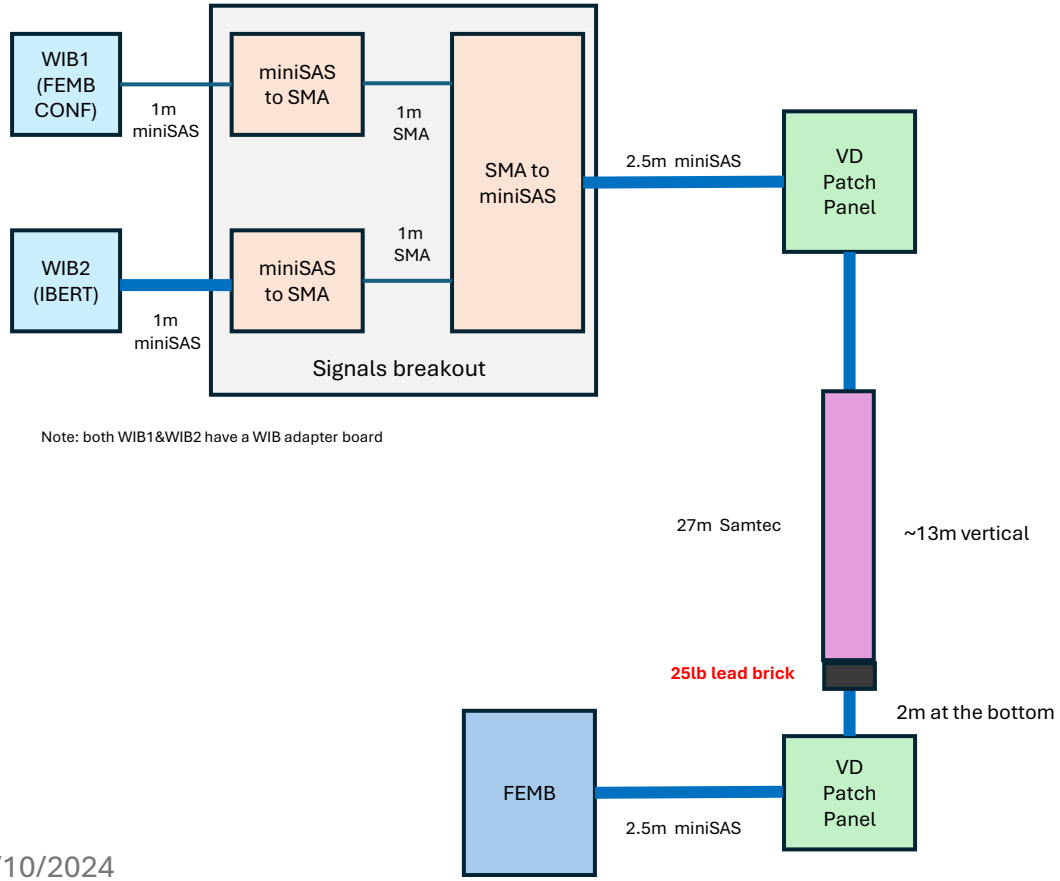
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern
Ungrouped Links (4)								
Link 0	MGT_X0Y12/TX	MGT_X0Y12/RX	1.250 Gbp	1.14E14	0E0	8.773E-15	Reset	PRBS 7-bit
Link 1	MGT_X0Y13/TX	MGT_X0Y13/RX	1.250 Gbp	1.14E14	0E0	8.773E-15	Reset	PRBS 7-bit
Link 2	MGT_X0Y14/TX	MGT_X0Y14/RX	1.250 Gbp	1.14E14	0E0	8.773E-15	Reset	PRBS 7-bit
Link 3	MGT_X0Y15/TX	MGT_X0Y15/RX	1.250 Gbp	1.14E14	0E0	8.774E-15	Reset	PRBS 7-bit



2024/12/07 9:50 AM --- 20241208 10:30AM

Summary

- Hanging data cable 12m in height with extra 12kg load doesn't affect the high-speed data transmission.
  - Keep in mind, the test setup is more stringent than VD configuration
    - Extra 1m miniSAS, 1m SMA, 2.5m miniSAS
    - More interconnections



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