ATLAS Upgrade Programme for LS1 and HL-LHC

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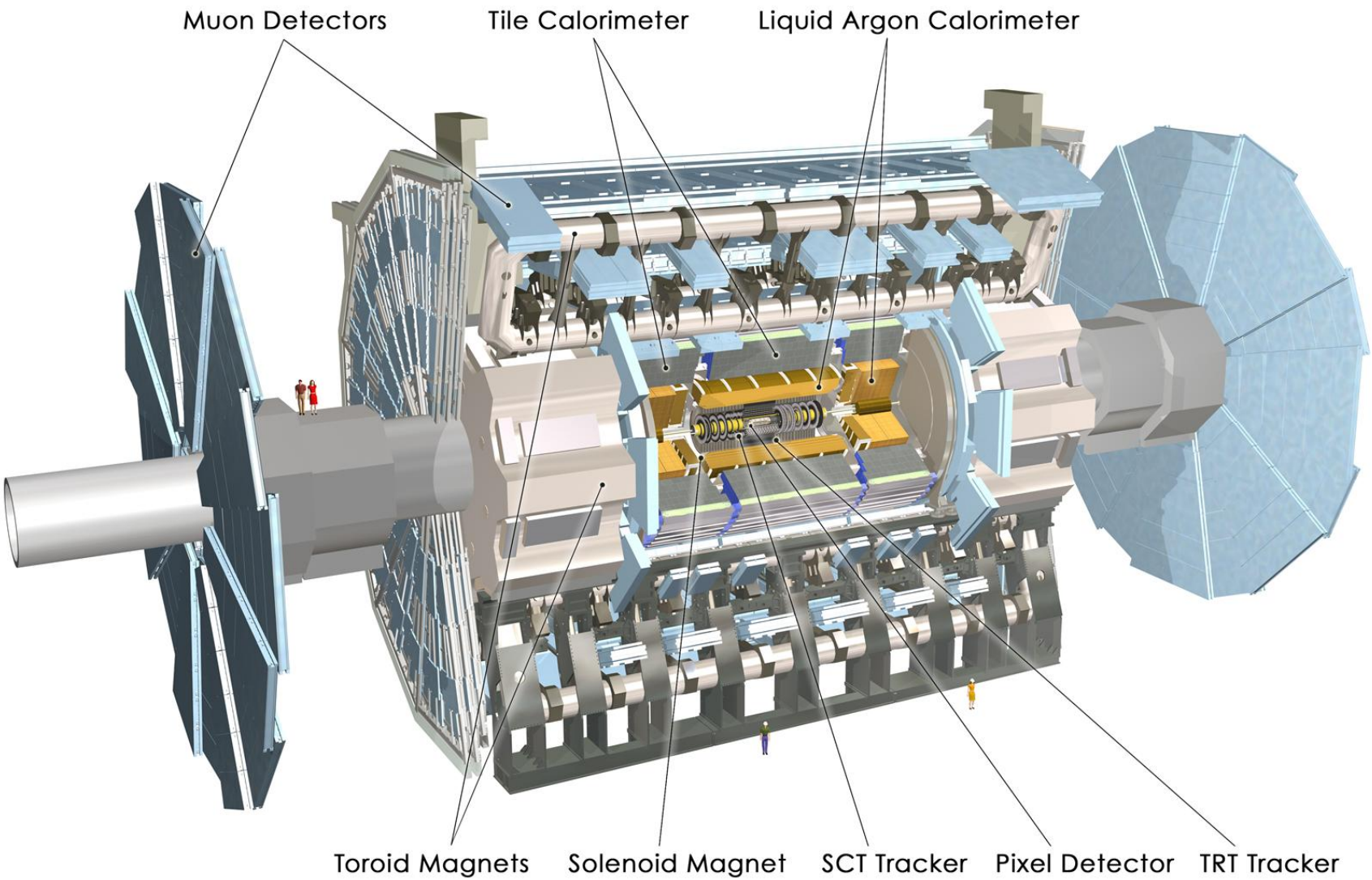
for the ATLAS collaboration

Outline

- ATLAS upgrade overview
- Muon system upgrade
- Calorimeter upgrade
- Tracker upgrade
- TDAQ system upgrade
- Summary

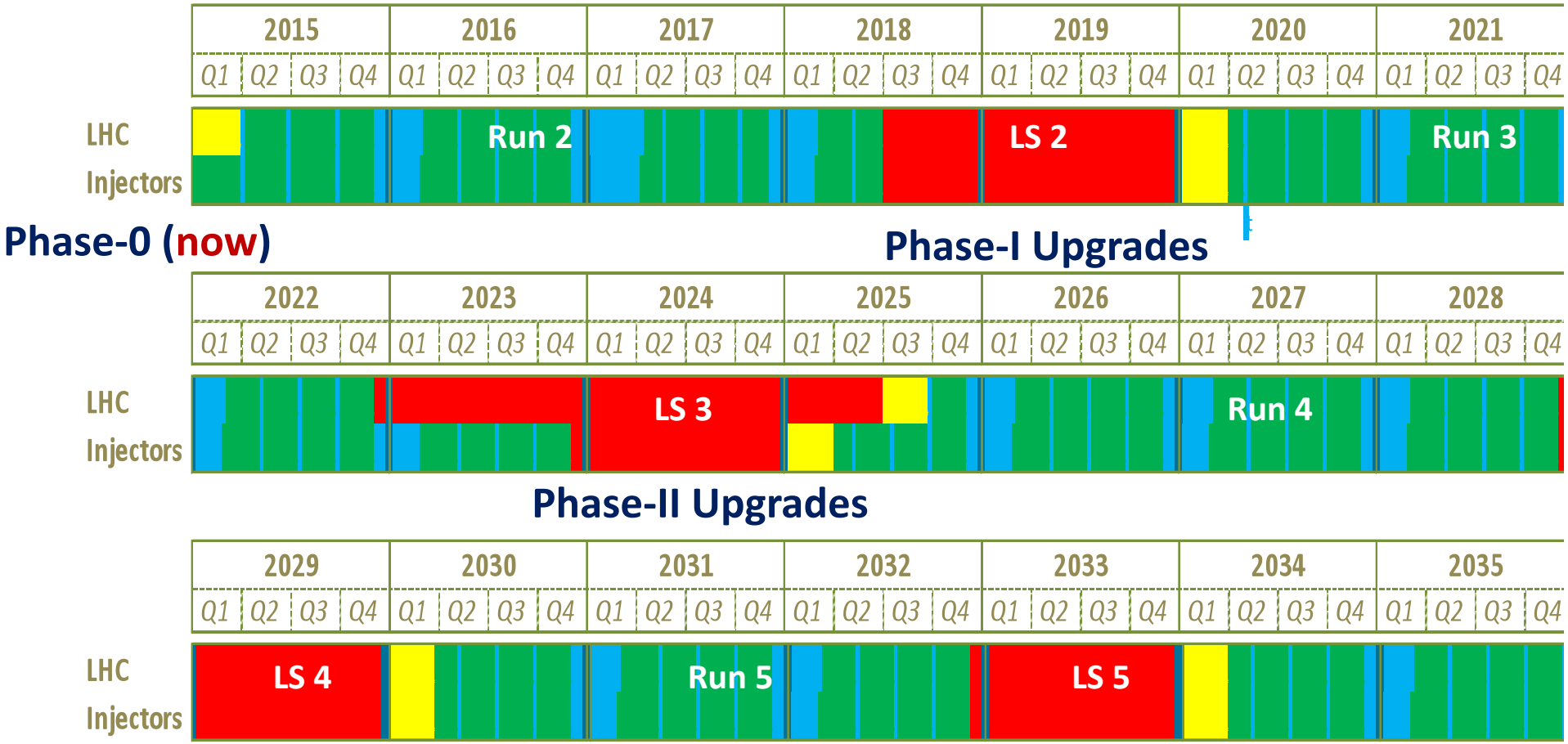
ATLAS Detector



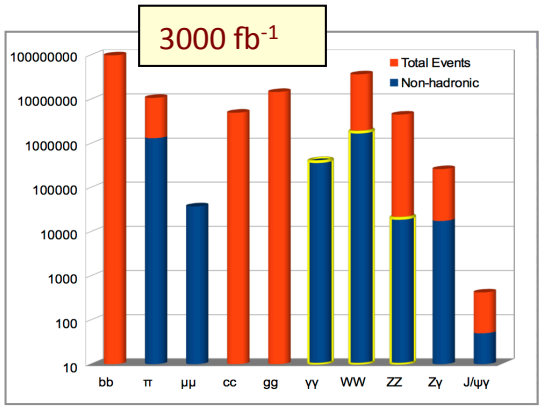
LHC Schedule

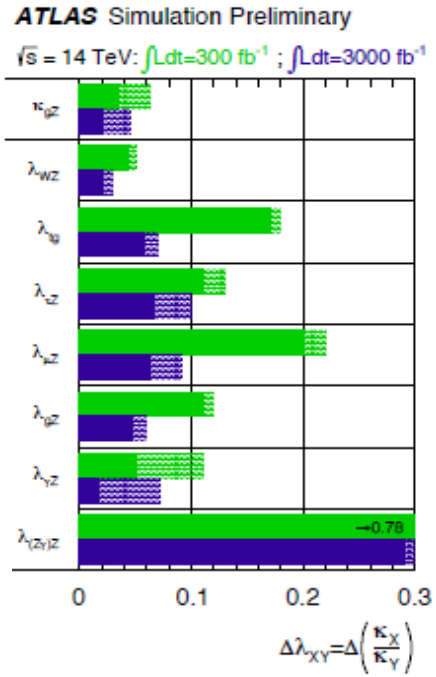
Only EYETS (19 weeks) (no Linac4 connection during Run2)

LS2	**starting in 2018 (July)**	**18 months + 3months BC (Beam Commissioning)**
LS3	**LHC: starting in 2023 =>**	**30 months + 3 BC**
	injectors: in 2024 =>	**13 months + 3 BC**

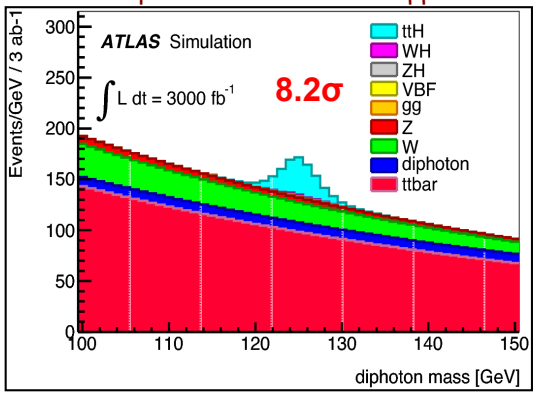


Physics Studies (Samples)

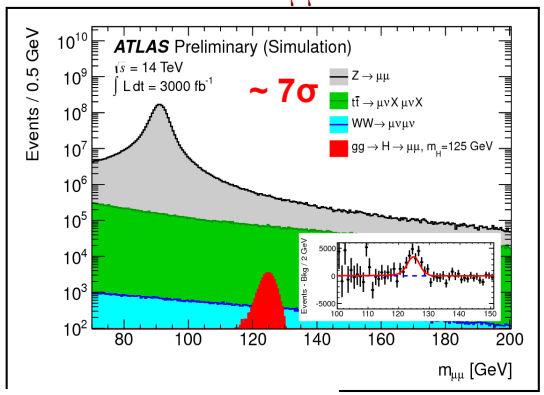


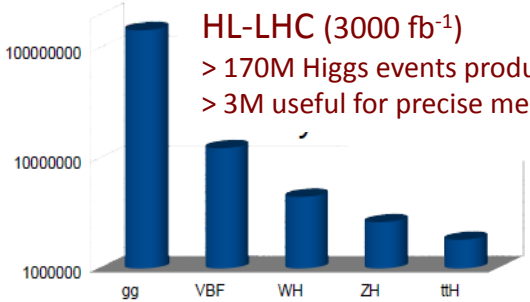


ttH production with H → γγ



H →μμ



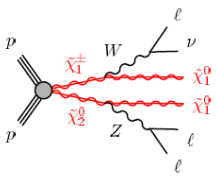


HL-LHC (3000 fb-1)

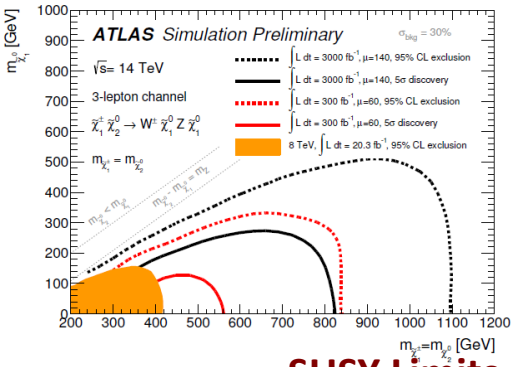
> 170M Higgs events produced

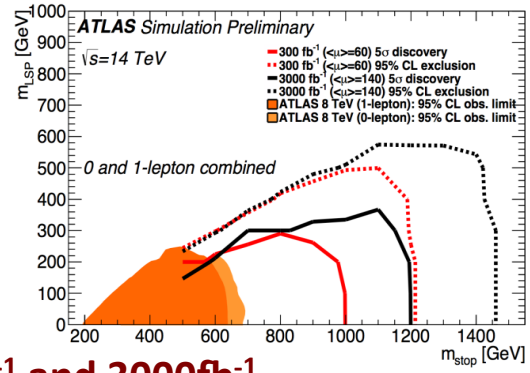
> 3M useful for precise measurements

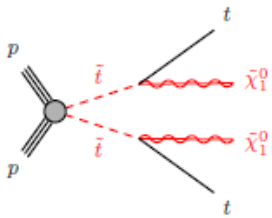
Higgs Coupling



(a) WZ-mediated







SUSY Limits at 300fb-1 and 3000fb-1

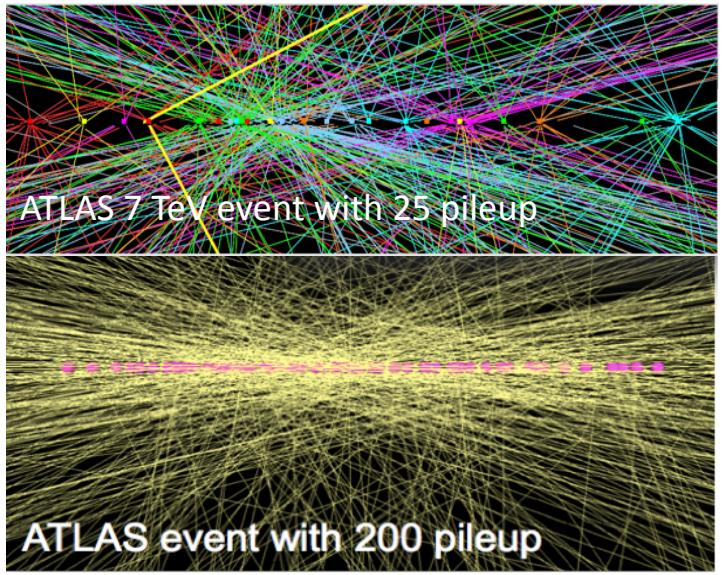
Challenge in Brief

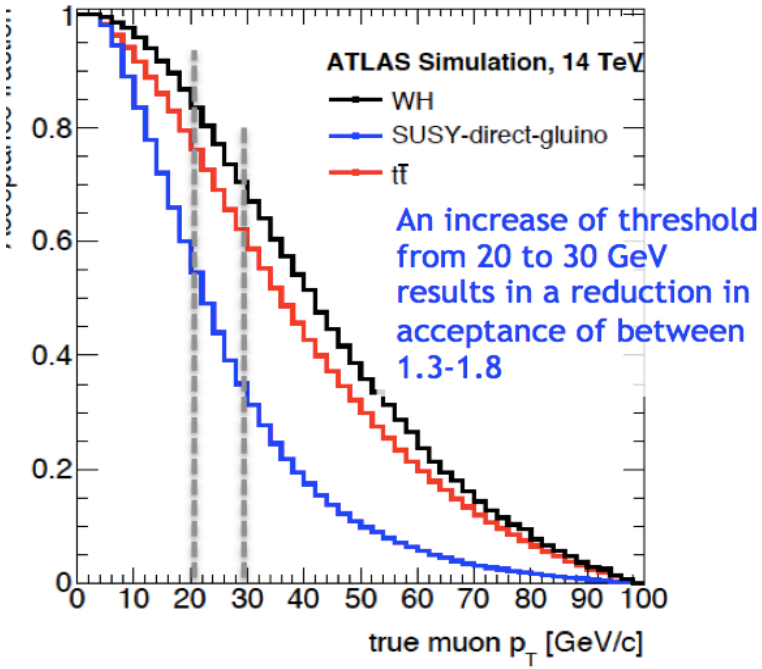
High instantaneous luminosity

- ~200 pileups/bunch crossing
- Higher detector occupancy and larger event size
- Higher trigger rate so critical to refine the triggers to maintain sensitivity to physics
  - Low threshold for single leptons
  - rejection on pileups

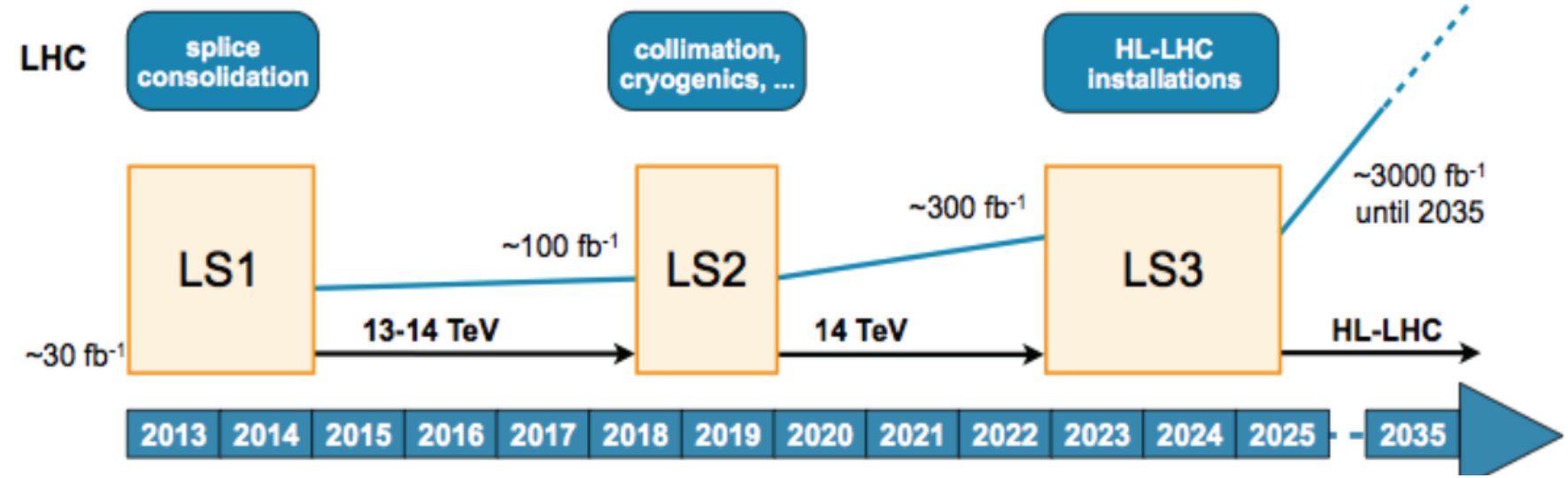
High integrated luminosity

- Higher radiation damage (fluence ~ 10^{16} n_{eq}/cm^2 close to the beam pipe)
- Higher activation of the materials





ATLAS Upgrades



Go to design energy, nominal luminosity
$\mathcal{L} = 1 \times 10^{34}\ cm^{-2}s^{-1}$

Injector and LHC Phase-1 upgrade to ultimate design luminosity
$\mathcal{L} = 2\text{-}3 \times 10^{34}\ cm^{-2}s^{-1}$

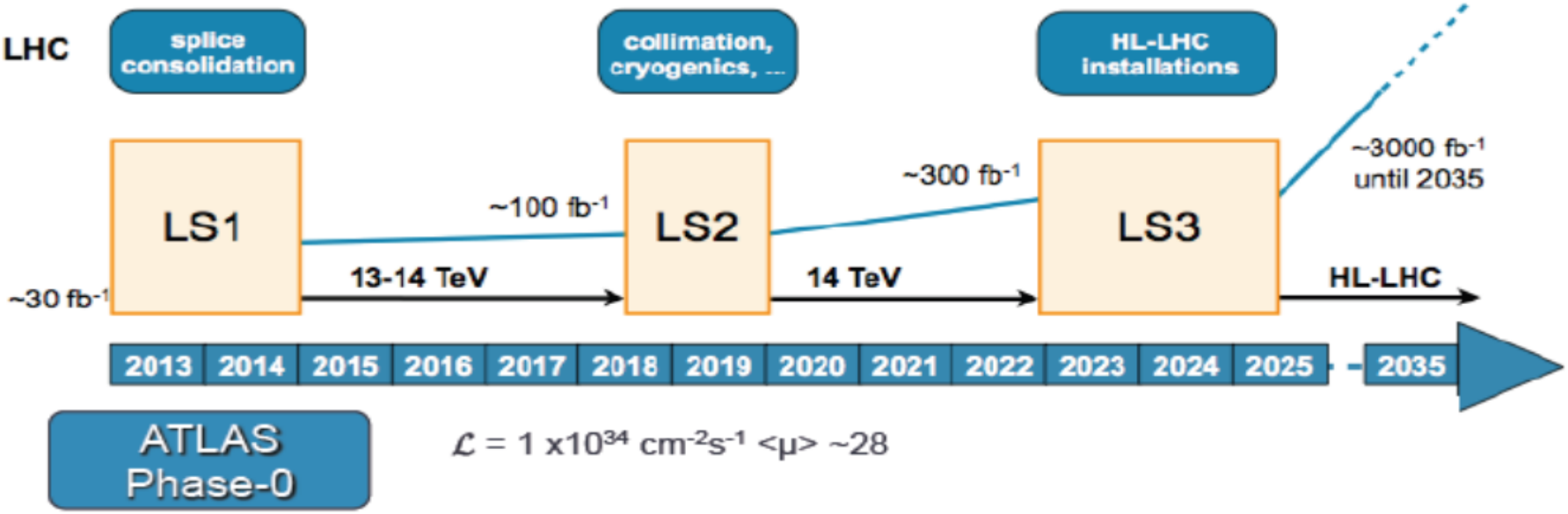
HL-LHC Phase-2 upgrade, IR, luminosity leveling, ...
$\mathcal{L} = 5 \times 10^{34}\ cm^{-2}s^{-1}$

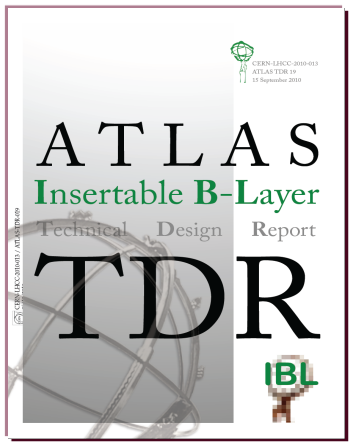
ATLAS Phase-0

ATLAS Phase-1

ATLAS Phase-2

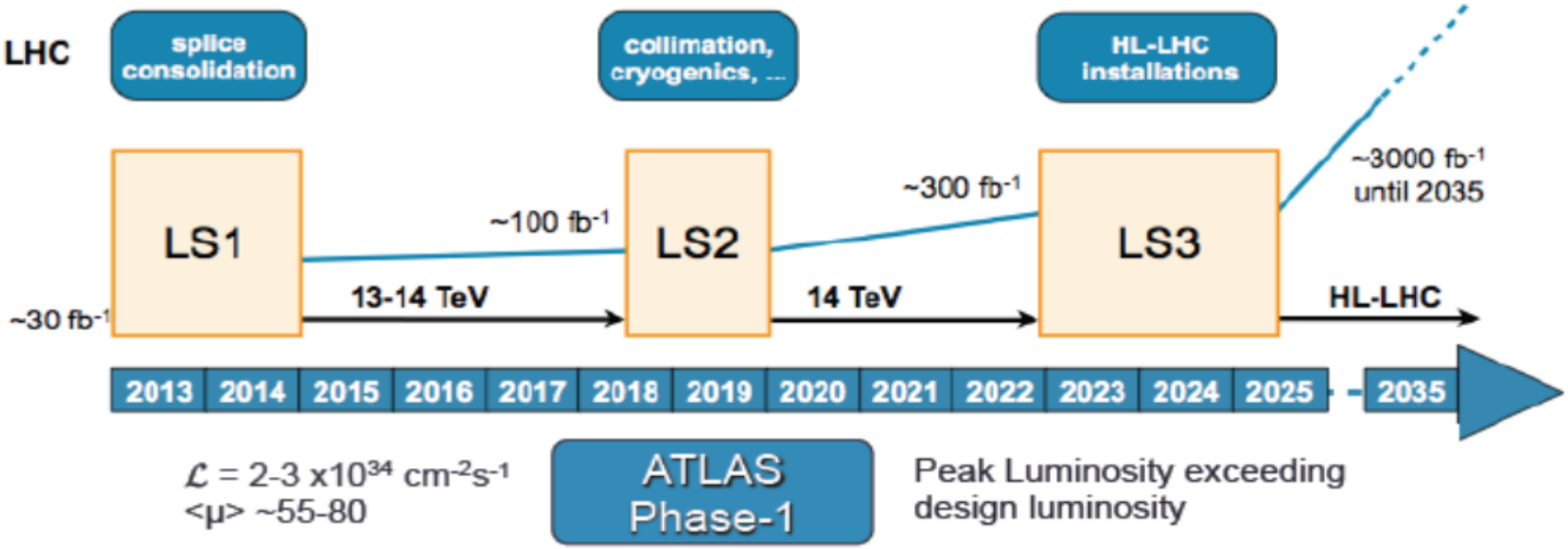
ATLAS Upgrades



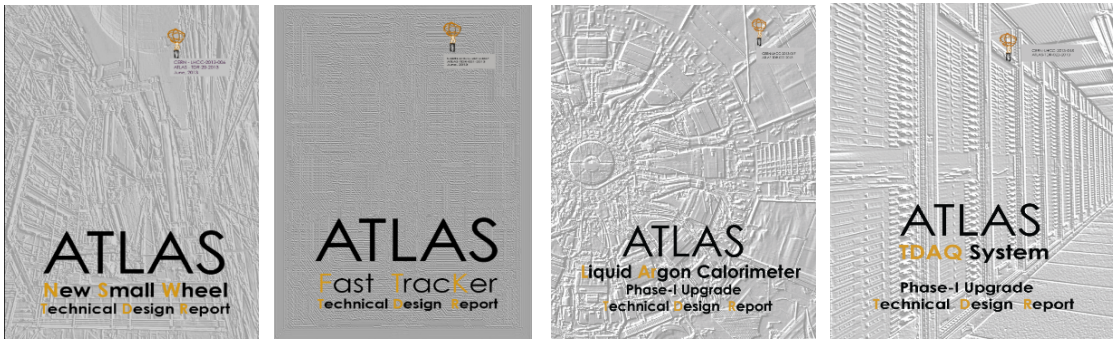


- Insertable B Layer
- Improvement on muon spectrometer coverage
- Consolidation of some parts of the detector
- Infrastructures and services
- Preparation work for Phase-I
- TDAQ system improvement
- … …

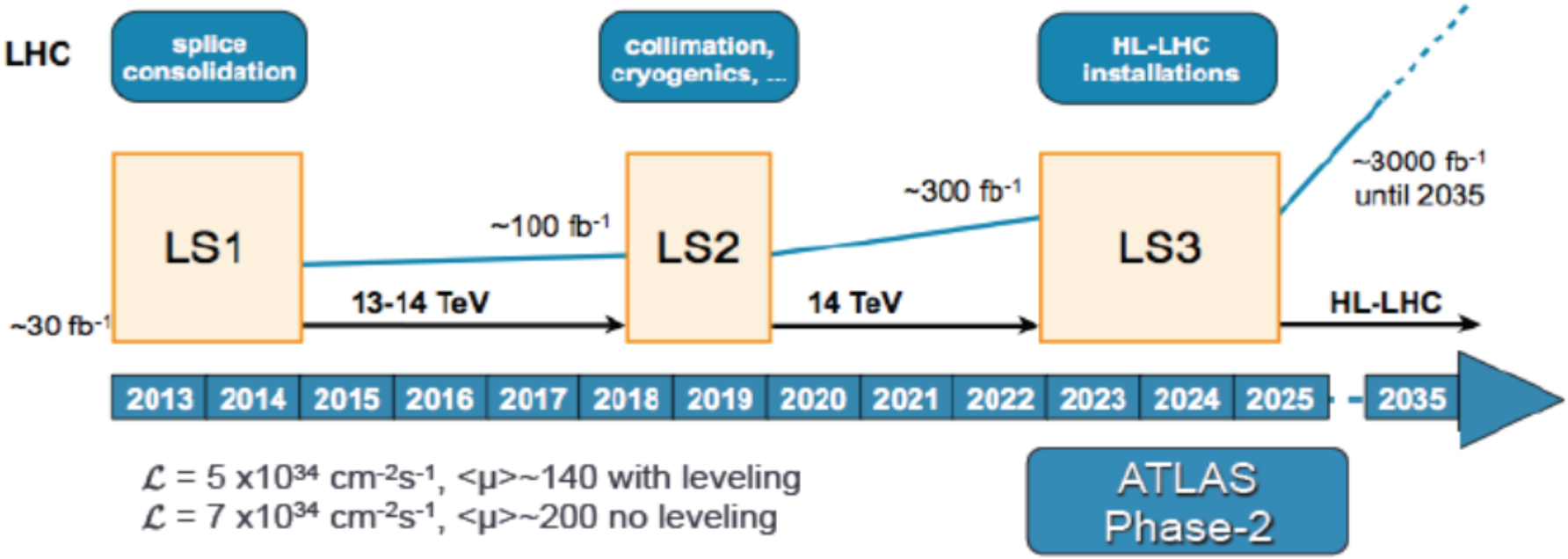
ATLAS Upgrades



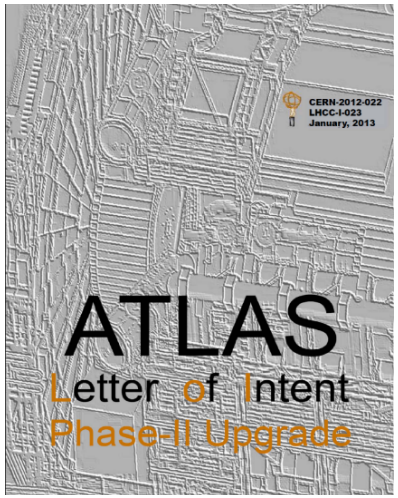
- New Small Wheels to improve muon trigger
- Liquid Argon Calorimeter (LAr) trigger path electronics
- TDAQ with higher granularity Level-1 calorimeter trigger, new readout, etc
- Fast TracKer
- ATLAS Forward Physics detectors



ATLAS Upgrades



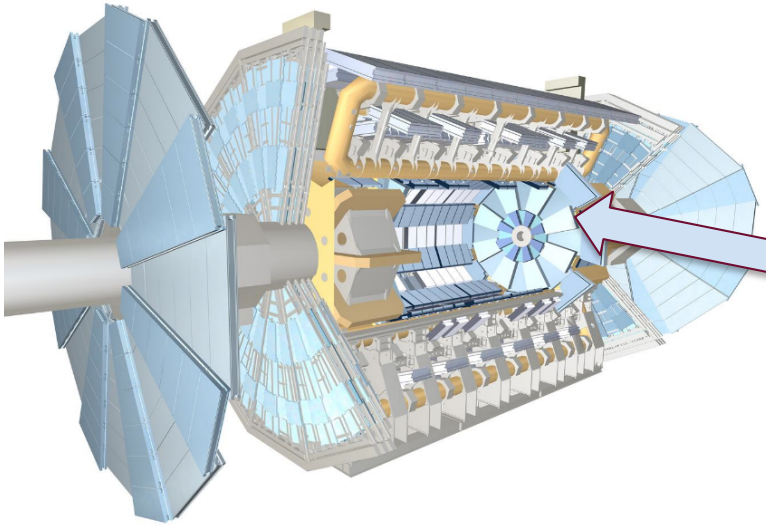
- New all silicon Inner Tracker
- New TDAQ system with Level-1 track trigger
- New electronics for LAr and Tile calorimeter
- Upgrade to muon system electronics and possibly some new chambers
- Major evolution of software and computing
- … …



Muon System Upgrade

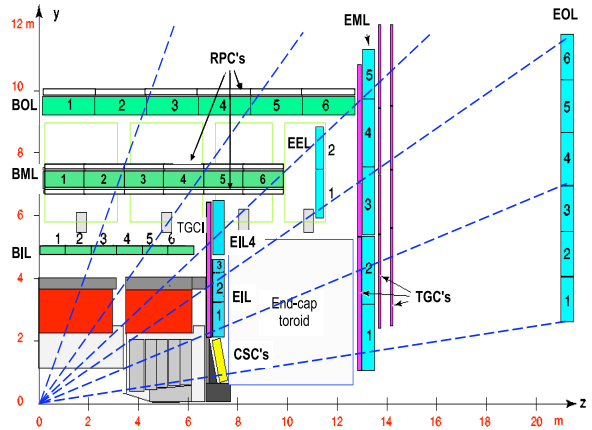
- Phase-I: New Small Wheel (NSW)

NSW



The innermost station of the muon endcap

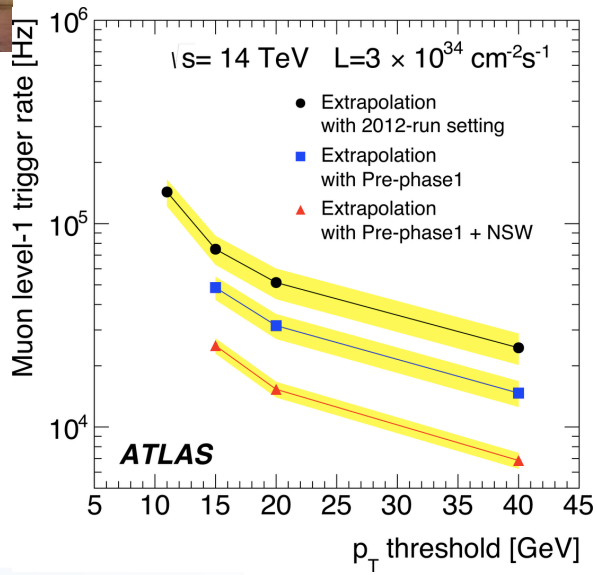
Located between endcap calorimeter and endcap toroid



- In forward direction the efficiency of muon chambers deteriorates as the luminosity goes beyond the design value
- Level-1 muon trigger rate exceeds the available bandwidth unless thresholds raised

Replace small wheels

- To reject fake muon triggers by requiring high quality pointing to interaction region
- To combinine sTGC and micromegas technologies for robustness to Phase-II luminosities



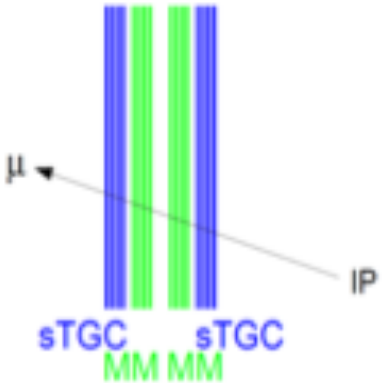
NSW

Micromegas as primary precision tracker

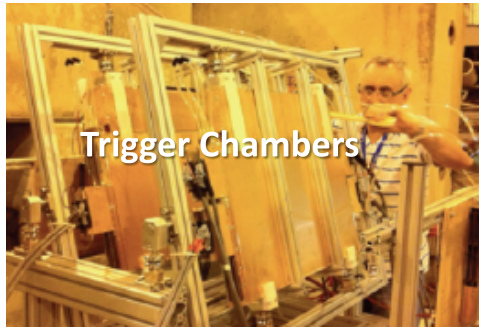
- Space resolution < 100 µm independent of track incidence angle
- Good track separation due to small readout granularity
- High rate capability due to small gas amplification region and small space charge effect

sTGCs as primary trigger detector

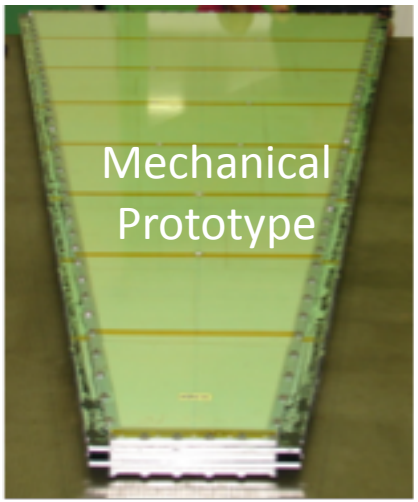
- Bunch ID with good timing resolution to suppress fakes
- Track vectors with < 1 mrad angular resolution
- Based on proven TGC technology



2.4m×1m Micromegas Prototype
(New Small Wheel: 1280m^2)



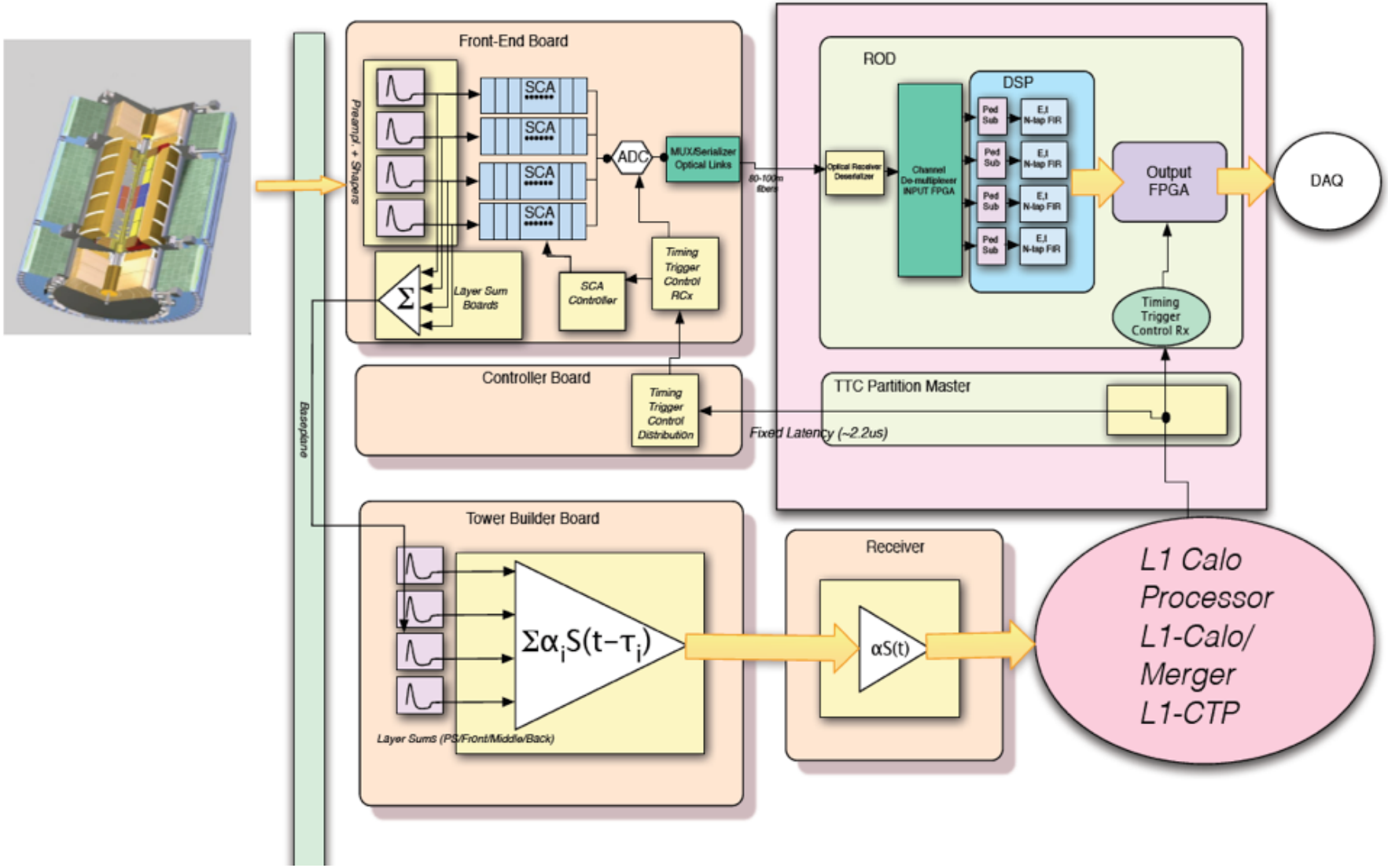
sTGC Prototype



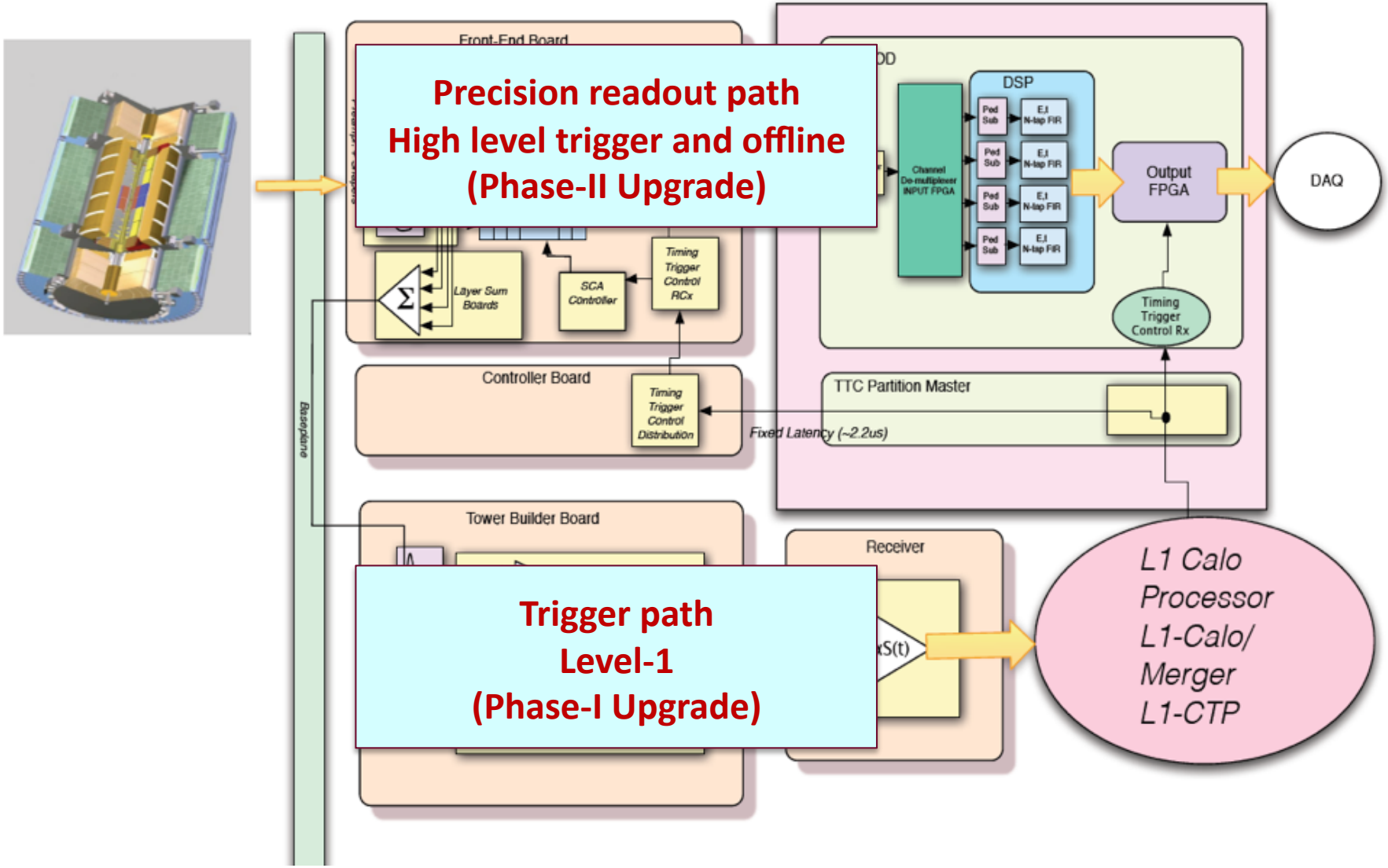
Calorimeter Upgrade

- Phase-I: LAr trigger path electronics
- Phase-II: Tile electronics

LAr Readout Electronics

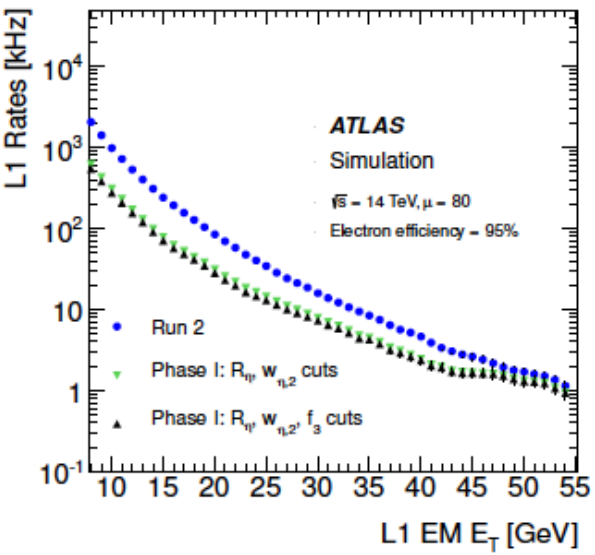


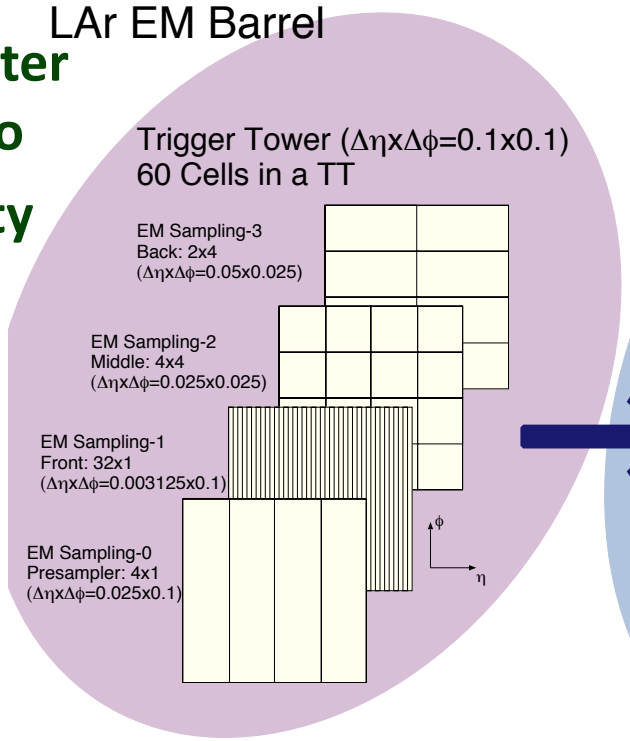
LAr Readout Electronics Upgrade

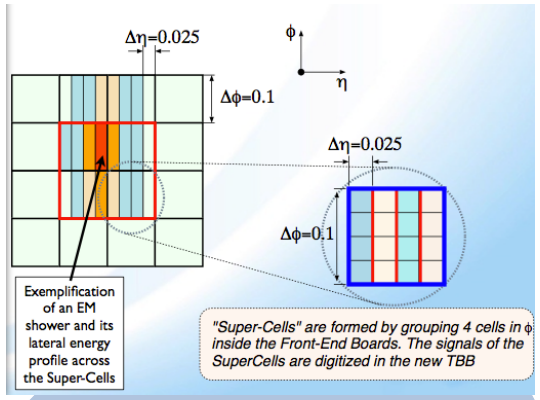


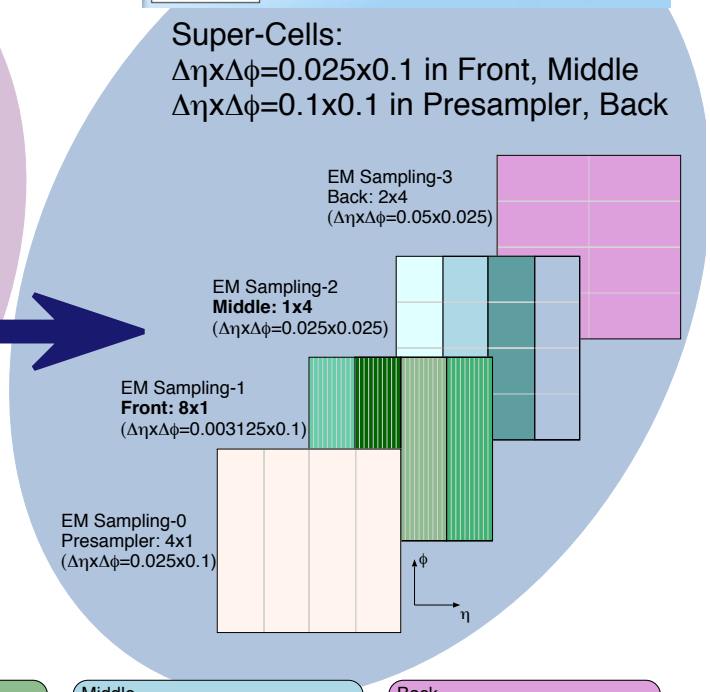
LAr Readout Phase-I Upgrade

- To maintain high efficiency for Level-1 triggering on low P_T electrons and photons
- To change LAr calorimeter front-end electronics to provide finer granularity for Level-1



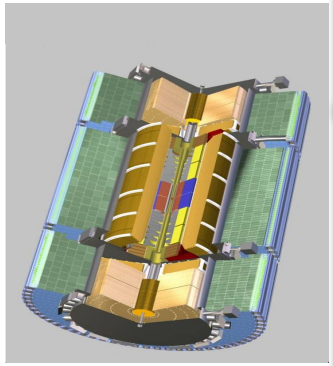






Presampler	Front	Middle	Back
SC_layer=0	SC_layer=1	SC_layer=2	SC_layer=3
SC_region=0	**SC_region=0**	**SC_region=0**	**SC_region=0**
SC_eta=0...13 [Δη=0.1]	SC_eta=0...55 [Δη=0.025]	SC_eta=0...55 [Δη=0.025]	SC_eta=0...12 [Δη=0.1]
SC_region=1	**SC_region=1**	**SC_region=1**	SC_eta=13 [Δη~0.05]
SC_eta=14(15) [Δη~0.1(0.12)]	SC_eta=56..58 [Δη=0.025]	SC_eta=56 [Δη=0.075]	SC_phi=0...63 [Δϕ=0.1]
SC_phi=0...63 [Δϕ=0.1]	SC_phi=0...63 [Δϕ=0.1]	SC_phi=0...63 [Δϕ=0.1]	

LAr Readout Phase-I Upgrade



New or modified Components (in red)

Possible implementation
ΔηxΔφ=0.025x0.1 1st and 2nd layer EM
ΔηxΔφ=0.1x0.1 elsewhere

Baseplane

Front-End Board
Preampl.
Shaper
Linear Mixer
SCA
ADC
MUX/Serializer Optical Links
New Layer Sum Boards [LSB]
SCA Controller
Timing Trigger Control RCx
80-100m fibers

ROD
Optical Receiver Deserializer
Channel De-multiplexer INPUT FPGA
DSP
Ped Sub
E,t N-tap FIR
Output FPGA
Timing Trigger Control Rx
DAQ

Controller Board
Timing Trigger Control Distribution
TTC Partition Master
Fixed Latency (~3.0us max)

Tower Builder Board [TBB]
PZ+Dly
Trigger Tower Sum and Drivers
$\Sigma\alpha_i S(t-\tau_i)$

Receiver
$\alpha S(t)$

Current L1Calo Processors
Level-1 Calorimeter Trigger System

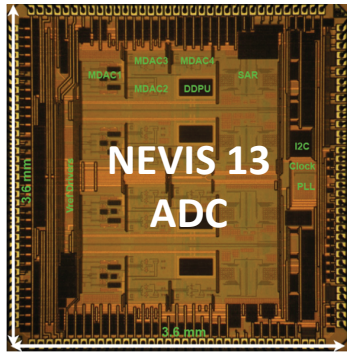
LAr Trigger Digitizer Board (LTDB)
ADC
CLK Fanout
ORx
MUX/Serializer (FPGA)
Optical Links
~250 Gbps/board
Crate Monitoring

Digital Processing System (DPS)
OTx CLK & Cfg.
Optical Receiver Deserializer
FPGA
Ped Sub
E,t N-tap FIR
Timing Trigger Control Rx
SDRAM
480Gbps/module
1.92 Tbps/board

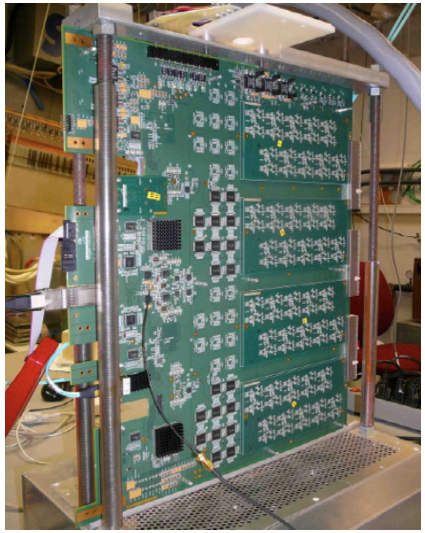
Feature Extractor [FEX]

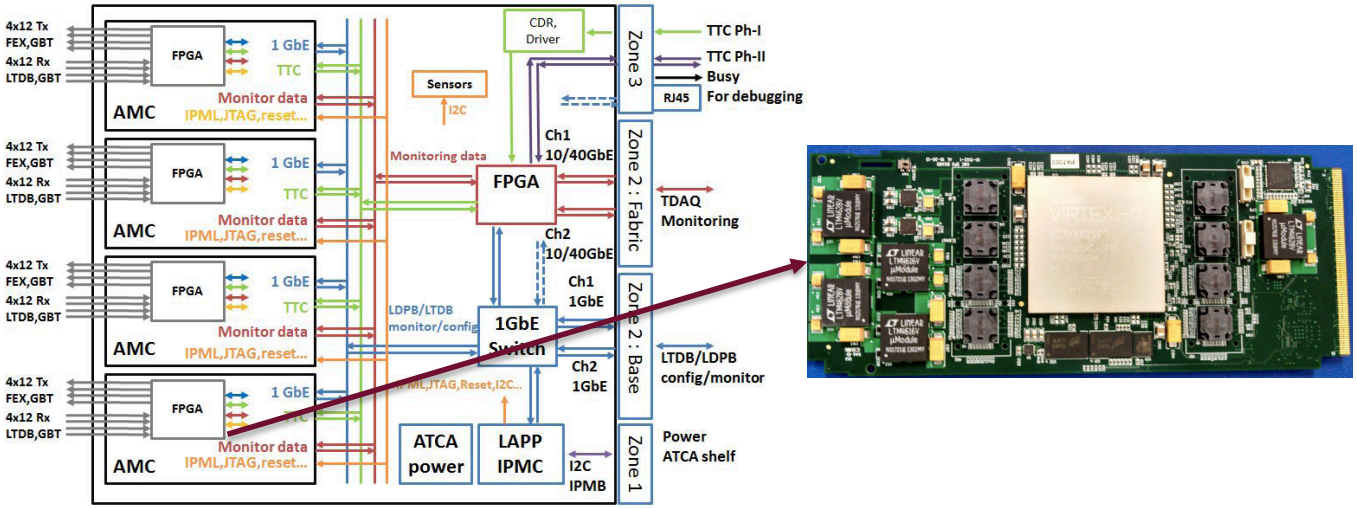
LAr Readout Phase-I Upgrade

- **LAr Trigger Digitizer Board (LTDB)**
  - 320 channels per board
  - Digitization with 12-bit precision @ 40MHz
  - 200 Gbs output per board
  - ADC requirements similar to for Phase-II FEB
- **LAr Digital Processing System (LDPS)**
  - ~800 Gbs input and output per board
  - With features of Phase-II Pre-Processor



LTDB demonstrator



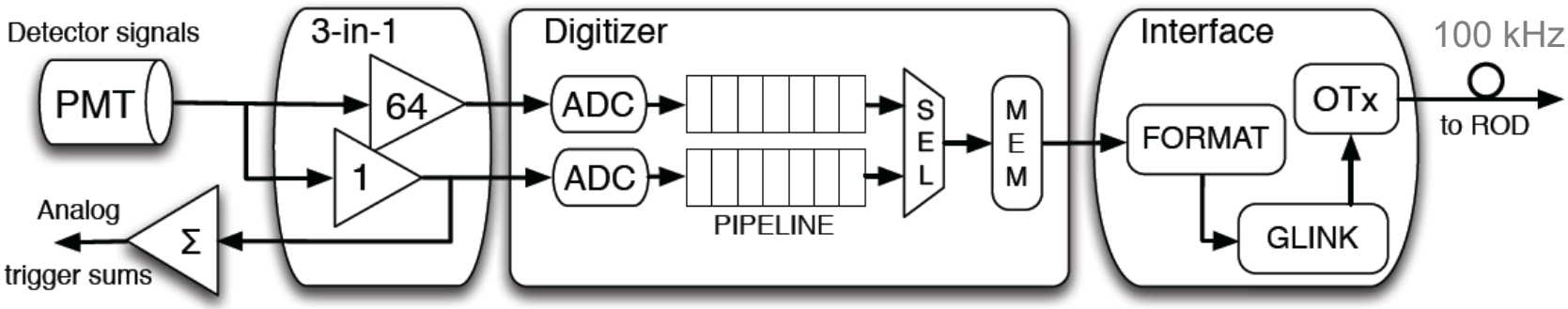


LDPS

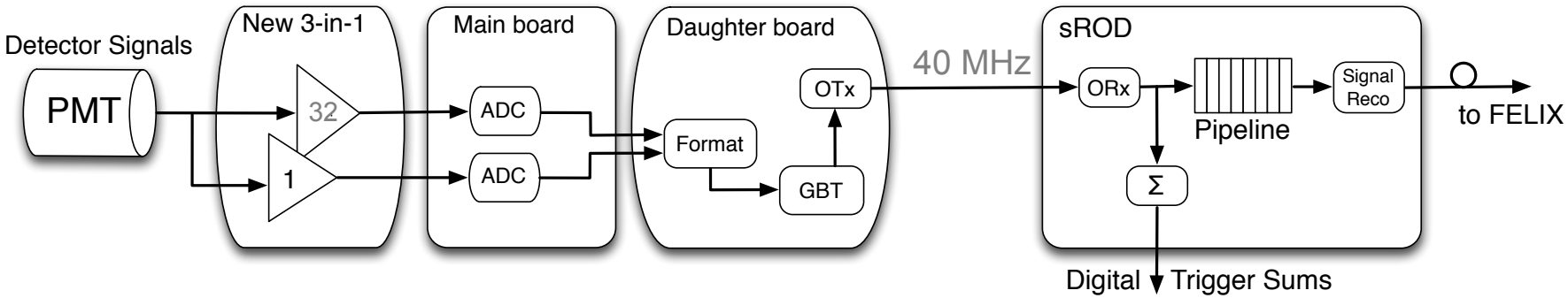
Tile Readout Electronics Upgrade

- Complete FE&BE electronics replacement in Phase-II
- New read-out architecture
  - Full digitization at 40MHz and transmission to off-detector system
  - Digital information to L0/L1 trigger

Present

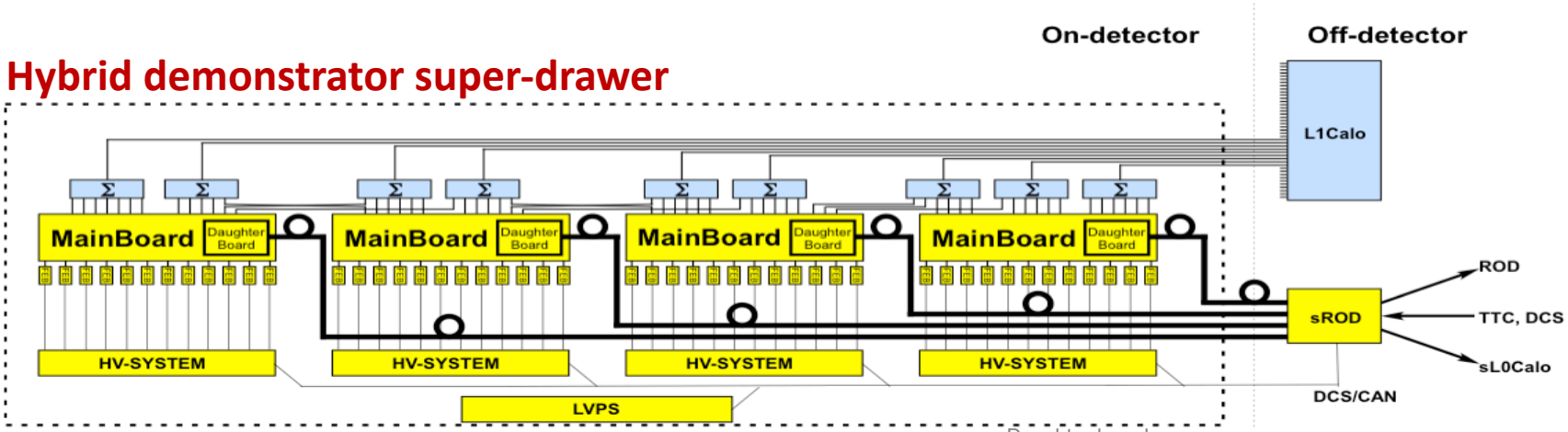


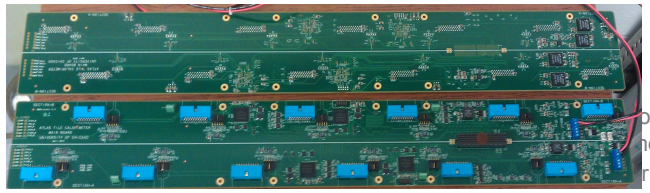
Phase-II Upgrade

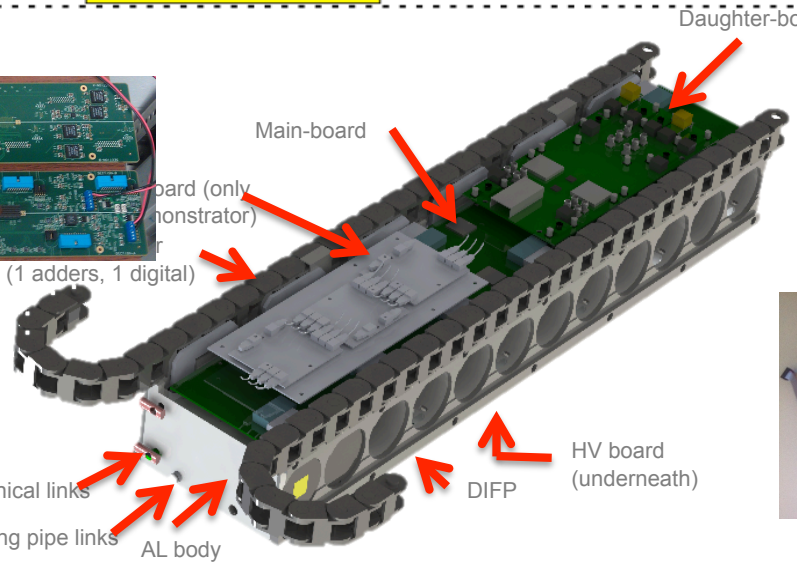


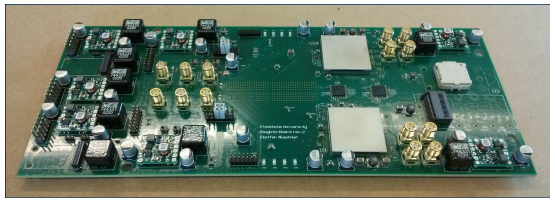
Tile Readout Demonstrator

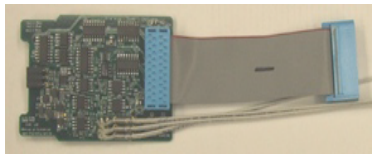
Hybrid demonstrator super-drawer

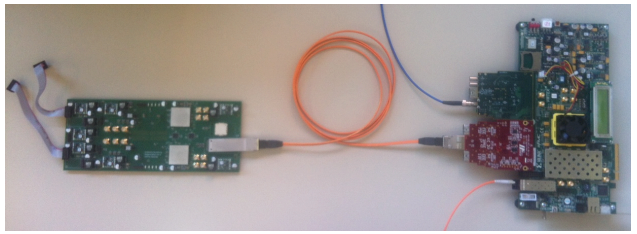


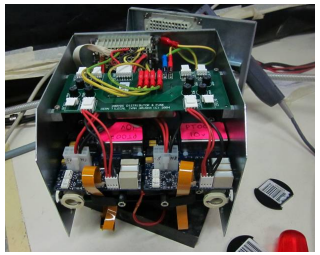


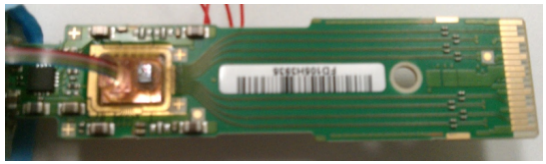


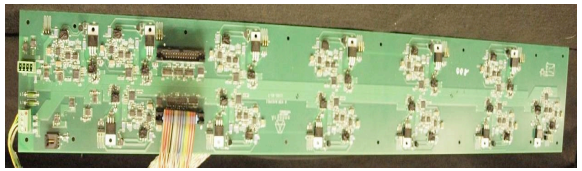










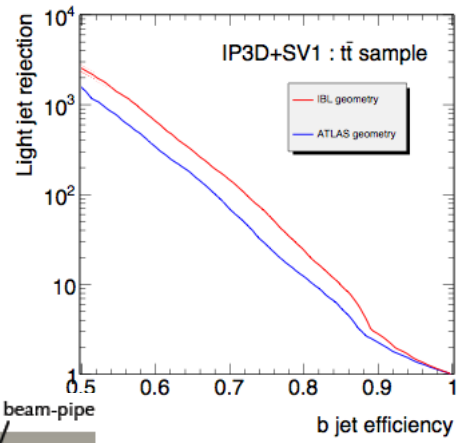


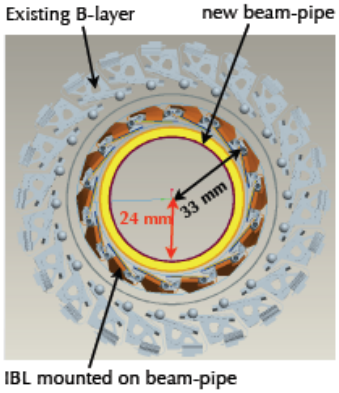
Tracker Upgrade

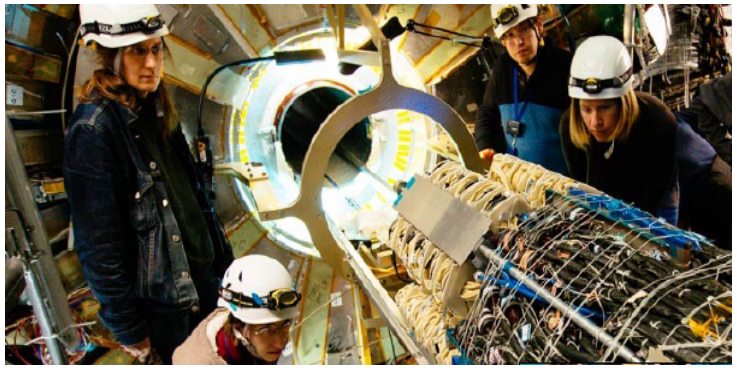
- Phase-0: Insertable B Layer (IBL)
- Phase-II: New all-silicon Inner Tracker (ITk)

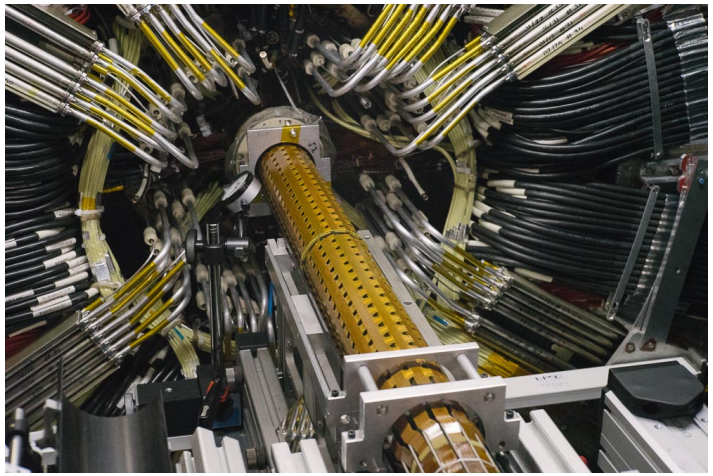
IBL

- New pixel layer around new smaller beam pipe
- Current pixel package brought to surface for
  - IBL support tube insertion at surface
  - New services installed to fix problems and improve R/O bandwidth (nSQP)
  - New diamond beam monitors with IBL (FE-I4) ASICs
- Pixel detector reinserted and reconnected
- IBL inserted into ATLAS in May
  - Services being connected and tested
  - Preparing for operation and commissioning



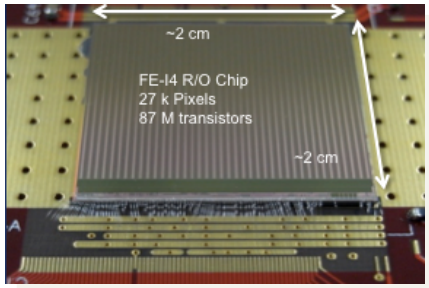


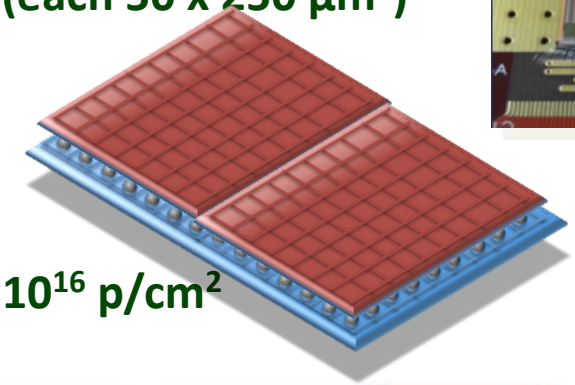


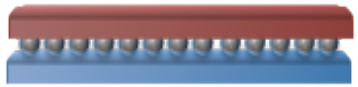


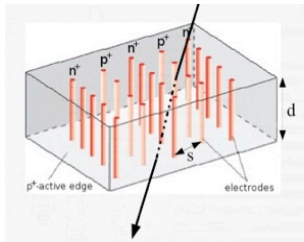
IBL

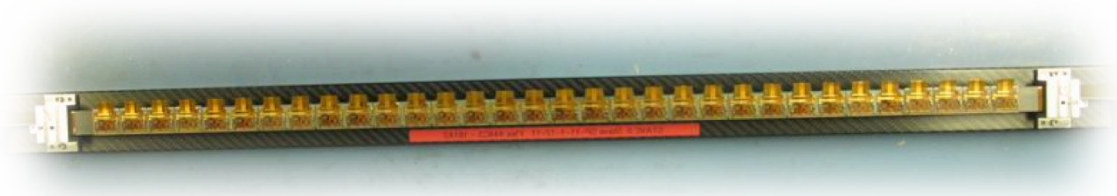
- 14 staves at <r>=3.3.cm,|η|<3.0
- 1.9% X/X_0 radiation length including the new beam pipe
- 32 FE-14 FE chips per stave (4x1-chip 3D + 12x2 chip Planar + 4x1-chip 3D)
- FE-I4 chip
  - 19 x 20 mm^2 130 nm CMOS process
  - based on an array of 80 by 336 pixels (each 50 x 250 μm^2)
- Planar sensor
  - oxygenated n-in-n
  - 200µm thickness
  - Minimization of inactive edge
  - Radiation hardness proven up to 2.4×10^{16} p/cm^2
- 2 types of 3D sensors

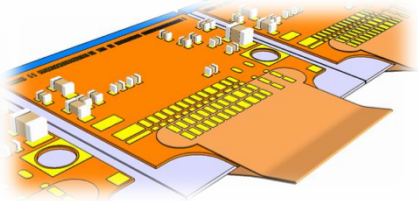


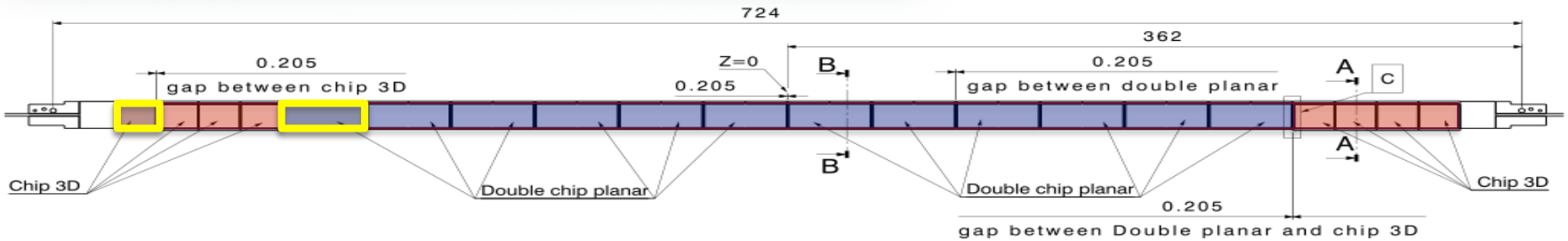




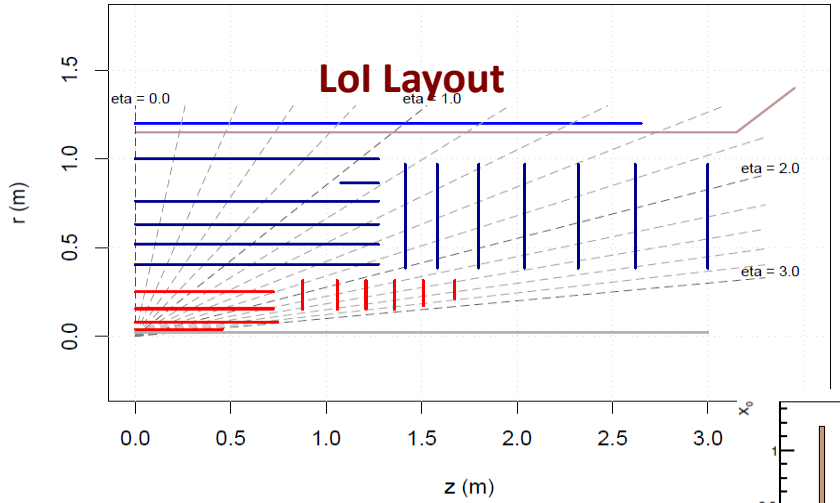




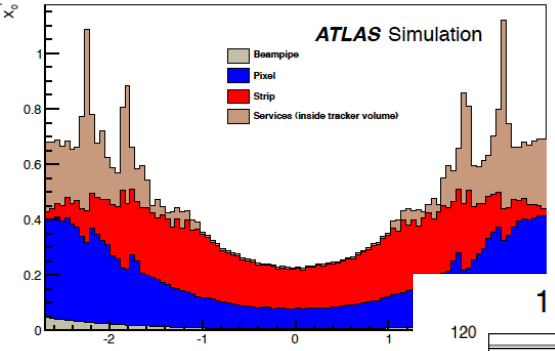




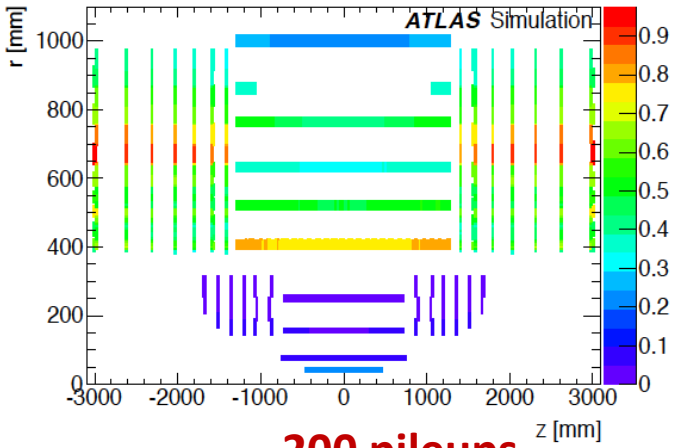
ITk



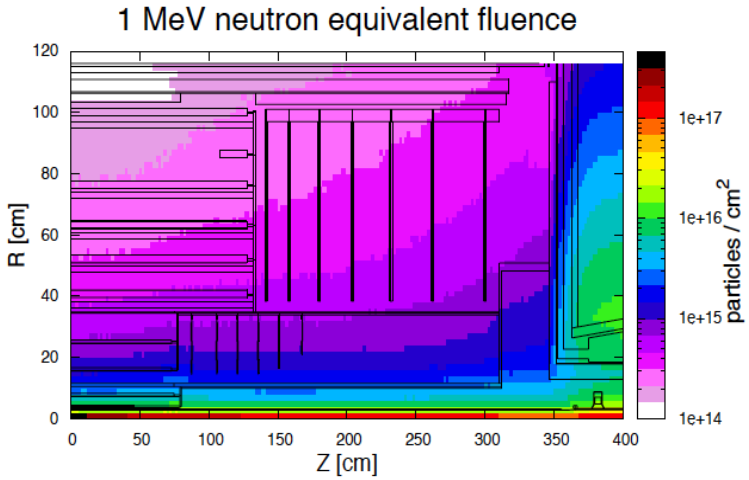
- 4/6 pixel layers/disks
- 5/7 strip layers/disks + stub cylinders
- 50x250 μm² pixels (25x150 for inner layers)
- 24/48 mm strips for barrel inner/outer layers and various different lengths in disks



	Silicon Area	Channels [10⁶]
Pixel	8.2m²	638
Strip	193m²	74



200 pileups

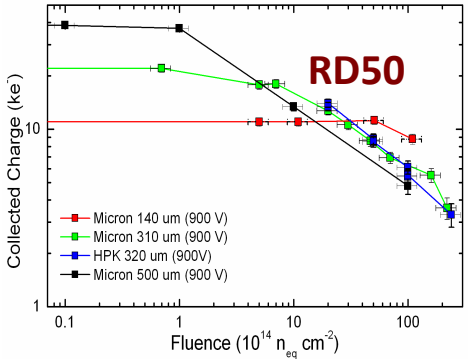


3000 fb^{-1} @ 14 TeV

ITk Pixel Detector

- Planar (n-in-n, n-in-p), 3D and diamond sensors proved to doses up to $2\times10^{16} n_{eq}/cm^2$ and 1Grad

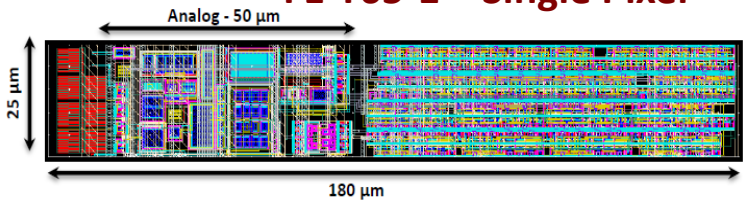
- TSMC 65nm technology allowing pixel sizes down to 50µm×50µm or 25µm×100µm (RD53)
- Test structures in 65nm produced and studied after irradiation

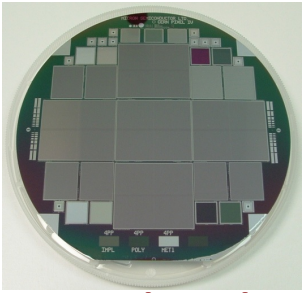


- Larger area sensor quads/sextuplets produced with several foundries
- Irradiated quad pixel modules studied in test-beam with excellent performance

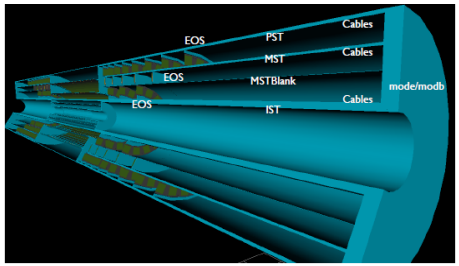
- Prototyping of local supports for various concepts carried out
- Different support designs and service routings studied

FE-T65-1 – Single Pixel

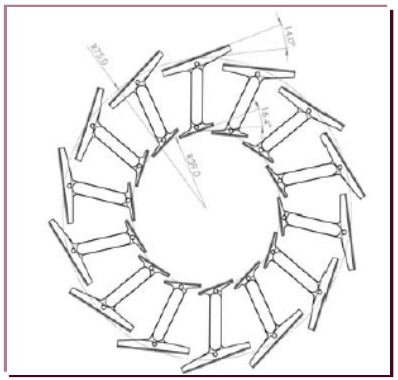




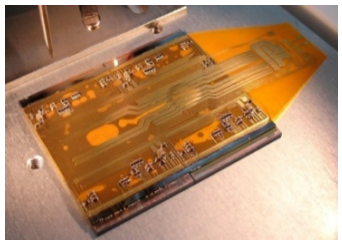
Quad Pixel Sensor Sensor



Forward Pixel Services

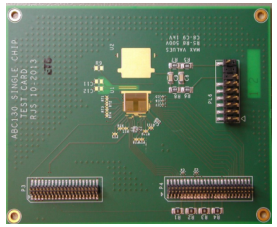


Possible Barrel Support Concept

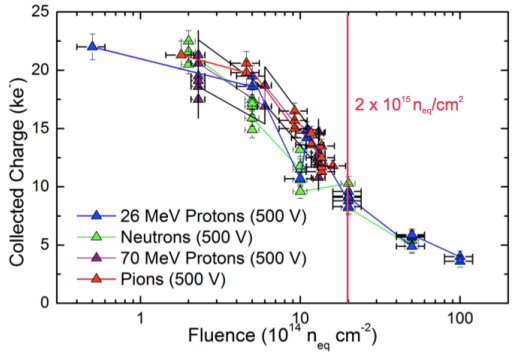


Quad Pixel Module

ITk Strip Tracker

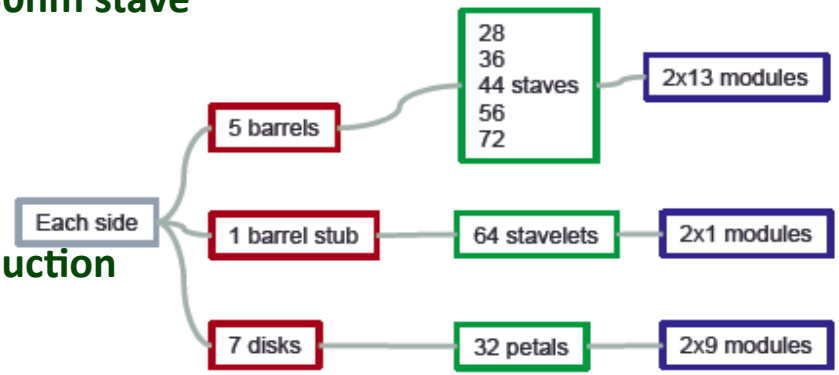


- New n-in-p sensor prototype delivered with 4 rows of 2.4cm long strips at 74.5µm pitch
- New 130nm CMOS ASIC with 256 channels received

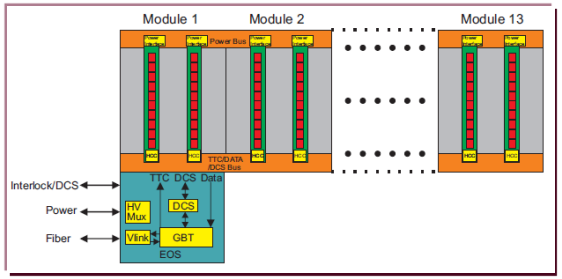


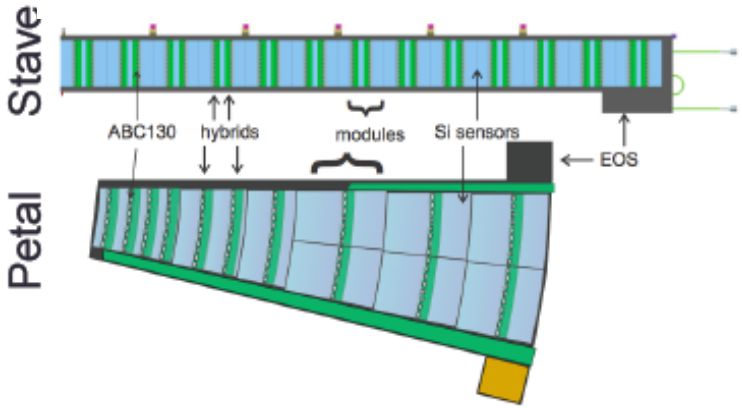
- Strip modules (single/double sided) prototyped with 250nm ASICs
- Large area stave DC-DC prototype (120cm×10cm) produced and under study
- Serial and DC-DC powering studied on the short 250nm stave

- Other new chips (HCC, DC-DC, etc)
- Hybrid/module designs for them completed



- Local supports prototyped and further material reduction achieved
- Progress in Petal and Stave support designs
- End-of-stave card for 130nm developed

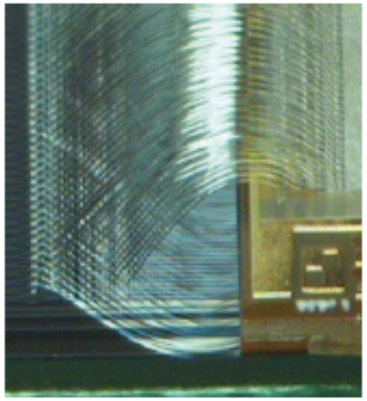




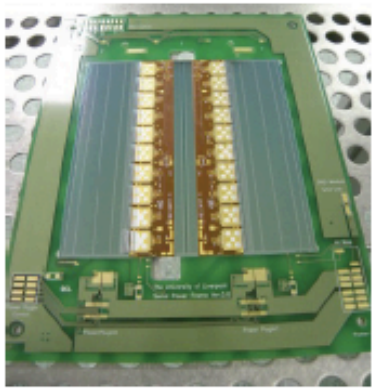
ITk Strip Prototype Components

Sensor: 4 strip rows

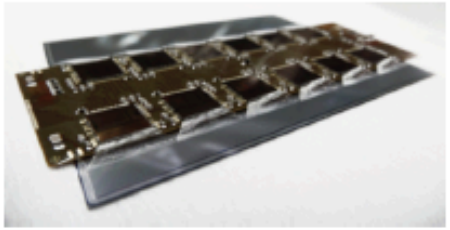
4 row wire bonds

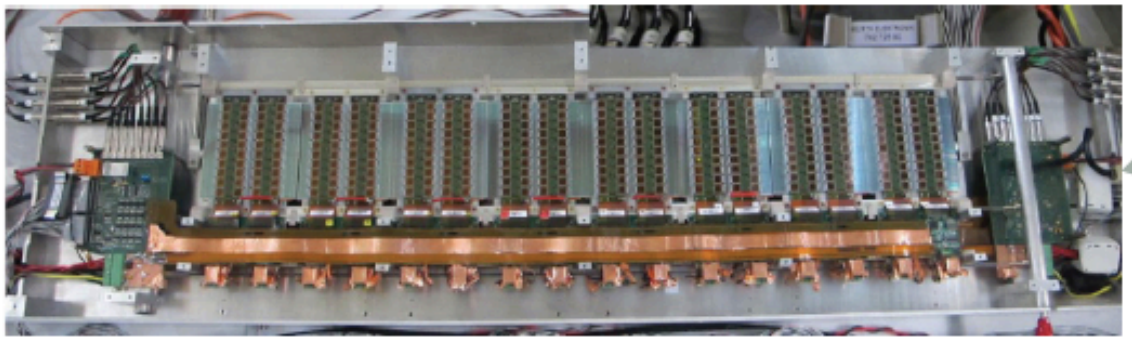


Barrel module



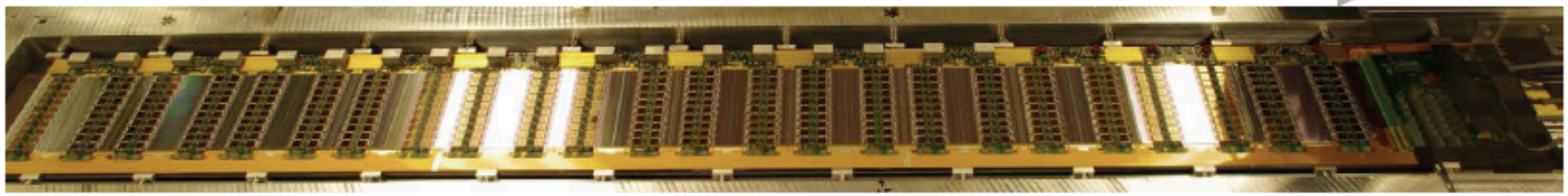
Prototype EC module





Double sided 8 module stavelet

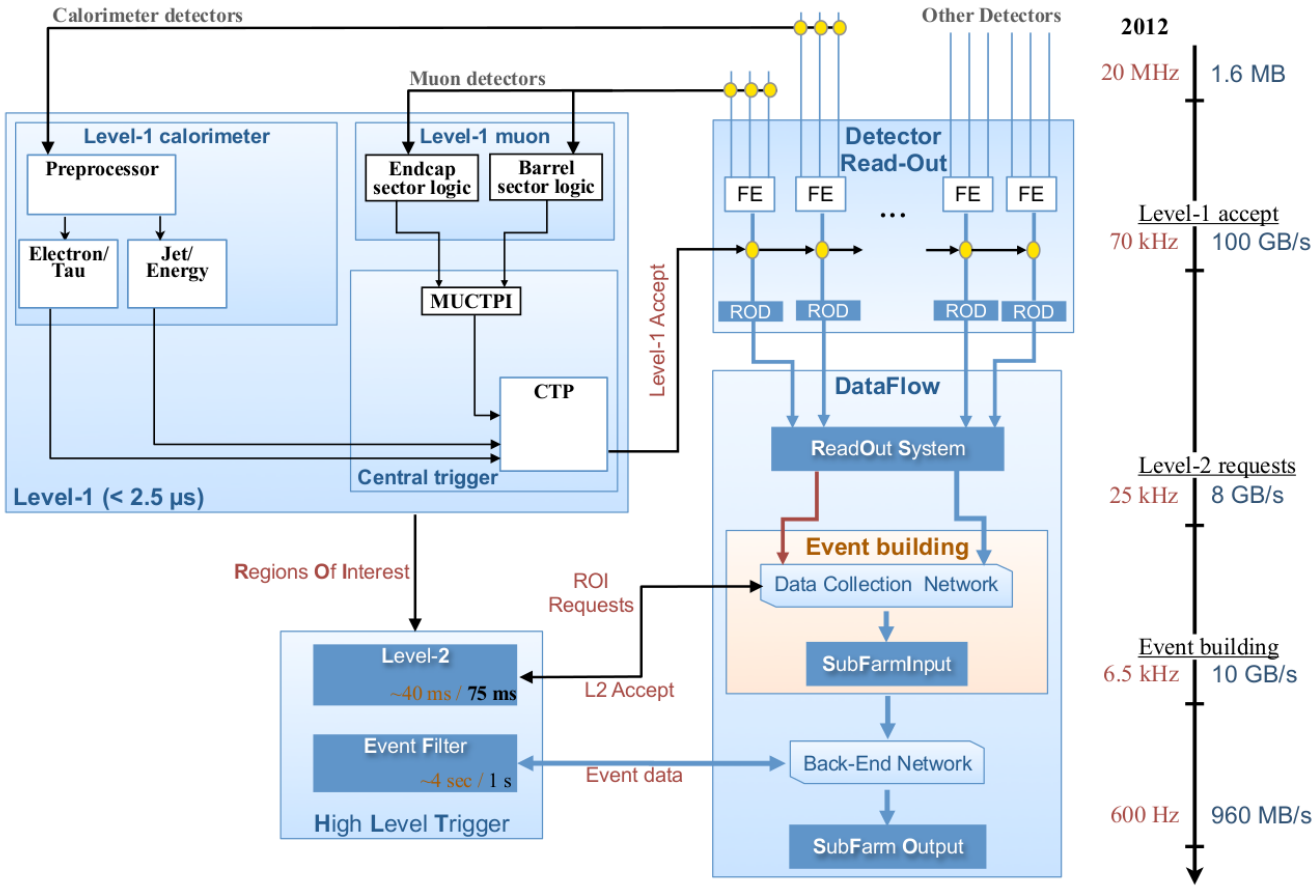
12 module stave



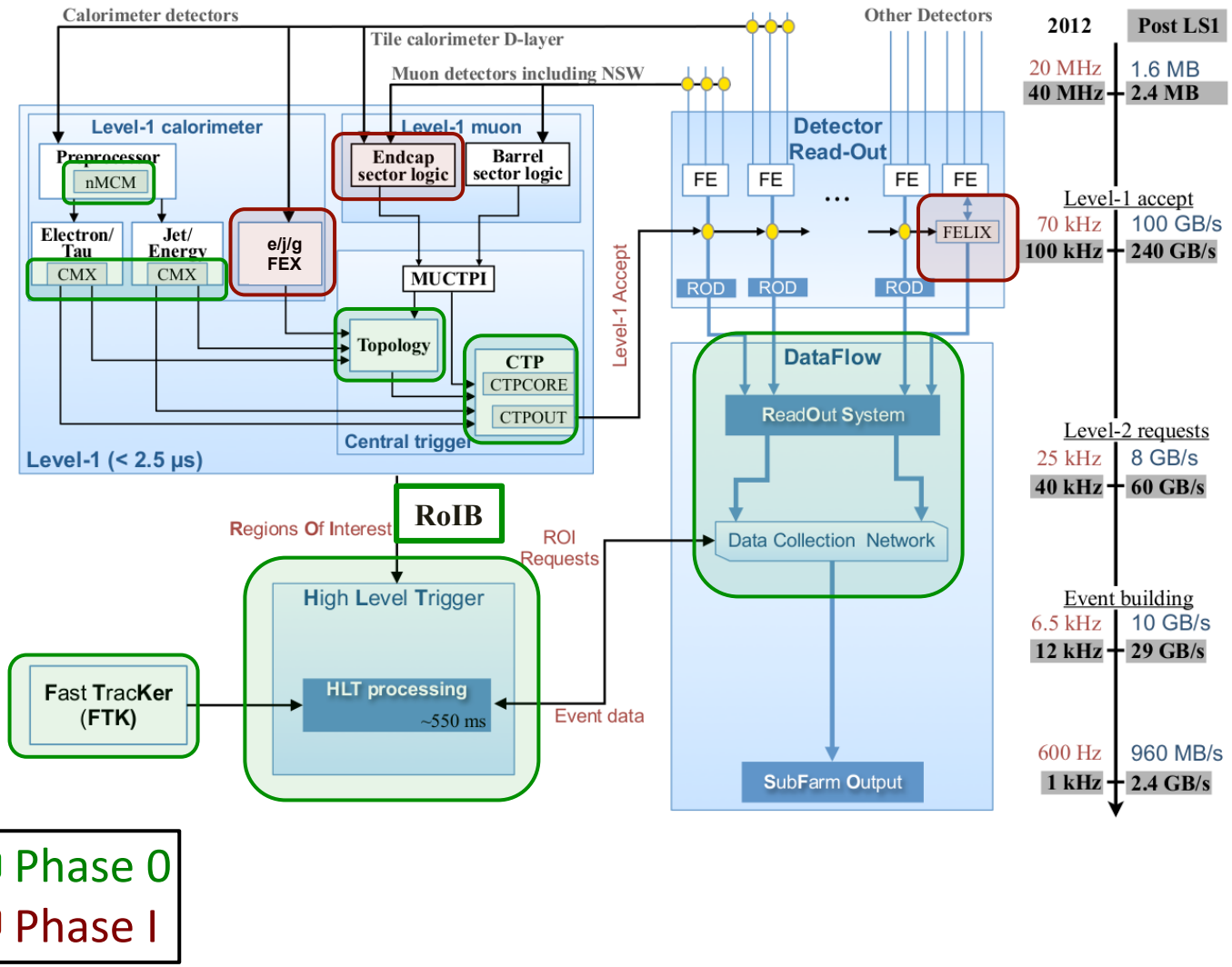
TDAQ System Upgrade

- Phase-I: Fast TracKer (FTK),
  Level-1 Calorimeter Trigger (L1CALO),
  Front-End LInk eXchange (FELIX)
- Phase-II: Trigger architecture

ATLAS TDAQ


Calorimeter detectors
Other Detectors
2012
Muon detectors
Level-1 calorimeter
Preprocessor
Electron/ Tau
Jet/ Energy
Level-1 muon
Endcap sector logic
Barrel sector logic
MUCTPI
CTP
Central trigger
Level-1 (< 2.5 μs)
Level-1 Accept
Detector Read-Out
FE
ROD
DataFlow
ReadOut System
Event building
Data Collection Network
SubFarmInput
Back-End Network
SubFarm Output
Regions Of Interest
ROI Requests
L2 Accept
Event data
Level-2
~40 ms / 75 ms
Event Filter
~4 sec / 1 s
High Level Trigger
20 MHz
1.6 MB
Level-1 accept
70 kHz
100 GB/s
Level-2 requests
25 kHz
8 GB/s
Event building
6.5 kHz
10 GB/s
600 Hz
960 MB/s

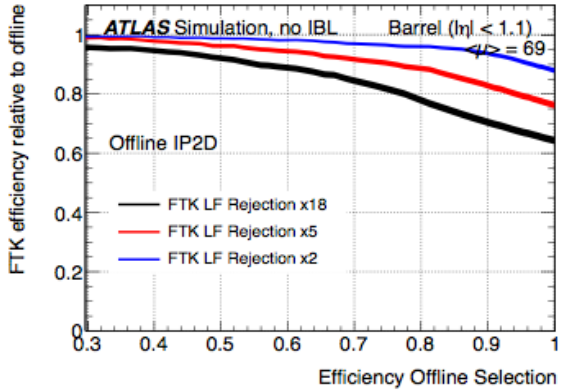
ATLAS TDAQ after LS1

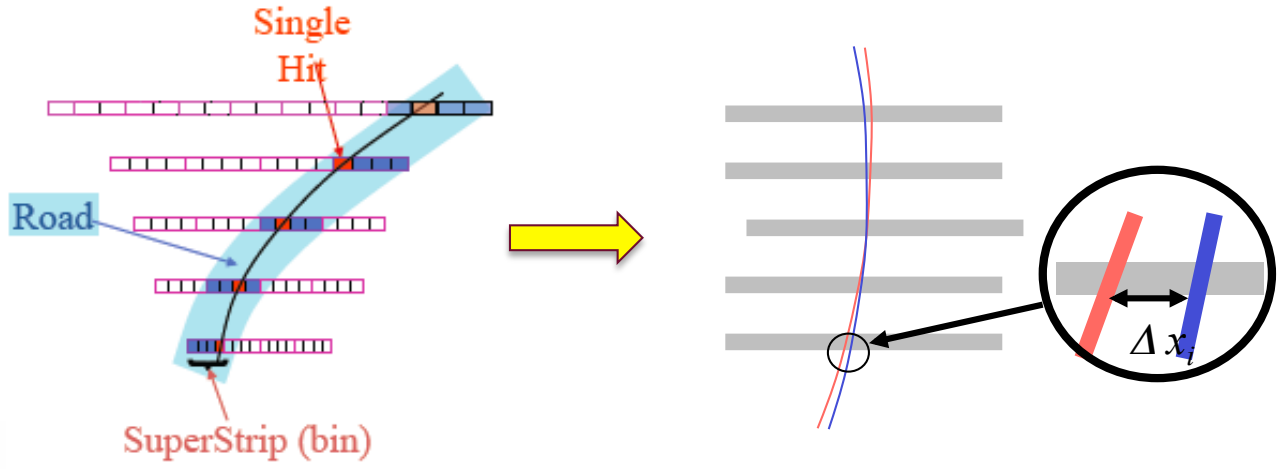


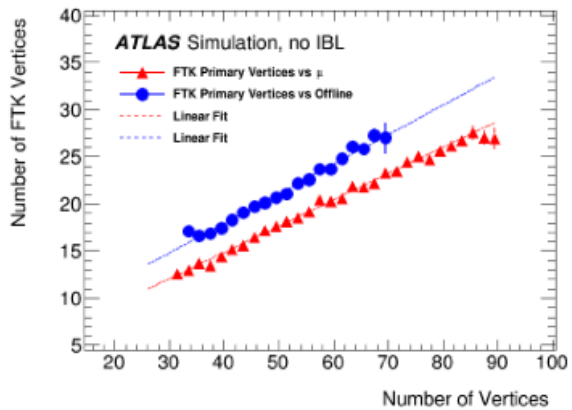
FTK

Use hardware to perform the global tracking @100 kHz in two steps

- **Pattern recognition with Associative Memory**
- **Track fitting with DSPs in FPGA**







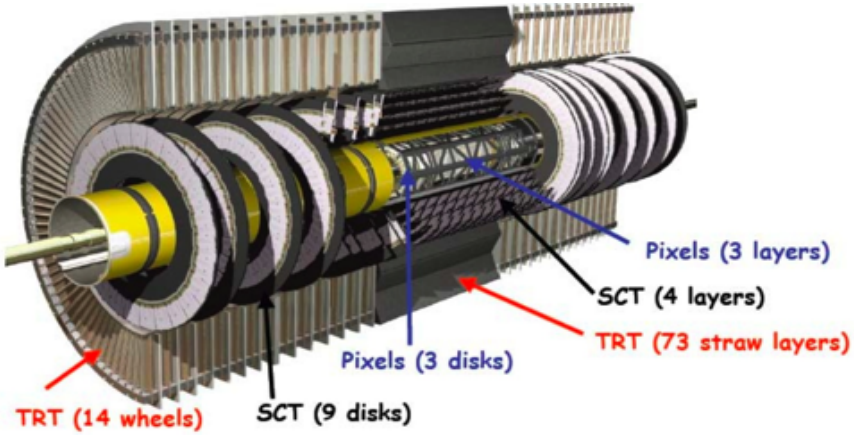
Pattern recognition in coarse resolution (superstrip➔road)

Track fit in full resolution (hits in a road)

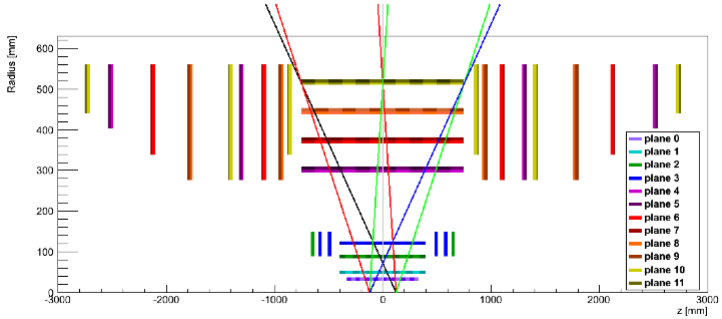
$F(x_1, x_2, x_3, \ldots) \sim a_0 + a_1\Delta x_1 + a_2\Delta x_2 + a_3\Delta x_3 + \ldots = 0$

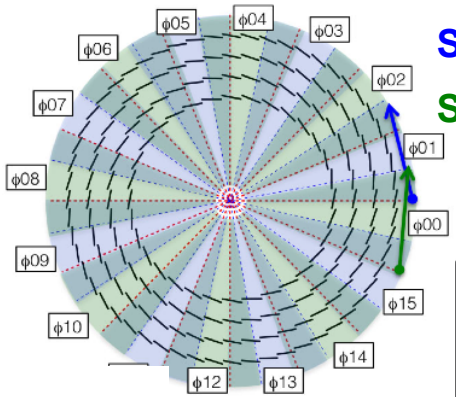
Road size to balance the workload between two steps (pattern size vs fitting combinatorics)

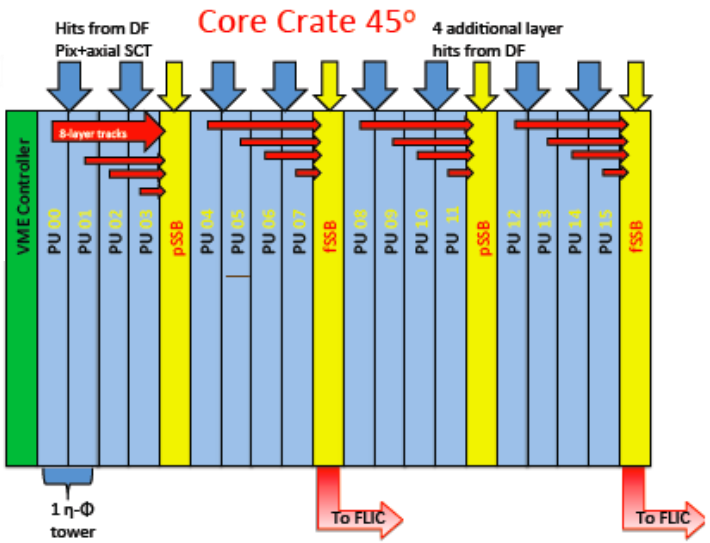
System Overview



- Detector silicon trackers, PIX (4 layers) & SCT (4 double layers)
- Pattern matching and initial track fitting with 3 PIX, 4 SCT axial and 1 SCT stereo layers
- IBL, other SCT stereo layer extrapolation and 12-layer fit

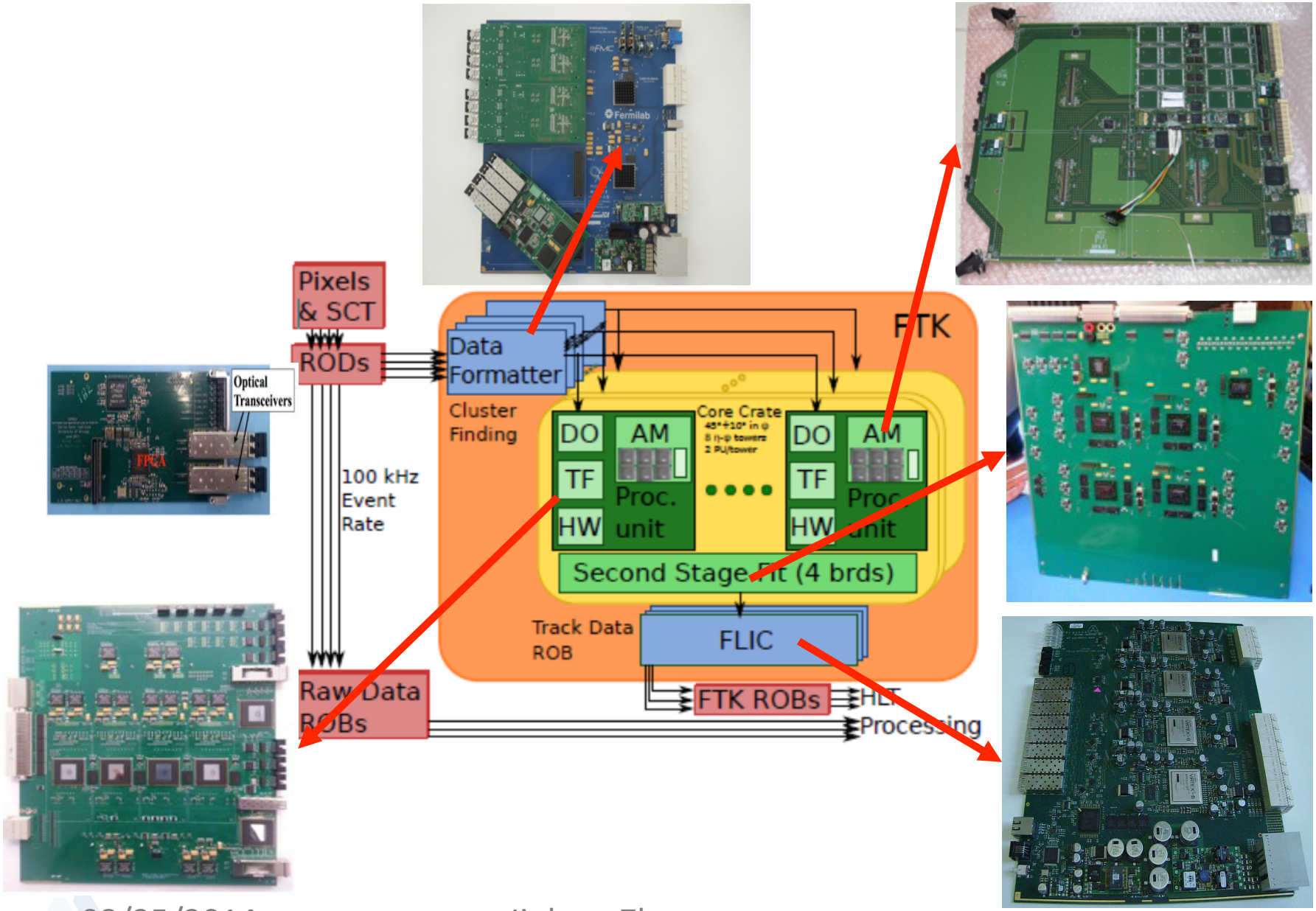






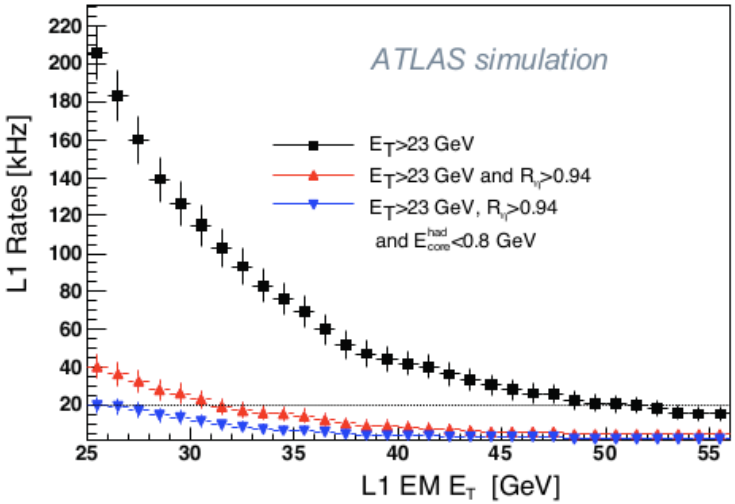
- 16 overlapping ϕ sectors, each sector further divided into 4 η towers
- 8 crates @ 10^{34} total planned, one crate processing 4X2 η−ϕ towers

Function Schematic & Prototypes

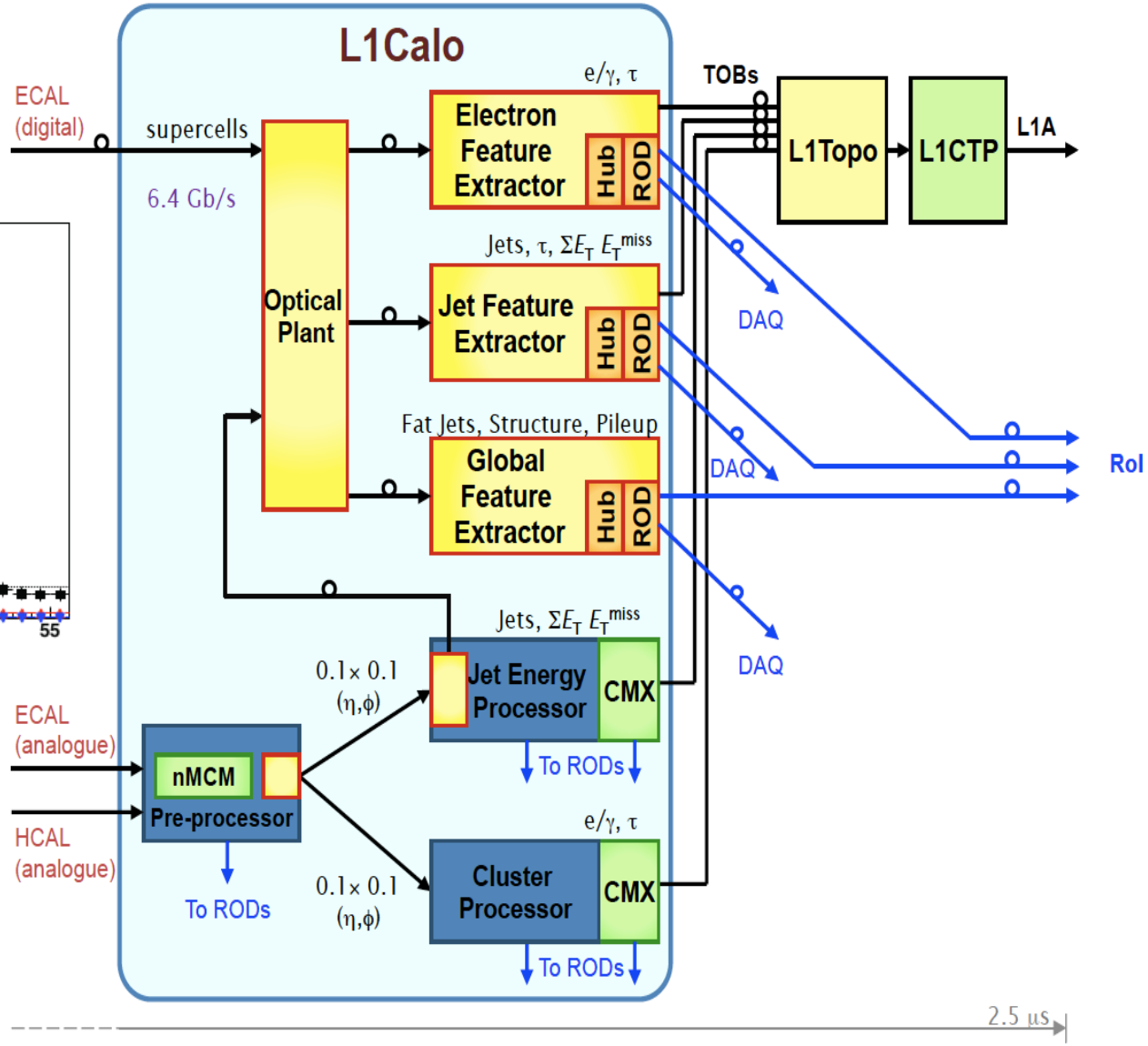


L1CALO in Phase-I

$$R_\eta = \frac{E_{3\times 2}}{E_{7\times 2}}$$

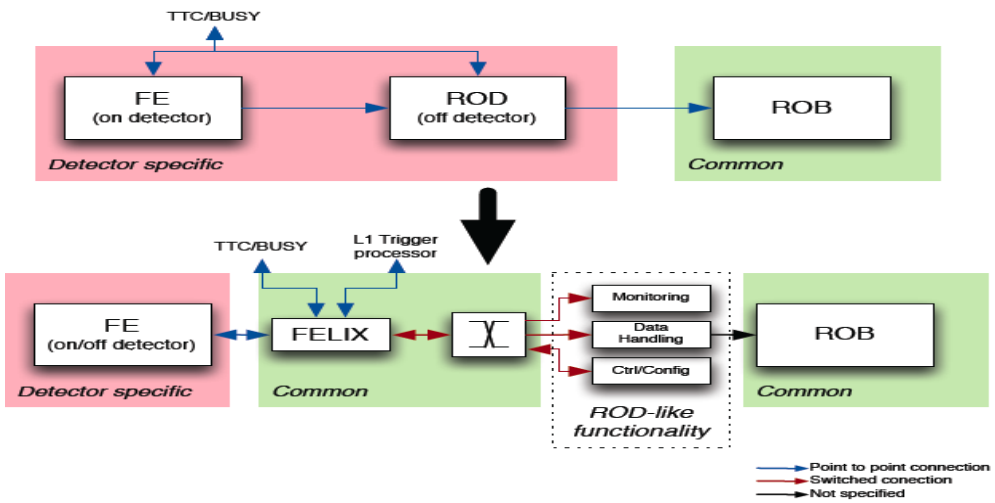


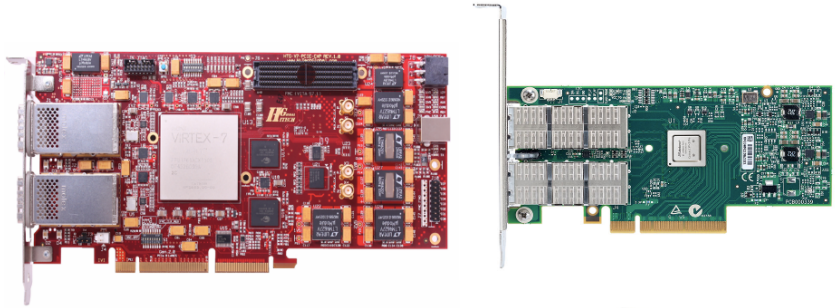
Retain unprescaled single lepton triggers with p_T threshold of 20–25 GeV

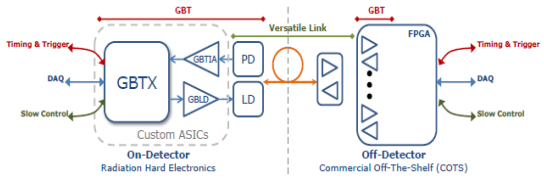


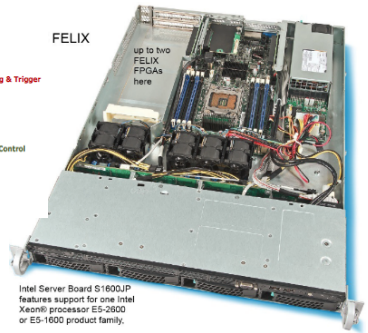
FELIX for Readout Upgrade

- Enabling transition from custom hardware to COTS as early as possible
- Using high level switch protocols of high speed and large bandwidth
- Configurable and flexible data routing and error handling, without relying on detector specific hardware
- Direct low latency paths between links
- Universal ATLAS-wide TTC/BUSY handling as for now
- Command scheduling with guaranteed timing for calibration

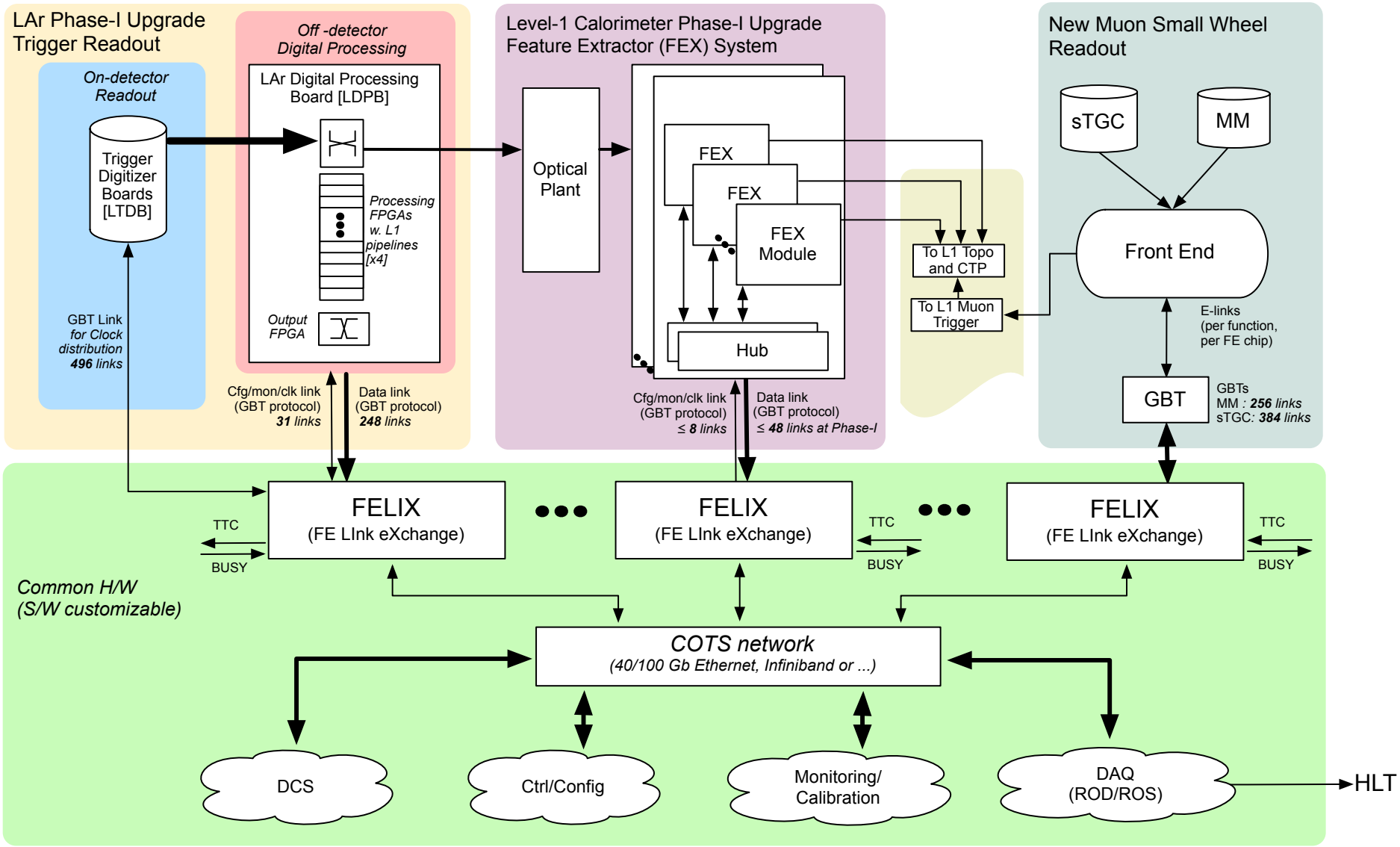




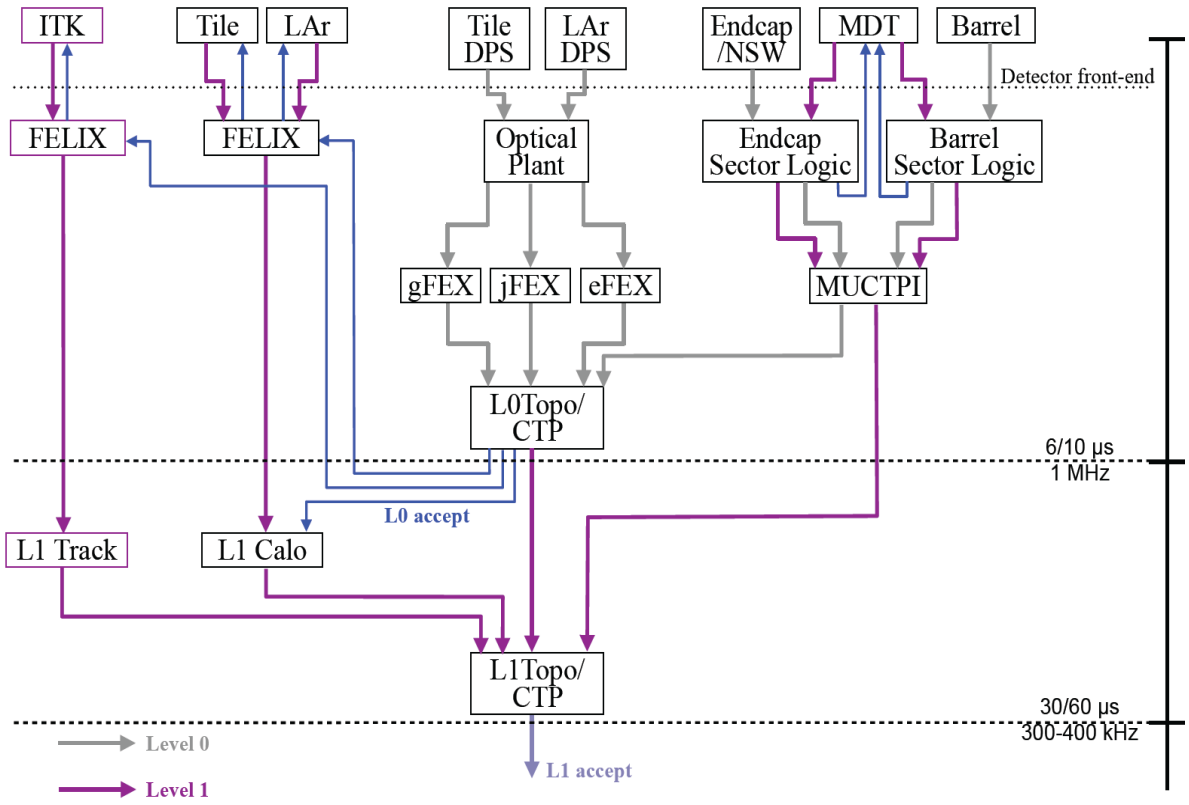




FELIX in Phase-I

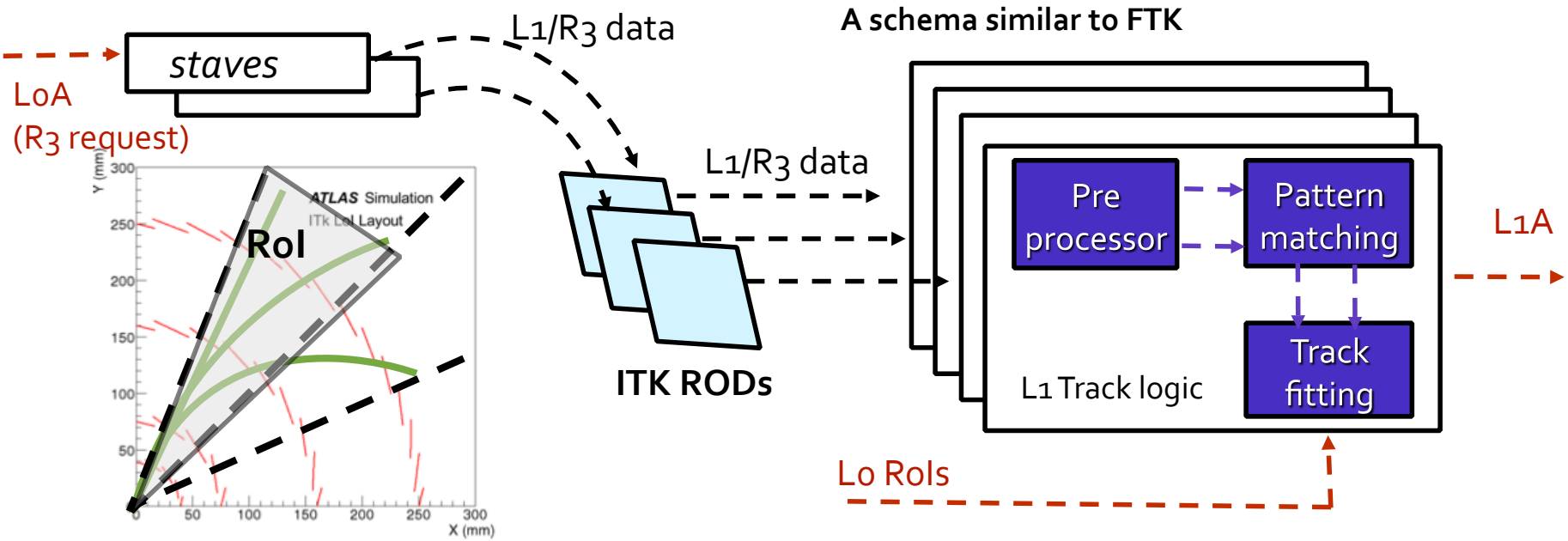


Phase-II Trigger Architecture

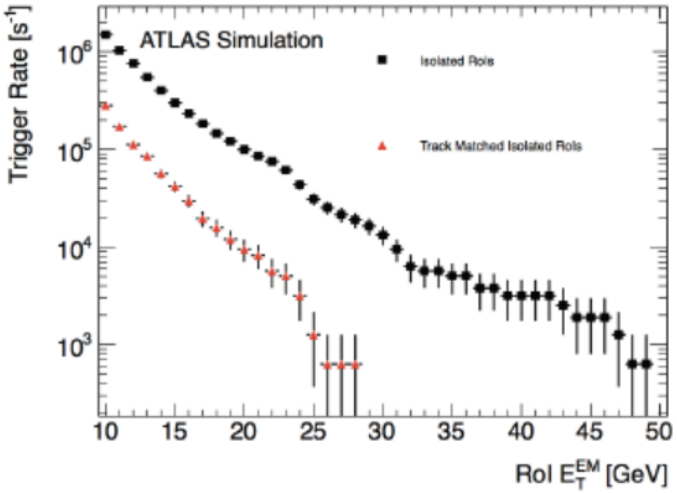


- A trigger architecture proposed in the ATLAS Phase-II upgrade LoI
  - FTK-like Level-1 Track Trigger (L1Track) system
  - Phase-I Level-1 becoming Level-0
- The Baseline requirements
  - L0 Accept: 1 MHz after a latency of 6 µs
  - L1 Accept: 300–400 kHz after an additional latency of 24 µs

L1Track



- **Processing ITK clusters , finding tracks thus refining objects associated with L0 RoIs**
- **A FTK like system but**
  - **Lower latency and higher parallelism**
  - **Using partial event since RoI based**
- **Possible challenge from the ITk full detector readout at L0A**



Summary

- **ATLAS has a coherent plan for upgrades through the coming years to meet the challenges up to and in the HL-LHC era. Not mentioning in this presentation:**
  - **Phase-I: AFP**
  - **Phase-II: HR/HV-CMOS R&D, Hadronic Endcap Calorimeter electronics, Forward Calorimeters, Muon detector electronics, extension to large η, … …**
  - **Software and Computing**
- **Major R&D programs are targeting most upgrades needed for ATLAS to operate at luminosities far beyond the design.**