Triggering at HL-LHC

Challenges + Instrumentation Developments

Wesley H. Smith

U. Wisconsin – Madison

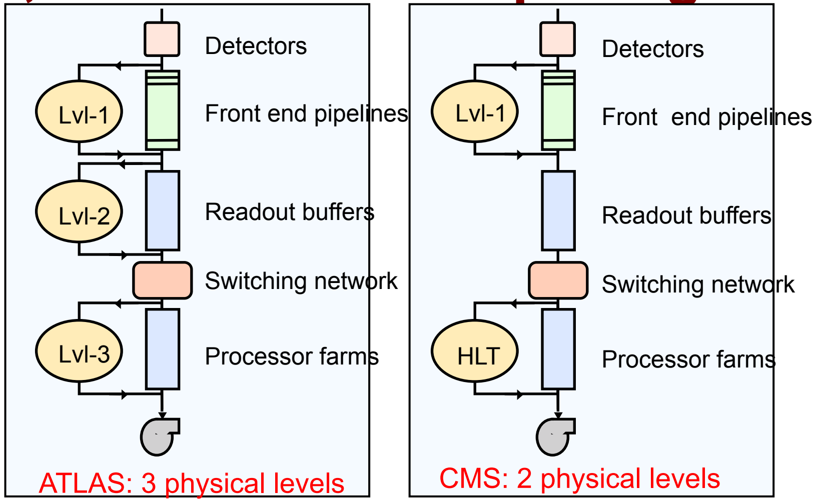
Next steps in the Energy Frontier - Hadron Colliders

August 25, 2014

Journey to HL-LHC

2012-2013 run:

- **Lumi = 7 x 10^{33}, PU = 30, E = 7 TeV, 50 nsec bunch spacing**
- **2012 ATLAS, CMS operating:**
  - L1 Accept ≤ 100 kHz,
  - Latency ≤ 2.5 (AT), 4 μsec (CM)
  - HLT Accept ≤ 1 kHz

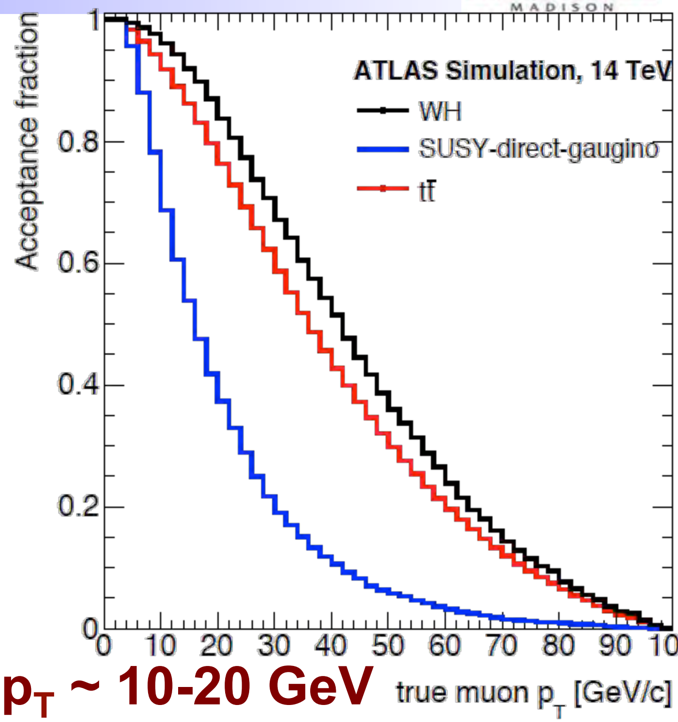


Where ATLAS & CMS will be:

- **Lumi = 5-7 x 10^{34}**
- **<PU> = 140, Max PU = 200 (increase × 6)**
- **E = 14 TeV (increase × 2)**
- **25 nsec bunch spacing (reduce × 2)**
- **Integrated Luminosity > 250 fb^{-1} per year**

Need to establish scenario for L1 Accept, Latency, HLT Accept & new trigger "features" (e.g. tracking trigger)

Need for Trigger Upgrade



Maintaining current physics sensitivity at HL-LHC challenging for trigger

- EWK, top (and Higgs) scale physics remain critical for HL-LHC
- 100 kHz L1 bandwidth saturated in 2012 with instantaneous luminosity below 10^{34} $cm^{-2}s^{-1}$
- Cannot fit same "interesting" physics events in trigger at 13 TeV, $5x10^{34}$ $cm^{-2}s^{-1}$

- **Increasing p_T thresholds reduces signal efficiency**
  - Trigger on lepton daughters from H→ZZ at p_T ~ 10-20 GeV
  - Very easy to reach the worst case: thresholds increase beyond energy scale of interesting processes
- **Backgrounds from HL-LHC pileup further reduces the ability to trigger on rare decay products**
  - Leptons, photons no longer appear isolated and are lost in QCD backgrounds
  - Increased hadronic activity from pileup impacts jet p_T and MET measurements

Overview: Improving L1 Trigger

Lepton/Photon Triggers

- **Improved performance by adding L1 track information**
  - Improves the muon momentum measurement
  - Reduces fake electrons via tracker + calorimeter matching
  - Dramatically improved tau trigger efficiency
  - Use tracking isolation instead of calorimeter isolation
- **Using improved calorimeter granularity at L1 further improves EM fake rejection**

Hadronic Triggers

- **Triggering on jets, missing energy**
  - L1 track information can be used to reject jets from pileup interactions
- **Loose (as loose as possible) trigger selection will be necessary to ensure high signal efficiency**
  - Increase trigger bandwidth at each trigger stage and output to disk
  - Allows detailed processing for refined selection where resources are most plentiful

Differences btw. ATLAS, CMS

Trigger Rates:

- **L1 tracking trigger rate affected by difference in magnetic field,**
- **L1 calorimeter trigger is impacted by the different geometry and ATLAS' ability to point to the IP**
  - Affects impact of tracking trigger on electrons
- **The L1 muon trigger is impacted by the difference in type of information available in L1.**
- **Therefore, one should not at the outset assume the same trigger rates from ATLAS and CMS.**

Architectural Considerations:

- **ATLAS has used a Region of Interest strategy deployed with a Level-2 Trigger following Level-1**
- **CMS does not use regions of interest at the lower levels of triggering, following the Level-1 Trigger directly with the Computer Farm-based Higher Level Triggers which use RoI based on L1 info.**
- **These decisions affect the electronic readout systems of both detectors and their options for upgrades.**
- **Latency: differences in Front End electronics systems may restrict either ATLAS or CMS from increasing Latency from 10 to 20 μsec.**
  - Constrains designs using L0/L1 or L1 Region of Interest

ATLAS & CMS @ HL-LHC

An introductory Summary

ATLAS*:

- **Divide L1 Trigger into L0, L1 of latency 6, 30 μsec, rate ≤ 1 MHz, ≤ 400 kHz, HLT output rate of 5 - 10 kHz**
  - Calorimeter readout at 40 MHz w/backend waveform processing (140 Tbps)
- **L0 uses Cal. & μ Triggers, which generate track trigger seeds**
- **L1 uses Track Trigger & more muon detectors & more fine-grained calorimeter trigger information.**

CMS:

- **L1 Trigger latency: 12.5 μsec**
- **L1 Trigger rate: 500 kHz (PU=140), 750 kHz (PU=200)**
- **L1 uses Track Trigger, finer granularity μ & calo. Triggers**
- **HLT output rate of 5 kHz (PU=140), 7.5 kHz (PU=200)**

ATLAS & CMS Triggered vs. Triggerless Ph. 2 Architectures

1 MHz (Triggered):

- **Network:**
  - 1 MHz with ~5 MB: aggregate ~40 Tbps
  - Links: Event Builder-cDAQ: ~ 500 links of 100 Gbps
  - Switch: almost possible today, for 2022 no problem
- **HLT computing:**
  - General purpose computing: 10(rate)x3(PU)x1.5(energy)x200kHS6 (CMS)
    - **Factor ~50 wrt today maybe for ~same costs**
  - Specialized computing (GPU or else): Possible

40 MHz (Triggerless):

- **Network:**
  - 40 MHz with ~5 MB: aggregate ~2000 Tbps
  - Event Builder Links: ~2,500 links of 400 Gbps
  - Switch: has to grow by factor ~25 in < 10 years, difficult
- **Front End Electronics**
  - Readout Cables: Copper Tracker! – Show Stopper
- **HLT computing:**
  - General purpose computing: 400(rate) x3(PU)x1.5(energy)x200kHS6 (CMS)
    - **Factor ~2000 wrt today, but too pessimistic since events easier to reject w/o L1**
    - **This factor looks impossible with realistic budget**
  - Specialized computing (GPU or …)
    - **Could possibly provide this …**

Trigger Challenges at HL-LHC: ATLAS & CMS

Goals:

- **Study with high precision properties of Higgs with focus on self-couplings and precision measurements of couplings**
  - Keep trigger acceptance for Higgs at least as high as in 2012.
- **Keep same sensitivity for SUSY and Exotic searches as in 2012.**

Challenges:

- **Higher Interaction Rates**
  - For physics of interest and backgrounds!
  - ~ 6k primary tracks per bunch crossing within $|\eta|<2.5$ plus conversions and nuclear interactions ~ one order of magnitude larger than 2012
- **Occupancy causes degraded performance of algorithms**
  - Electrons: reduced rejection at fixed efficiency from isolation
  - Muons: increased background rates from accidental coincidences
- **Implies raising E_T thresholds on electrons, photons, muons, jets and use of less efficient multi-object triggers, unless we have new information $\Rightarrow$ Tracker at L1**
  - Compensate for larger interaction rate & degradation in algorithm performance

ATLAS & CMS L1 Tracking Trigger

Reduces Leptonic Trigger Rate

- Validate calorimeter or muon trigger object, e.g. discriminating electrons from hadronic ($\pi^0 \rightarrow \gamma\gamma$) backgrounds in jets
- Addition of precise tracks to improve precision on p_T measurement, sharpening thresholds in muon trigger
- Degree of isolation of e, γ, μ or τ candidate
- Requires calorimeter trigger trigger at the finest granularity to reduce electron trigger rate

Other Triggers

- Primary z-vertex location within 30 cm luminous region derived from projecting tracks found in trigger layers,
- Provide discrimination against pileup events in multiple object triggers, e.g. in lepton plus jet triggers.

HL-LHC L1 Track Trigger Architectures:

"Self - seeded" path (CMS Tracker Approach):

- L1 tracking trigger data combined with calorimeter & muon trigger data regionally with finer granularity than presently employed.
- After regional correlation stage, physics objects made from tracking, calorimeter & muon regional trigger data transmitted to Global Trigger.

"RoI - based" path (ATLAS Tracker Approach):

- L1 calorimeter & muon triggers produce a "Level-0" or L0 "pre-trigger" after latency of present L1 trigger, with request for tracking info at ≤ 1 MHz. Request only goes to regions of tracker where candidate was found. Reduces data transmitted from tracker to L1 trigger logic by ≤ 40 (40 MHz to ≤ 1 MHz) times probability of a tracker region to be found with candidates, which could be less than 10%, (e.g. 100 kHz, ~ speed of ATLAS FTK)
- Tracker sends out info. for these regions only & this data is combined in L1 correlation logic, resulting in L1A combining track, muon & calo. info..

"HLT Usage" (both ATLAS & CMS):

- L1 Track trigger info, along with rest of information provided to L1 is used at very first stage of HLT processing. Provides track information to HLT algorithms very quickly without having to unpack & process large volume of tracker information through CPU-intensive algorithms. Helps limit the need for significant additional processor power in HLT computer farm.

ATLAS Phase 2 Trigger Scenario
(Taken from ATLAS Phase II LoI)

Constraints:

- **MDT limiting case in rate, latency (30% ~ inaccessible)**

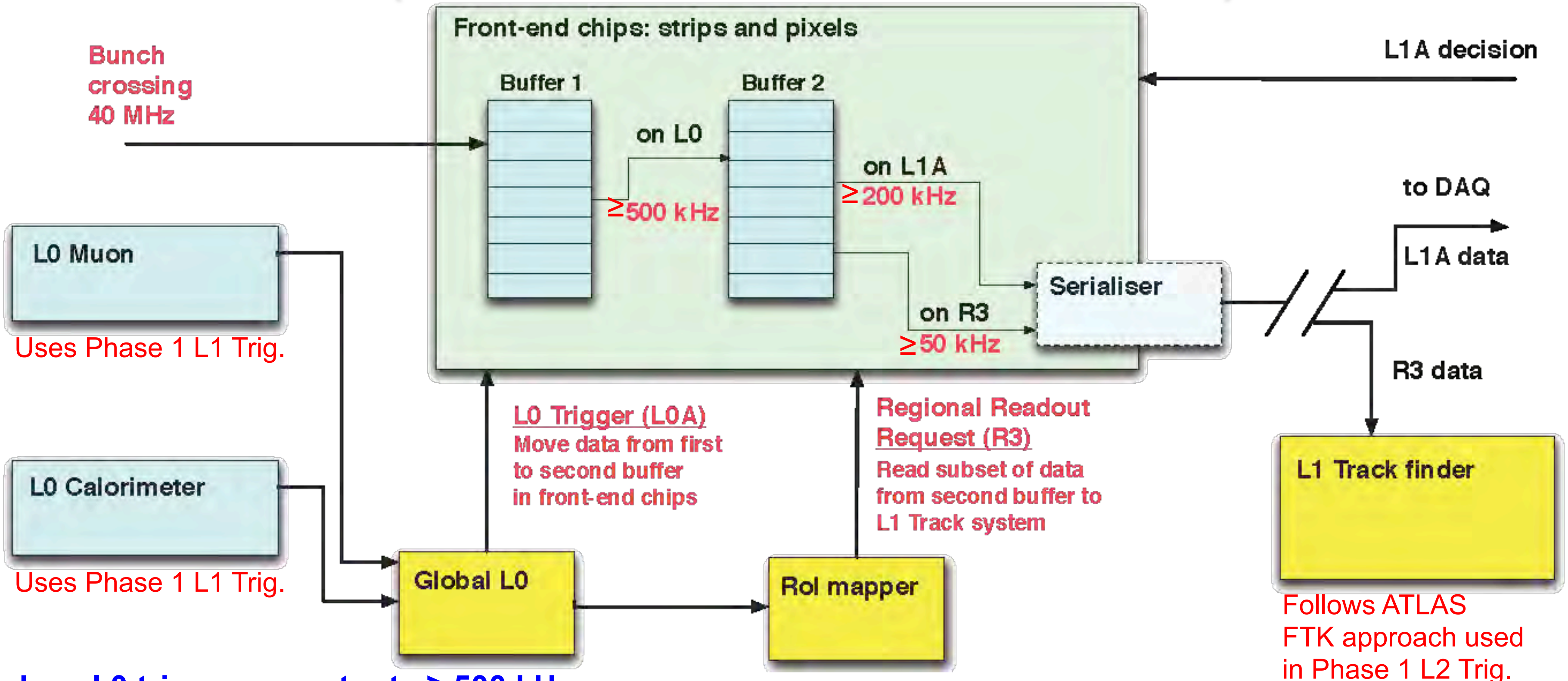
Constraints	Max Rate	Max Latency
MDT	~ 200 kHz	~ 20 μsec
LAr	Any	Any
Tile	> 300 kHz	Any
ITK	> 200 kHz	< 500 μsec

Rate Estimates:

- **Estimate of HL-LHC rates based on Phase-1 system**
- **Trigger rate at least 500 kHz w/o track trig.**

Object(s)	Trigger	Estimated Rate No L1Track	With L1Track
e	EM20	200 kHz	40 kHz
γ	EM40	20 kHz	10 kHz
μ	MU20	> 40 kHz	10 kHz
τ	TAU50	50 kHz	20 kHz
ee	2EM10	40 kHz	< 1 kHz
$\gamma\gamma$	2EM10	as above	~5 kHz
$e\mu$	EM10_MU6	30 kHz	< 1 kHz
$\mu\mu$	2MU10	4 kHz	< 1 kHz
$\tau\tau$	2TAU15I	40 kHz	2 kHz
Other	JET + MET	~100 kHz	~100 kHz
Total		**~500 kHz**	**~200 kHz**

ATLAS "Double buffer" readout
(Taken from ATLAS Phase II LoI)



- Level 0 trigger accept rate ≥ 500 kHz
  - On an L0 accept, copy data from primary to secondary buffer
  - Identify "Regions" in detector (~10% of the detector on each L0 accept) like L1 RoI
  - Generate "Regional Readout Request" (R3) - modules in "Region" read out subset of their data
- On an L1 accept (≥ 200 kHz), all modules read out event from Secondary buffer
- Since only ~10% of the detector (the "Regions") will be read out on the Level 0 accept, R3 request rate for any specific part of the detector will be ≥ 50 kHz

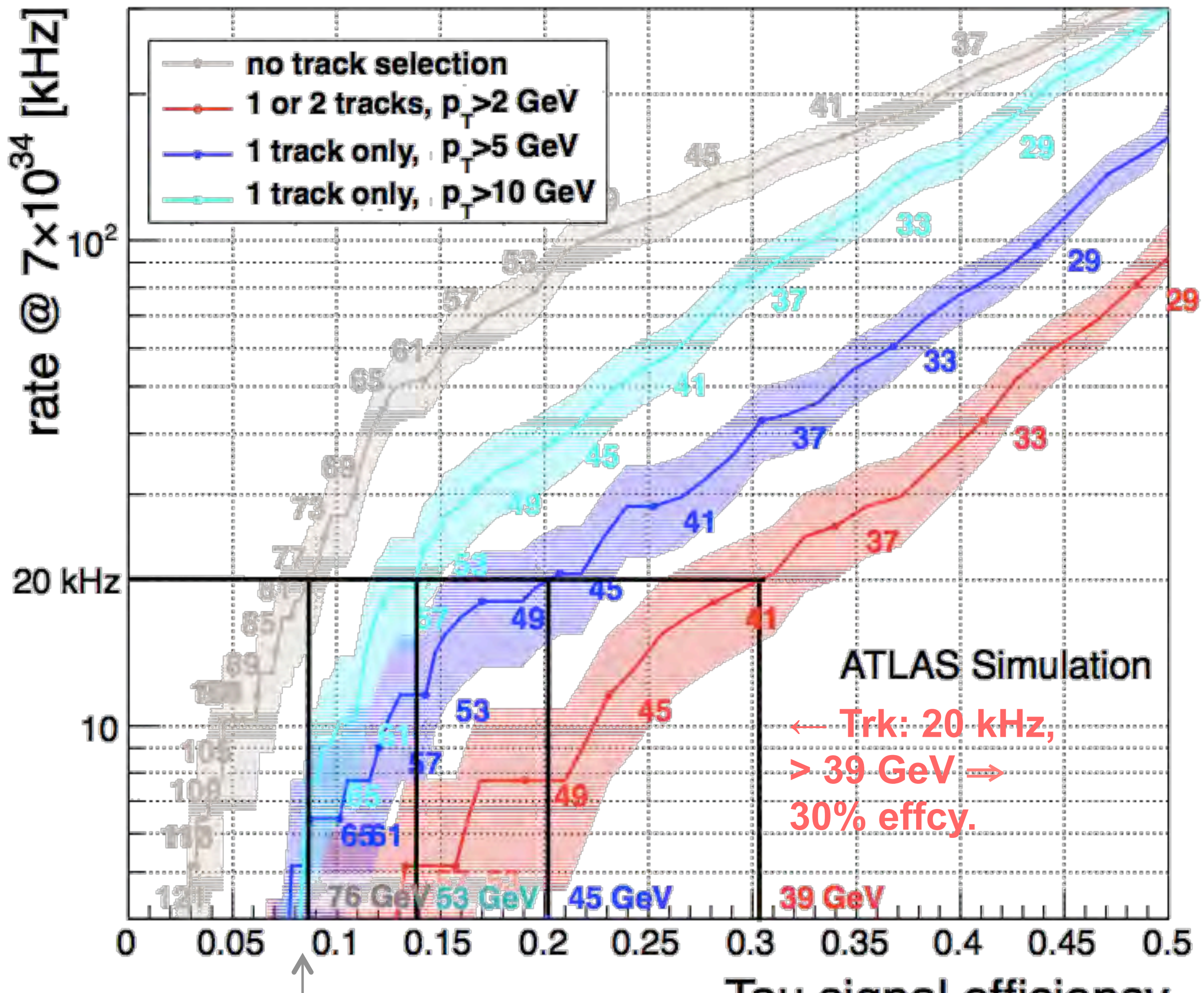
ATLAS Gains from Track Trigger

- Matching tracks to Level 1 objects (electrons, taus and muons) can significantly reduce rate
  - Remove mis-reconstructed or fake objects
  - Ensure objects come from the same vertex
- Potential benefits have been studied for electrons, muons, taus and jets, single and multiple/combined object triggers using both smeared offline tracks, and smeared truth particles
  - Even modest resolution tracking information (p_T, η, φ) can provide sufficient rejection
  - Factors of between 3 and 5 for electrons, taus, muons (p_T > 20 GeV) with only small efficiency losses (~5%) wrt. Phase 1 Trigger system.
    - Taus on next slide

ATLAS Gain from Track Trigger

Rate vs. tau finding efficiency curves for taus from the decay of a 120 GeV Higgs boson for the inclusive tau trigger at 7×10^{34} cm^{-2} s^{-1} for different track multiplicity and minimum track p_T requirements.

The bands show the rate vs. efficiency parameterized for different L1 cluster E_T thresholds, shown as the small numbers next to the corresponding points on each band.



No Trk: 20 kHz, > 76 GeV ⇒ 10% effcy.

CMS Phase 2 Trigger Scenario

Replace ECAL Barrel and Endcap Front End electronics

- **Allows L1 latency & accept rate increases (below)**
- **Includes providing individual crystal level (not 5x5 sums) trigger information**
  - Resolution based on $\Delta\eta\times\Delta\phi = 0.087\times0.087 \rightarrow 0.017\times0.017$
  - Improved spike rejection in EB
- **Assume: EE electronics replaced with EE replacement**

Latency of 12.5 μsec

- **Limit from Endcap Muon Cathode Strip Chamber Front End Electronics ~ 10 usec**
- **Complications for tracker readout above 12.5 μsec**

L1 Accept rate of 500 kHz (140 PU) 750 kHz (200 PU)

- **Provides more acceptance and lower thresholds**
- **Limits provided by DAQ readout, EVB, & HLT CPU, pixel readout**
- **Requires: Drift Tube Readout Electronics replacement (planned)**

Tracking Trigger

- **Leptons: P_T cut & isolation, Jets: Vertex**

New L1 Trigger (Calorimeter, Muon, Global) to incorporate Track Trigger

- **Finer calorimeter cluster trigger, muon & calorimeter seeds for track match**
- **Also incorporate additional muon chambers for |η| > 1.5 (e.g. GEMs)**

HLT Output Rate of 5 kHz (140 PU) 7.5 kHz (200 PU)

- **Limit from Downstream Computing**

CMS Tracking Trigger

Outer Tracker "Baseline"

- Lighter Tracker, with better overall Tracking and Calorimetry performance compared to the present systems
- Level-1 Tracking Trigger including all tracks with p_T > 2 GeV, well measured & with ~ 1mm primary vertex resolution
- Pursuing a "Push" Architecture based on
  - **Module filtering of hits from tracks with p_T above ~ 2 GeV**
  - **Low power (low mass) 5 GHz optical links**
  - **Lower latency, less hits produced up front**

Inner Pixel Option

- **Usable for B-tags, Taus, c, electron-ID, added vertex info.**
- **Exploring a Region of Interest "Pull" architecture**
- **As a possible complement to the L1 "Push" Tracking Trigger and/or HLT pre-processor**
- **Not decided if it is needed**

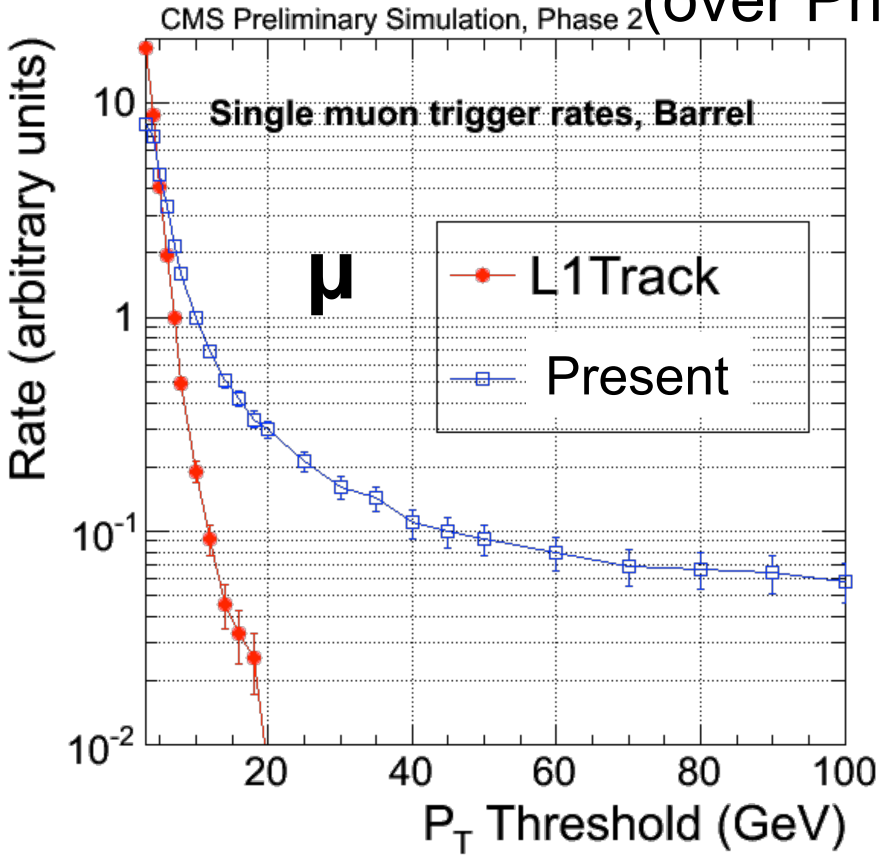
CMS Gains from Track Trigger

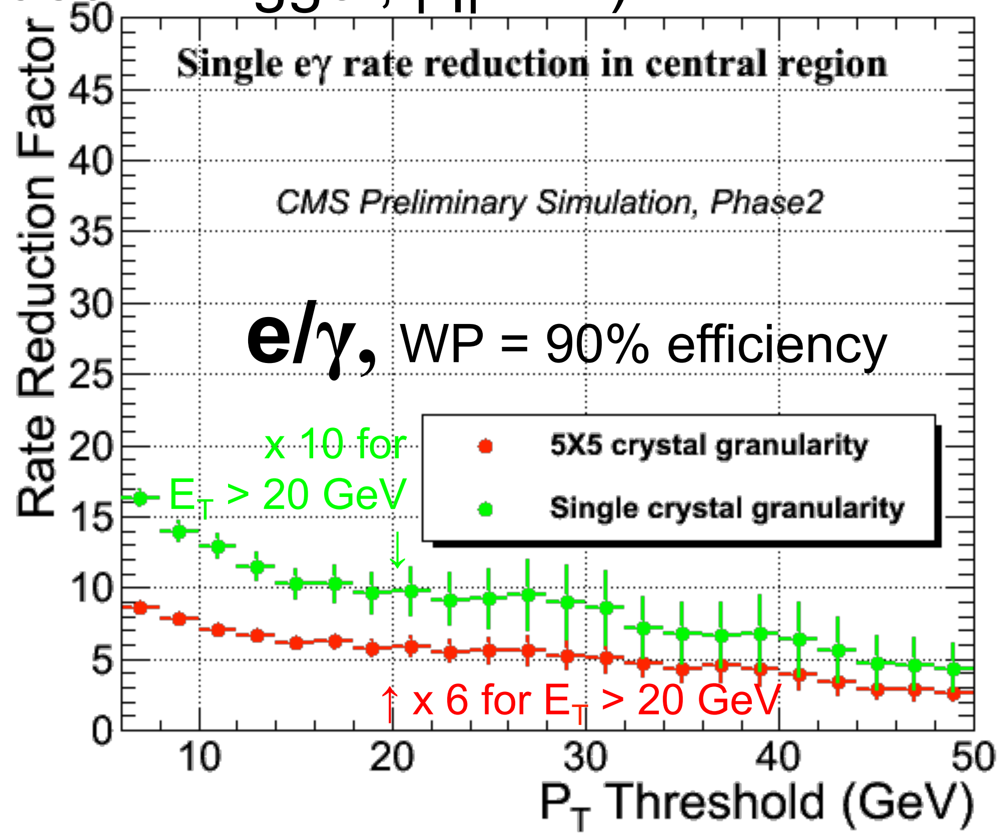
Preliminary simulation studies demonstrate addition of L1 tracking trigger provides significant gains in rate reduction with good efficiency for physics objects. Note these results are "work in progress".

Trigger, Threshold	Algorithm	Rate reduction	Full eff. at the plateau	Comments
Single Muon, 20 GeV	Improved Pt, via track matching	~ 13 ($\|\eta\| < 1$)	~ 90 %	Tracker isolation may help further.
Single Electron, 20 GeV	Match with cluster	> 6 (current granularity) >10 (crystal granularity) ($\|\eta\| < 1$)	90 %	Tracker isolation can bring an additional factor of up to 2.
Single Tau, 40 GeV	CaloTau – track matching + tracker isolation	O(5)	O(50 %) (for 3-prong decays)	
Single Photon, 20 GeV	Tracker isolation	40 %	90 %	Probably hard to do much better.
Multi-jets, HT	Require that jets come from the same vertex			Performances depend a lot on the trigger & threshold.

CMS Gains for μ, e Triggers

(over Phase 1 Trigger, $|\eta| < 1$)





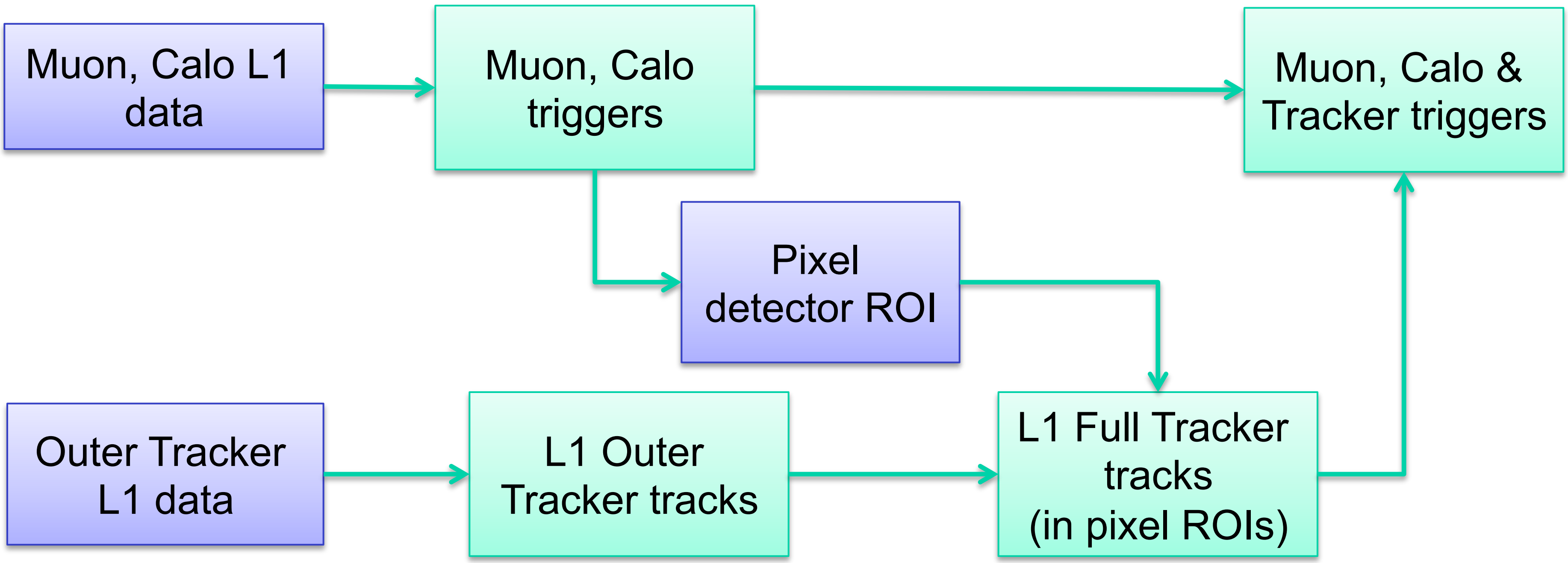
Matching Drift Tube trigger primitives with L1Tracks: **large rate reduction:**
> 10 at threshold > ~ 14 GeV.
Normalized to present trigger at 10 GeV. Removes flattening at high P_t

Rate reduction brought by matching L1 e/γ to L1Track stubs for $|\eta| < 1$.
Red: with current (5x5 xtal) L1Cal granularity.
Green : using single crystal-level position resolution improves matching

CMS Phase 2 pixel trigger?

Needs a trigger itself

- **Local data reduction is not viable below 20 cm**
- **Regional readout probably needed (e.g. Region of Interest)**
- **Pixel data already being read at 750 kHz**



Would provide precise PV determination @ Level-1

- **From < 1 mm with outer tracker to < 100 μm with pixels**
  - Question of Latency under discussion

CMS HL-LHC L1 Trigger Upgrade

Integration of Track & Pixel (option) information into L1 Trigger requires upgrade of rest of L1 Trigger

- **Calorimeter trigger should use full information to provide smallest resolution for combination with a tracking trigger**
  - Resolution based on calorimeter readout cells (e.g. barrel xtals).
  - Also improves calorimeter trigger pattern recognition (e.g. isol.)
  - Increases input data but can mitigate by compressed input scale, EM pre-clustering, taking advantage of newer technology higher speed links (presently 13 Gbps, guess at least ×2 for 2023)
- **Muon Triggers will need to calculate results on a finer scale for combination with a tracking trigger**
- **Muon triggers may integrate track trigger information into muon track-finders**
- **Global Trigger will be processing coincidences on a finer resolution**

CMS HL-LHC L1 Trig. Latency, Rate

Extended Latency: Simplifies tracking trigger

- **Timing is tight for tracking trigger**
  - Including processing & use of track trigger information
- **Makes design of tracking trigger easier**
  - Relaxed constraints: reduces power, transmission bandwidth…

Extended Latency: Provides option of pixel tracking trigger

- **Pixel trigger requires "pull" architecture**
- **Required for b-tags in L1 Trigger**
  - Along with 750 kHz L1 bandwidth

Higher Rate: Reduces Thresholds for physics signals

- **Can set thresholds comparable to present ones when coupled with tracking triggers**

Higher Rate: Needed for Hadronic Triggers

- **Track Trigger helps leptonic triggers**
- **Less of an impact on hadronic triggers**
  - Vertex for jets

Higher Rate: Needed for b-tags

- **Pixel trigger may not reduce rate sufficiently**

CMS HL-LHC HLT Output Rate

Processing 500 kHz (140 PU), 750 kHz (200 PU) Input

- DAQ hardware & HLT processing compatible with Moore's Law scaling until 2023 & estimated x4 longer reconstruction time, event size for PU ≥ 140 (must cope with peak luminosity)
  - Prediction of HLT CPU time/event = 600 ms at PU=125 (200 now)
    - Issue of complexity of events passing L1 w/tracking trigger
- Use of L1 Track Trigger information as input allows immediate, fast use of tracking information.
- Possibility to share resources with Tier-0 (Cloud computing)
  - Goes both ways
- If need more CPU, we can bring more online rapidly (if can afford)

5 kHz (140 PU), 7.5 kHz (200 PU) Output Rate

- .5/.75 MHz L1 Accept Rate → 5/7.5 kHz HLT output rate keeps same reduction of L1 rate (x100) as present HLT design (100 kHz → 1 kHz)
- Output to Computing
  - Compatible with Moore's Law scaling (with SW work) until 2023 & estimated X3 longer reconstruction time, event size (avg'd over year)

CMS DAQ after LS3

	LHC run 1	LHC Phase-I upgr.	HL-LHC Phase-II upgr.	
Energy	7-8 TeV	13 TeV	13 TeV	
Peak Pile Up (Av./crossing)	35	50	140	200
Level-1 accept rate (maximum)	100 kHz	100 kHz	500 kHz	750 kHz
Event size (design value)	1 MB	1.5 MB	4.5 MB	4.5 MB
HLT accept rate	1 kHz	1 kHz	5 kHz	7.5 kHz
HLT computing power	0.2 MHS06	0.4 MHS06	6 MHS06	13 MHS06
Storage throughput (design value)	2 GB/s	3 GB/s	27 GB/s	38 GB/s

Remarks

- **750 kHz L1 rate**
  - allows for flexible physics trigger
  - Feasible for front end electronics
- **Event Size 4.5 MB**
  - Estimated from linear pile-up extrapolation to PU=140
    - **Need simulation work to back up this assumption**
- **HLT accept rate:**
  - Requires factor 100 suppression in HLT as today
- **Computing power: next slides**

CMS Estimation of required HLT CPU power

Observation so far

- **Required HLT power scales linearly with pile-up**
  - This has been observed for PU in the range of 10-40
    - **Conservatively assume this continues – needs verification**

Assuming

- **Linear scaling with average PU up to 140 - 200**
- **A factor 1.5 due to energy increase to 13 TeV**
  - Also conservative – takes into account complexity of events selected by L1 Trigger scaling with energy
  - Operation after LS1 with 6.5 TeV per beam will quickly allow refining this estimate
- **5 – 7.5 times higher L1 rate**

A total factor of 50 increase of HLT power would be needed wrt. today's farm.

- **This results in 10 M HEP-SPEC-06**

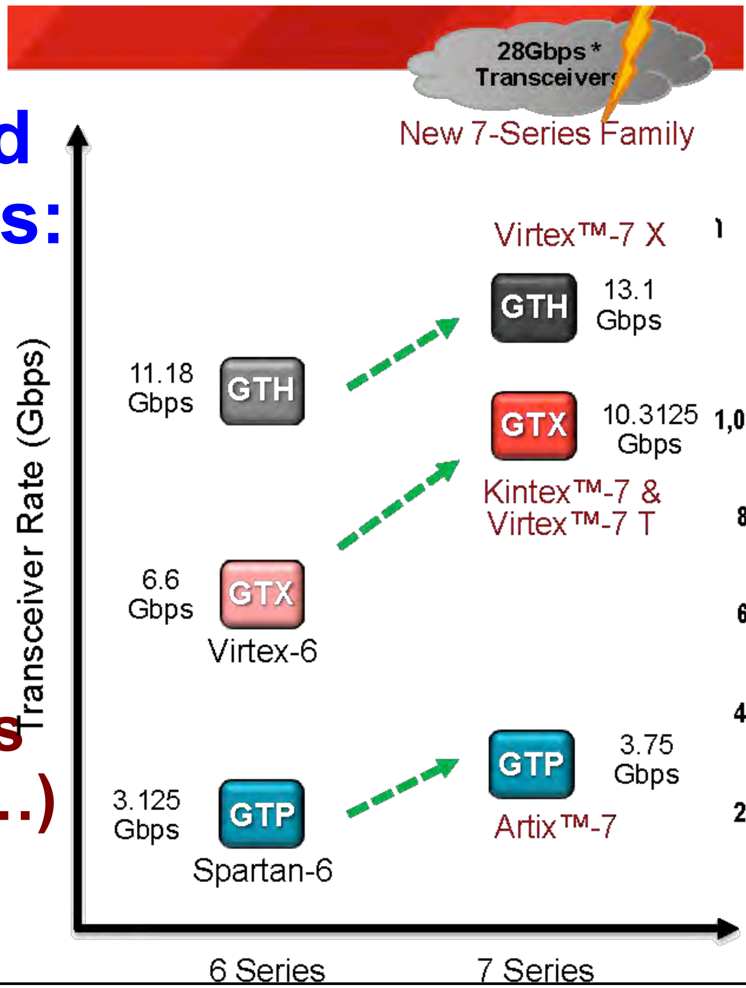
Tools for Triggers: FPGAs

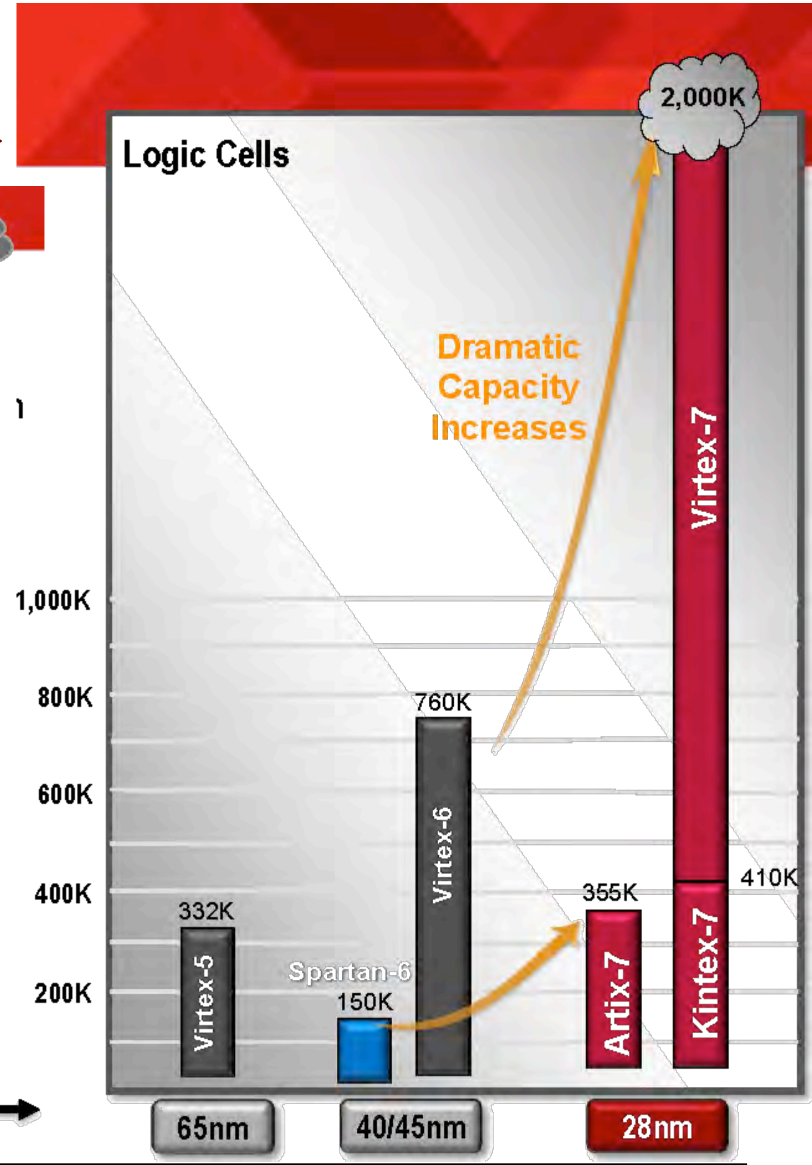
Logic Cells

- 28 nm: > 2X gains over 40 nm→

On-Chip High Speed Serial Links:

- Connect to new compact high density optical connectors (SNAP-12…)





FPGA Challenges/Opportunities

Latest generation FPGAs create complex placement issues that are difficult for Xilinx tool algorithms to resolve

- **Build times getting in excess of 24 hours**
- **Need to perform smart explorer builds to achieve timing closure**
- **Can use batch systems (e.g. Condor) to perform multiple builds in parallel**

Designs must be heavily floor-planned

- **Similar to ASIC layout process**
- **Needs detailed knowledge of routing structure & alternative Xilinx tool flows**

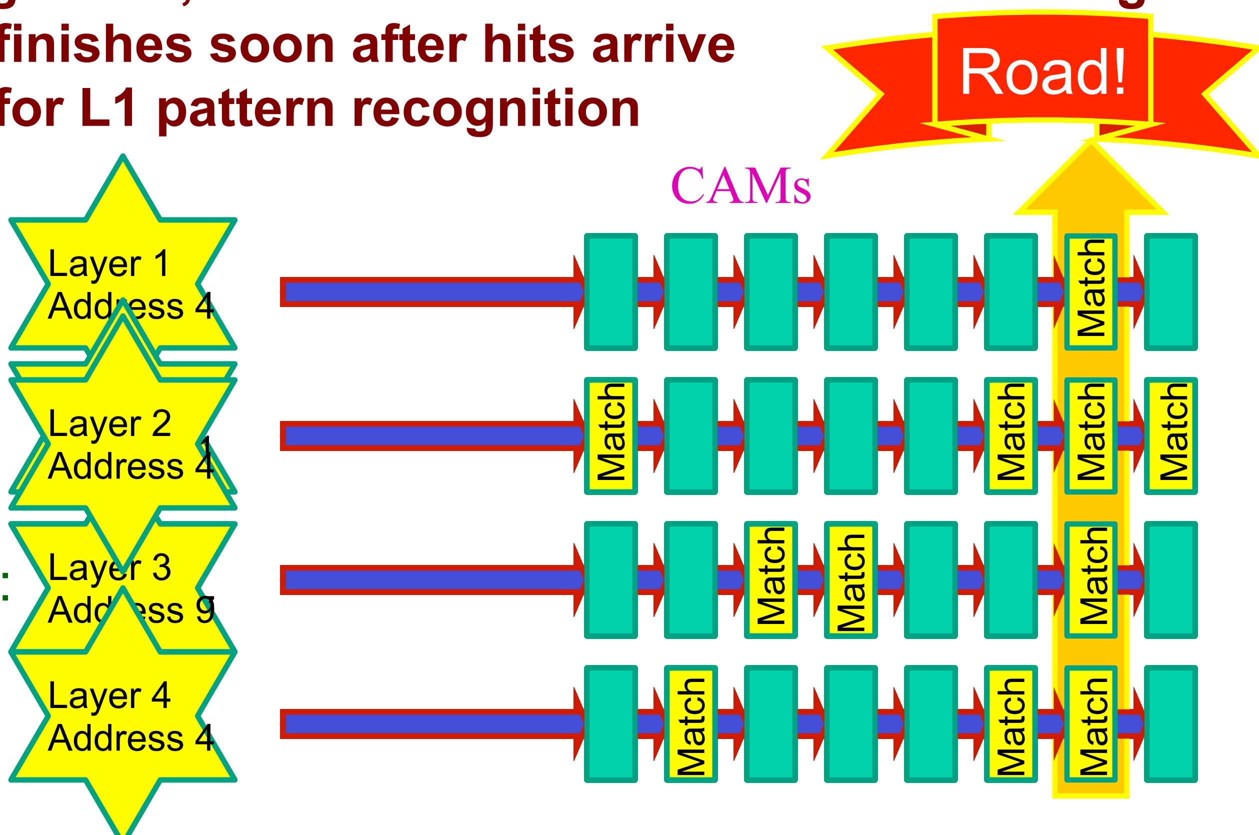
Embedded Processors

- **Move many tasks from FPGA design to SW design**
- **Shortens design cycle**
- **Remove FPGA design integration burden for commodity interface cores**
  - Utilize proven and FREE embedded system IP
- **Interfaces more flexible under software control**
  - Conform to industry standards at core
  - Add software application above core to specialize
- **Ensures FPGA design focus on custom logic**
  - Custom high speed communication interfaces and custom physics algorithms
- **Example: Xilinx ZYNQ**
  - Runs PetaLinux (also runs on Microblaze on Xilinx V6 & V7)
  - Write Communications and Control functions in Linux

Tool for Tracking Triggers: Associative Memories

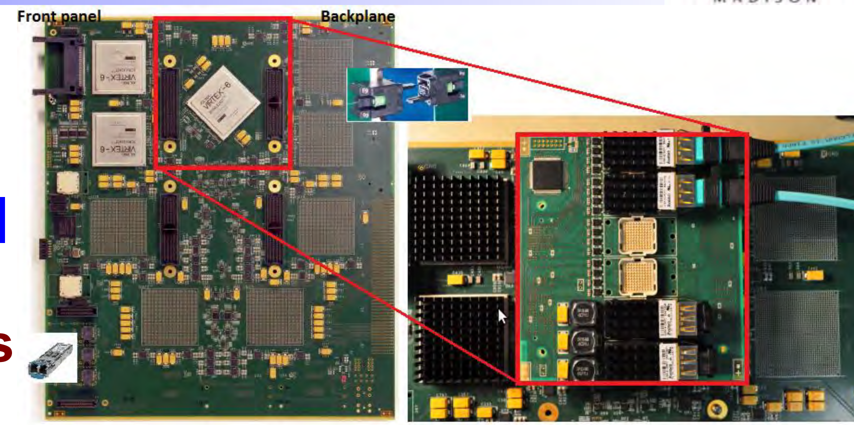
Pattern Recognition Associative Memory (PRAM)

- **Based on CAM cells to match and majority logic to associate hits in different detector layers to a set of pre-determined hit patterns**
  - e.g. ATLAS FTK Level 2 Trigger for Phase 1, installed 2015-16
- **highly flexible/configurable, much less demand on detector design**
- **Pattern recognition finishes soon after hits arrive**
- **Potential candidate for L1 pattern recognition**
- **However: Latency**
- **Challenges:**
  - Increase pattern density by 2 orders of magnitude
  - Increase speed x 3
  - Same Power
  - Use 3D architecture: Vertically Integrated Pattern Recognition AM - VIPRAM

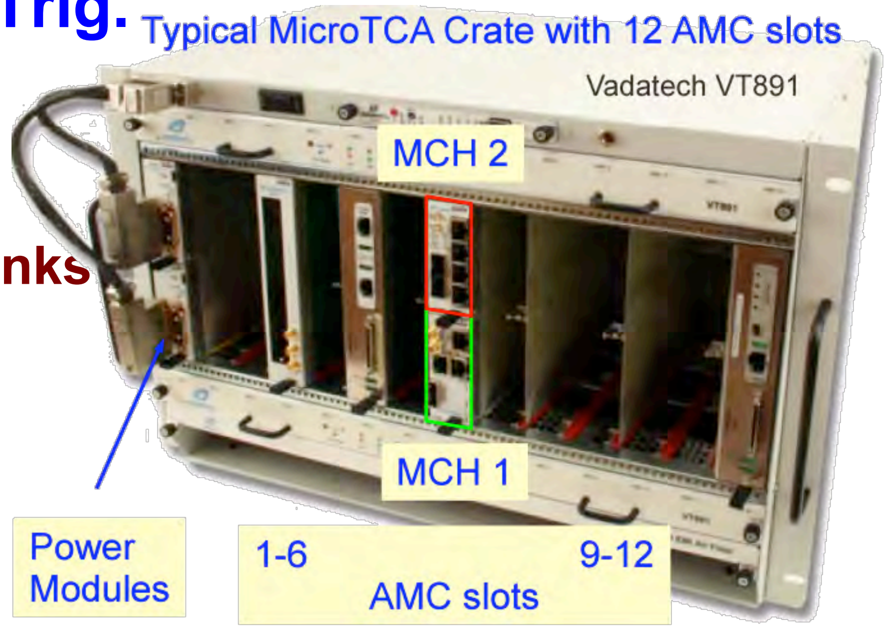


Tools for Trigger/DAQ: xTCA

- **Advanced Telecommunications Computing Architecture ATCA**
- **Example: ATLAS Upgrade Calorimeter Trigger Topological Processor Card**
  - **12-chan. ribbon fiber optic modules**
  - **Backpl. opt. ribbon fiber connector**



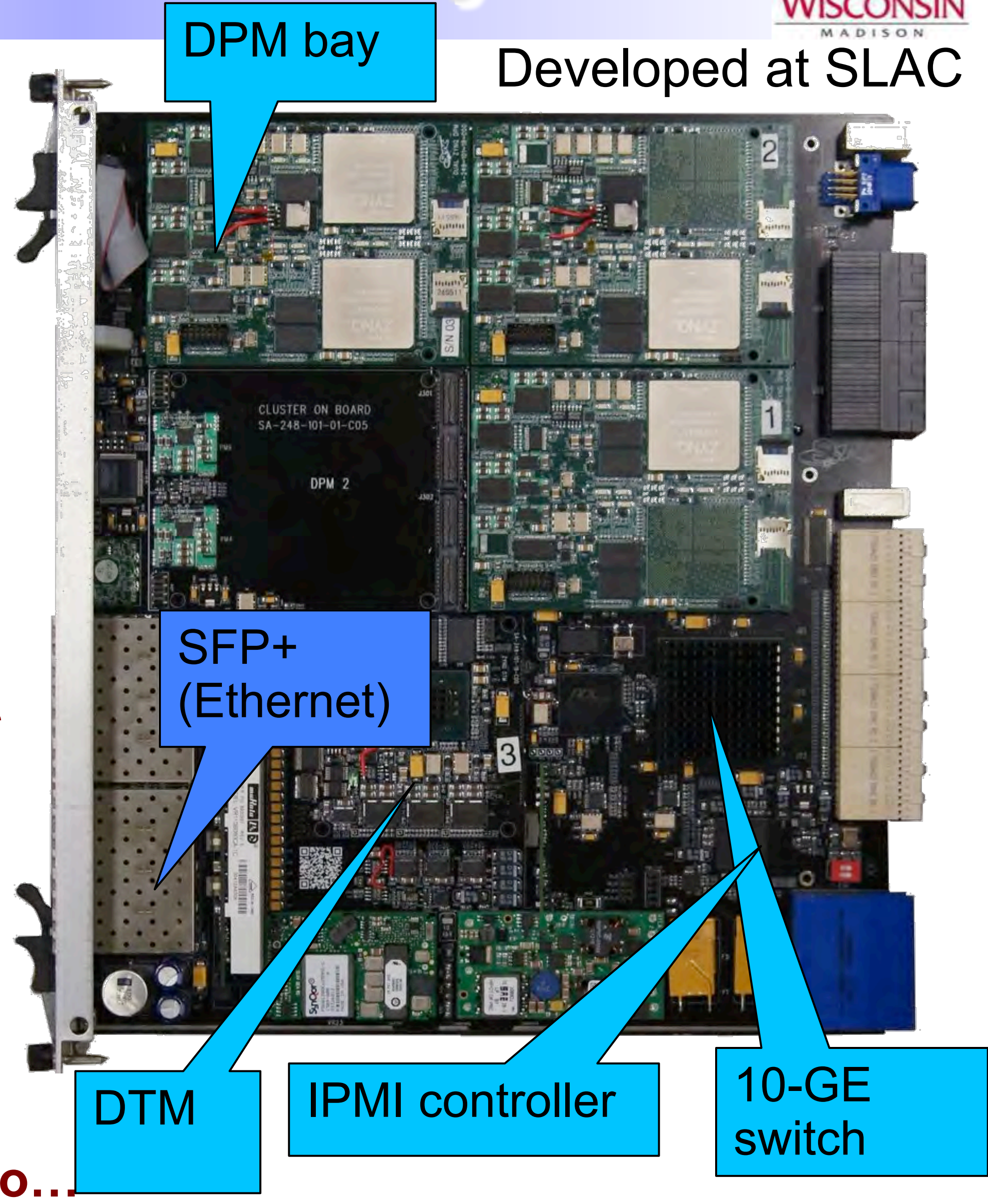
- **Example: μTCA derived from AMC std. used by CMS HCAL, Trig.**
  - **Advanced Mezzanine Card**
  - **Up to 12 AMC slots**
    - *Processing modules*
  - **6 standard 10Gb/s point-to -point links slot to hub slots (more available)**
  - **Redundant power, controls,clocks**
  - **Each AMC can have in principle (20) 10 Gb/sec ports**
  - **Backplane customization is routine & inexpensive**



ATCA Example: RCE System

Developed at SLAC

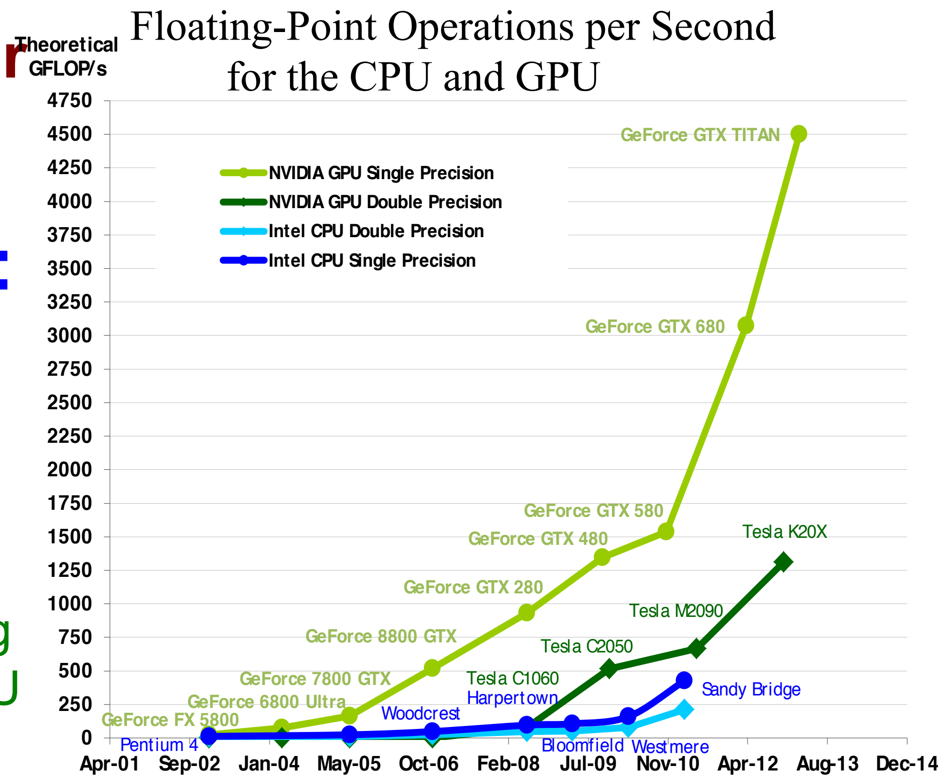
- Integrated hardware + software entity where generic core firmware & software infrastructure are common & provided.
- ATCA infrastructure used
- Xilinx ZYNQ series with ARM processors that can run either RTEMS or LINUX.
- Has three principal components:
  - <u>Programmable</u> FPGA *Fabric*
  - <u>Programmable</u> *Cluster-Element* (CE).
  - *Plugins*
- Currently being used in:
  - ATLAS CSC (proposed: Small Wheel), DArkside, Heavy Photon Search, LBNE, LSST, LCLS, nEXo…



Tools cont'd: CPU, GPU, PCIe

CPU Gains for High Level Triggers: Moore's Law

- **e.g. Xeon Phi Co-processor**
  - 1.2 TeraFlop/s double precision peak performance today



GPU Enhancement of HLT:

- GPU uses a highly scalable architecture that closely tracks Moore's Law
- High performance memory system with ≥ 5x bandwidth vs. CPU
- Better performance / Watt vs. CPU
- Hardware and software support for moving data directly from network interface to GPU memory

Enhancement of detector to DAQ readout:

- **PCI Express Gen3 Cards now available**
- **Up to 56Gb/s InfiniBand or 40 Gigabit Ethernet per port**

Conclusions for Phase 2 Trigger

ATLAS & CMS L1 Trigger Scenario:

- ATLAS: L0 ≤ 1 MHz, L1 ≤ 400 kHz
- CMS: L1 ≤ 500 (750 kHz) @ 140 (200) PU
- L1 Track Trigger

ATLAS & CMS Phase 2 DAQ

- HLT design to accept < 1 MHz of 5 MB events w/PU < 200
- Output of < 10 kHz.

Increasing L1 Accept rate and using a L1 Track Trigger provide the path for maximally exploiting the physics potential of the HL-LHC

Tools to implement Phase 2 Triggers are available

- Considerable R&D will be required to incorporate them

Backup

Where CMS starts – Phase 1
(from CMS Phase 1 Upgrade Trigger TDR)

CMS Level-1 Menu using the current L1 system and upgraded system.

The beam conditions are:

$$\sqrt{s} = 14TeV$$

$$L = 2.2 \times 10^{34} cm^{-2} s^{-1}$$

with a bunch spacing at 25ns and pile-up of 50.

	Current Level-1 $L = 2.2 \times 10^{34}$ cm^{-2}s^{-1}			Upgraded Level-1 $L = 2.2 \times 10^{34}$ cm^{-2}s^{-1}		
Trigger Algorithm	Rate [kHz]	95% Threshold [GeV]	Plateau Efficiency	Rate [kHz]	95% Threshold [GeV]	Plateau Efficiency
Single e/γ	10	67	1.0	11	57	1.0
Single iso e/γ	9.4	52	0.9	15	31	0.90
Single Mu	11	42	0.95	14	22	0.90
Single iso Mu	NA	NA	NA	15	19	0.82
Single Tau	NA	NA	NA	12	100	0.95
Single iso Tau	9.2	72	0.3	13	83	0.7
iso e/γ + e/γ	16	26 16	0.9	12	23 16	0.9
(iso)Mu + Mu	7.4	20 12	0.9	9.4	15 10	0.8
(iso)Tau + Tau	8.2	36 36	0.1	7.2	64 62	0.67
iso e/γ + Mu	6.2	24 12	0.85	11	21 10	0.85
(iso)Mu + e/γ	5.0	20 15	0.95	8.3	18 15	0.83
iso e/γ + Tau	NA	NA	NA	8.3	21 57	0.86
isoMu + Tau	NA	NA	NA	5.8	14 47	0.8
Single Jet	5.4	205	1.0	5.9	205	1.0
Double Jet	5.8	170 170	1.0	4.2	130 130	1.0
Quad Jet	4.8	4@96	1.0	5.0	4@55	1.0
Single iso e/γ + Jet	8.5	38 82	0.9	11	27 78	0.90
Single Mu + Jet	7.5	27 54	0.95	9.7	18 52	0.93
Single iso e/γ + H_T^{miss}	8.2	38 120	0.9	12	27 110	0.90
Single Mu + H_T^{miss}	9.8	20 93	0.95	11	18 86	0.93
H_T	5.4	580	1.0	3.0	380	1.0
Total Rate	92			95		

Starting Point – Phase 1 Upgrade
(CMS Trigger Phase 1 Upgrade TDR Design)

Process (x2 improvement highlighted)	1.1×10^{34} cm^{-2} s^{-1}		2.2×10^{34} cm^{-2} s^{-1}	
	2012	Upgrade	2012	Upgrade
W(eν),H(bb)	57.7%	87.0%	37.5%	71.5%
W(μν),H(bb)	95.9%	100%	69.6%	97.9%
VBF H(ττ(μτ))	42.6%	51.3%	19.4%	48.4%
VBF H(ττ(ετ))	24.4%	44.3%	14.0%	39.0%
VBF H(ττ(ττ))	17.2%	53.7%	14.9%	50.1%
H(WW(eeνν))	91.4%	97.8%	74.2%	95.3%
H(WW(μμνν))	99.9%	99.9%	89.3%	99.9%
H(WW(eμνν))	97.6%	99.4%	86.9%	99.3%
H(WW(μeνν))	99.6%	99.5%	90.7%	99.7%
Stop→bWχ→e, jets (600 – 450 GeV)	55.8%	68.2%	50.3%	64.8%
Stop→bWχ→μ, jets (600 – 450 GeV)	78.1%	81.6%	76.4%	84.5%
RPV Stop→jets (200 GeV)	70.1%	99.9%	43.6%	99.9%
RPV Stop→jets (300 GeV)	93.7%	99.9%	79.7%	99.9%

Average Improvement: 17% (Low Lumi) & 40% (High Lumi)