Wideband Feedback Technology Development Status

John Dusatko / SLAC

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Introduction

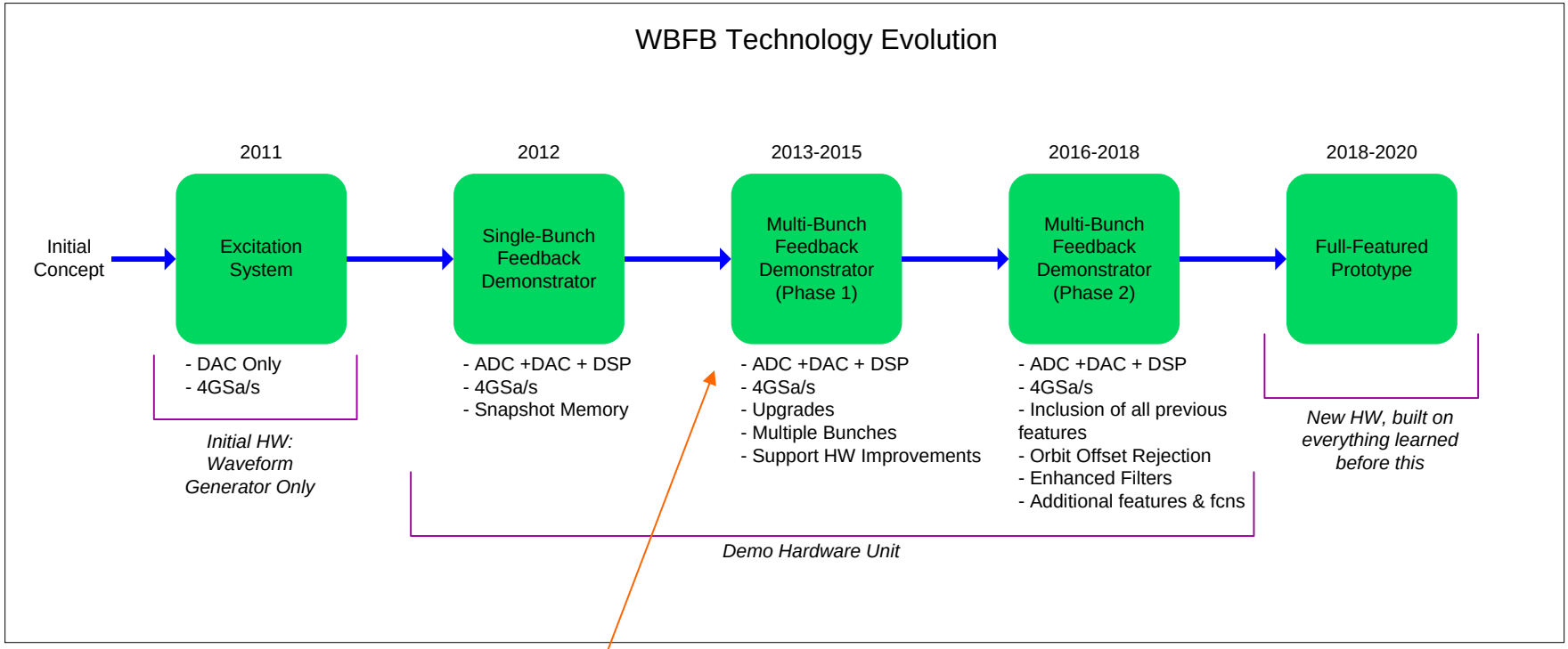
The Feedback Demonstrator System:

- It is a very high-speed flexible signal processing platform developed for transverse feedback control studies at the SPS.
- It measures the motion of protons within the 2ns to 4ns long bunch (by taking 16 samples spaced 250ps apart), computes a correction for each sample and drives that correction back onto the same bunch at the next turn. The existing diagonal filter algorithm treats each sample as an independent oscillator and computes a correction based on information from the past k turns. The filters are expressed as (x = input sample, h,j = coefficient, y = output):

  Filter algorithms (FIR is used presently, there are 16 filters total, one per sample slice):

  FIR Filter: $y(n) = \sum_{k=0}^{7} h(k)x(n-k)$ *IIR Filter:* $y(n) = \sum_{k=0}^{7} h(k)x(n-k) + \sum_{k=0}^{7} j(k)y(n-k)$

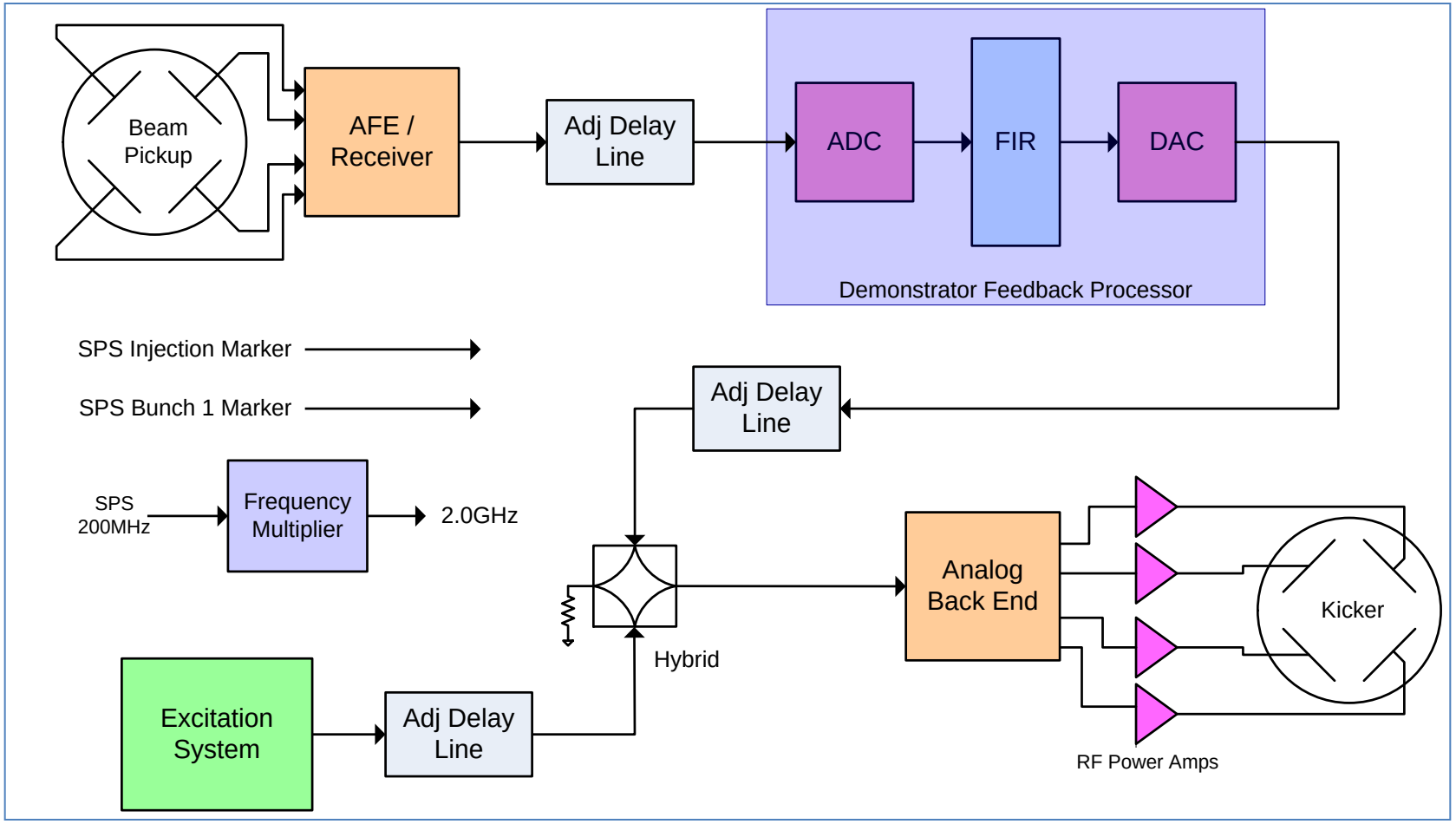
  - Though the concept is straightforward, the implementation is non-trivial due to the sampling and processing speeds involved
- Its modular architecture includes an FPGA-based processing core, an analog receiver, an analog back end, high-speed data converters, RF power amplifiers, and timing support components. The architecture includes diagnostic memories to drive the beam and record the motion for accelerator diagnostics.
- The demo system is an expandable platform whose development and use in machine studies provides a provides a means for exploring technologies, algorithms and control techniques.
- It has successfully demonstrated single-bunch control of Mode 0 instabilities at the SPS, just prior to the start of LS1.



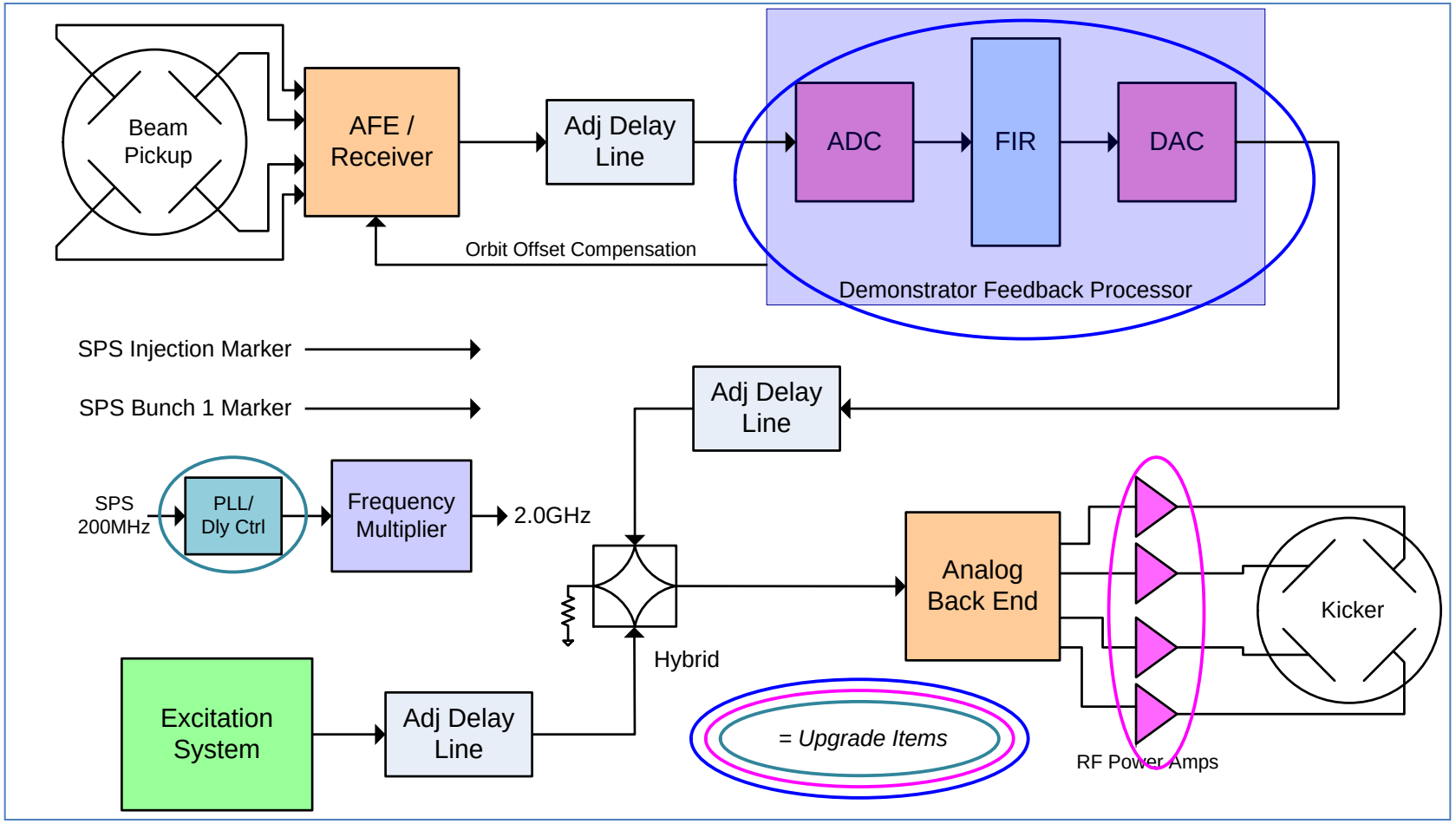
→ We are now in the process of adding functions and features the further expand the not only the demo system but other system hardware:

- Upgrade the Demo Feedback Processor
- Develop timing functions: Synchronization and Energy ramp delay control
- New RF Power Amplifier evaluation/characterization

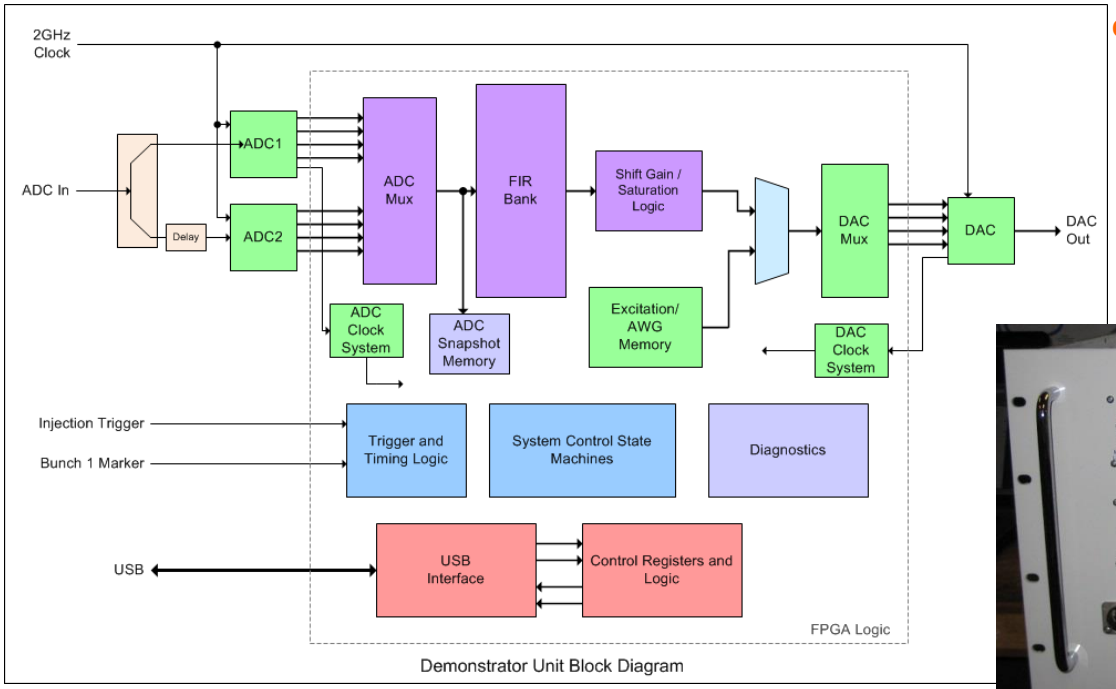
Overall Demo System Diagram



Overall System Diagram - *Upgrades*

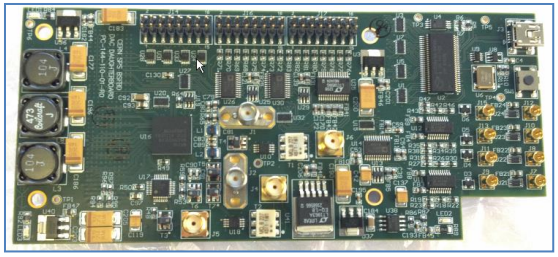


The Demo Feedback Processor



Demonstrator Unit Block Diagram

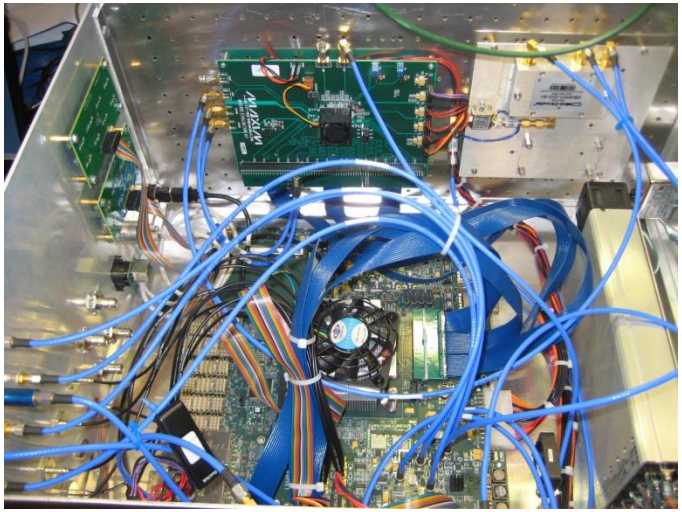
Custom DAC Daughterboard



FB Demo Unit Chassis

Features: **Expandable/Flexible Platform**

- Maxim MAX19693 12-bit 4 GSa/s DAC
- Two Maxim MAX109 2GSa/s 8-bit ADCs interleaved to get 4 GSa/s
- Xilinx Virtex-6 FPGA for all digital signal processing, acquisition, diagnostics & control
- Multi-mode operation: Feedback channel -or- Excitation/AWG
- Timing and Trigger processing
- Diagnostics include:
  - ADC Snapshot memory
  - Trigger rate and missing trigger
  - DSP Saturation Indicator
- USB 2.0 Interface to host
- Suite of Visual Basic & Matlab SW



Demo Chassis internal view

Development Plans

→ With the initial success of the single-bunch demonstrator, we proceeding with the following upgrades, enhancements and improvements for MD studies, which all work towards defining the final architecture:

- To Do Right Now:
  - **System Improvements / ADC Front End**: Small changes & mods / Improve system noise floor (SW/GW/HW work) (Fall 2014)
  - **Multi-Bunch Control**: Preliminary design studies suggest that the demonstrator platform can be expanded to serve at least 16 bunches / Ultimate limitation is FPGA internal resources (FPGA + SW work) (Fall 2014)
  - **Excite/Record Mode**: Add the ability to record into Snapshot memory while playing out an excitation sequence (FPGA + SW work) (Fall 2014…Winter 2015)
  - **DAC Clock Synchronization**: New Phase Locked Loop (PLL) developed for improved synchronization of DAC sample clock to SPS RF clock (HW work) (Fall 2014)
  - **SPS RF Clock Synchronization Improvements**: RF Clock synchronization to master oscillator (HW work in collaboration with CERN) (Fall 2014)
- Future/Ongoing Work:
  - **Orbit Offset Rejection**: Bunch-by-bunch orbit offset rejection via use of common mode range of ADC. Adds two bits of dynamic range to the front end (HW + FPGA + SW work) (Winter 2015…Fall 2015)
  - **Advanced Filter Structures**: Inclusion of cross-terms, IIR Structures, etc. as indicated by control and system dynamics studies (FPGA + SW work) (Winter 2015…2017)
  - **New RF Power Amplifiers**: Higher Power, better time-domain and phase response to support new 1GHz BW kickers (2014…2017)
  - **8GSa/s Architecture**: Defining delta-sigma topology, evaluating components (2014…2017)
  - **Additional Features & Upgrades:** Many items, longer term (2014…2017)

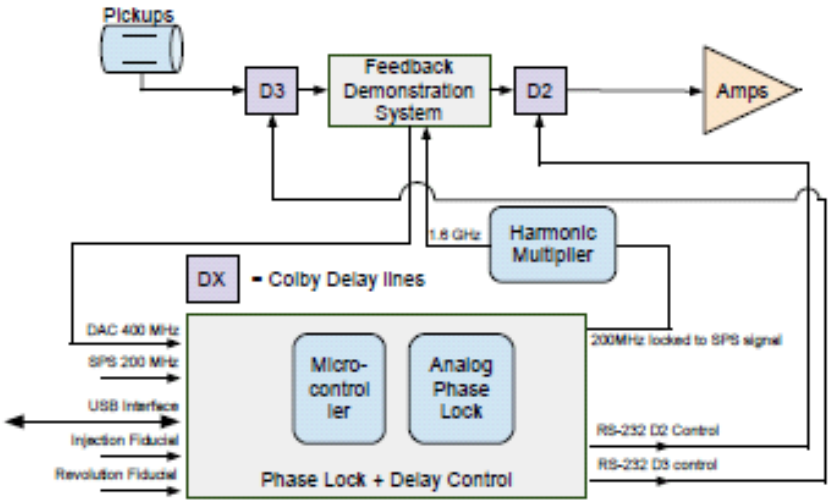
PLL/Delay Controller Development

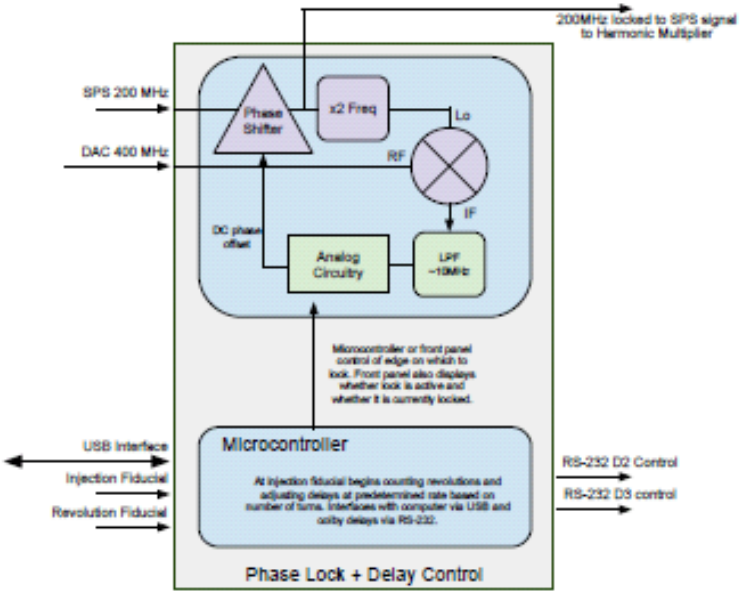
- A system clock phase locked loop and automatic delay controller has been under development. These are two distinct timing functions implemented in the same box:

  1) The PLL will lock to the SPS 200MHz RF Clock and provide a deterministic Sample Clock phase for the DAC

  2) The Delay control will automatically adjust the passive delay lines for computer-based timing & setup to make MDs faster & more efficient / development is in its preliminary stages

- **Status**: PLL board is completed, undergoing testing and the chassis is being assembled / Delay controller need further design

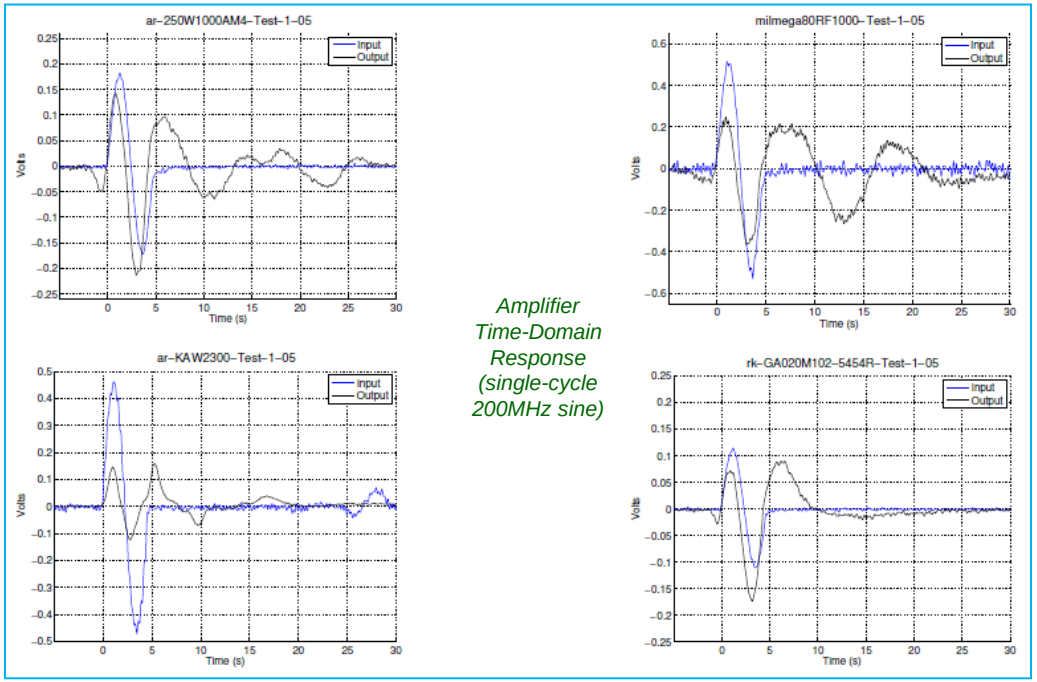




RF Power Amplifier Evaluation

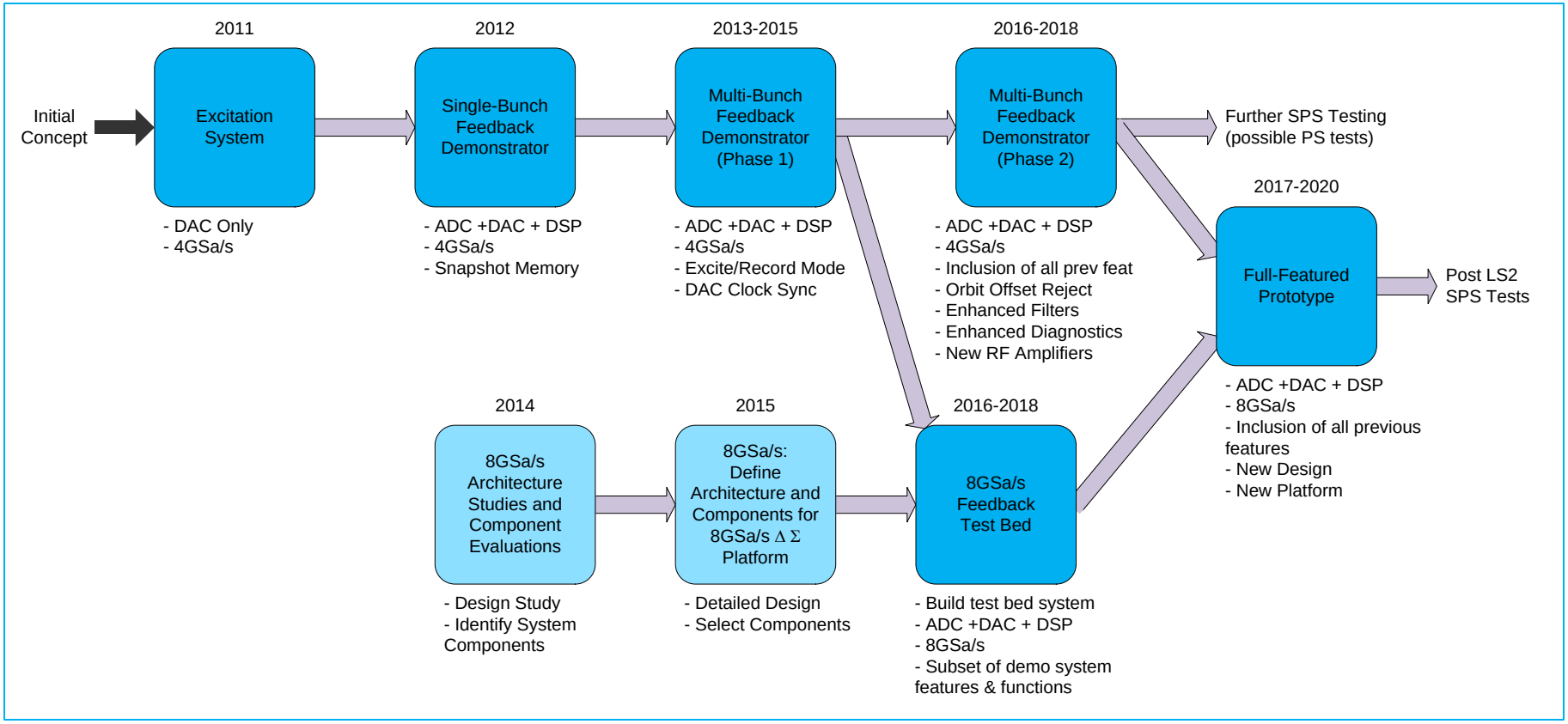
→ The RF Power amplifiers are a key ingredient in the system: we need clean RF power to drive the Kicker and hence, the beam

- The existing RF power amplifiers exhibit non-optimal time-domain behavior / differ widely in power response on a unit-to-unit basis
- The challenge: most amplifier manufacturers design (and only test in this space) for CW operation, we require pulsed mode operation
- We needed to evaluate a variety of amplifiers to determine their characteristics and see if they meet our requirements:
  - Developed set of standard tools for amplifier characterization
  - Tests were done in the time & frequency domains
- Four different amplifier units were evaluated:
  - MilMega 80RF1000-250
  - Amplifier Research KAW-2300 (modified)
  - R&K GA020M102-5454R
  - Amplifier Research 250W1000AM4
- **Status**: Proceeding with further evaluations and working with mfgr who is modifying one of their products for us.



Amplifier Time-Domain Response (single-cycle 200MHz sine)

WBFB Hardware Development Roadmap



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