Geant4 Version 10 Status and outlook

A. Dotti for the Geant4 collaboration HEP/ASCR Meeting; 5th February 2014







Introduction



- Event level parallelism via multi-threading (POSIX based)
- Built on top of experience of G4MT prototypes
- Main design driving goal: minimize user-code changes
- Integrated into Version 10.0 codebase
 - MT code integrated into
 G4

- Public release
- All functionalities ported to MT



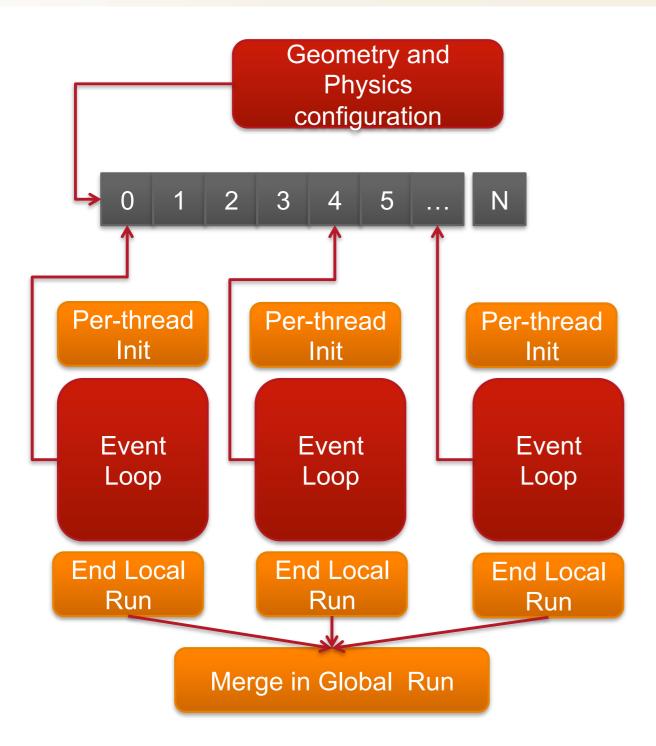
- Proof of principle
- Identify objects to be shared
- First testing

- API re-design
- Example migration
- Further testing
- First optimizations

- Further Refinements
- Focus on further performance improvements

Multi-threading master/worker model





Per-event RNS seeds pre-prepared: guarantees reproducibility

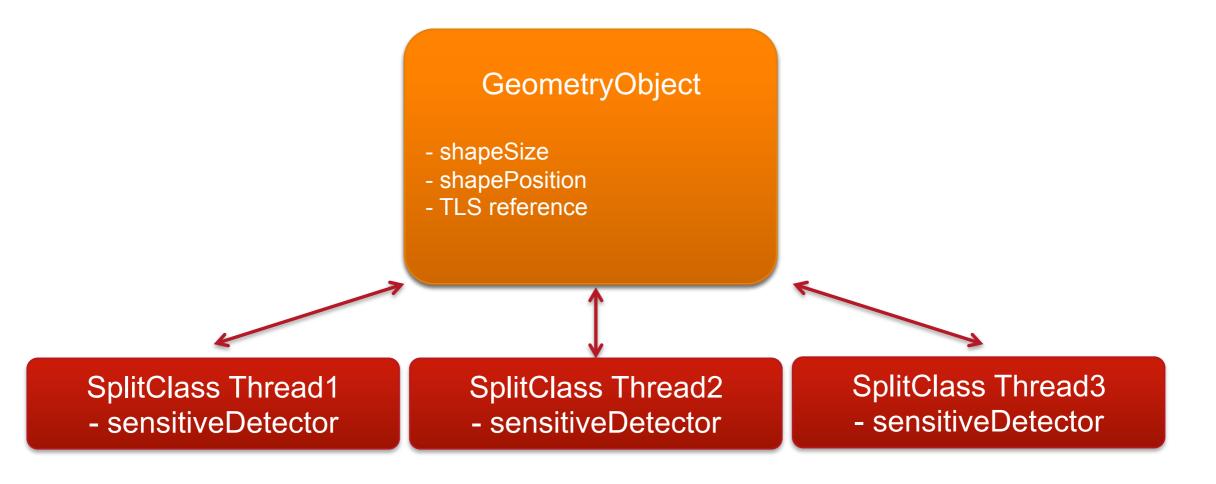
Threads compete for next "bunch" of events. Optimal bunch size is a parameter to minimize locking

Command line scoring and G4 histo tools automatically perform reductions at the end of the job.

Thread-safety in Version 10.0



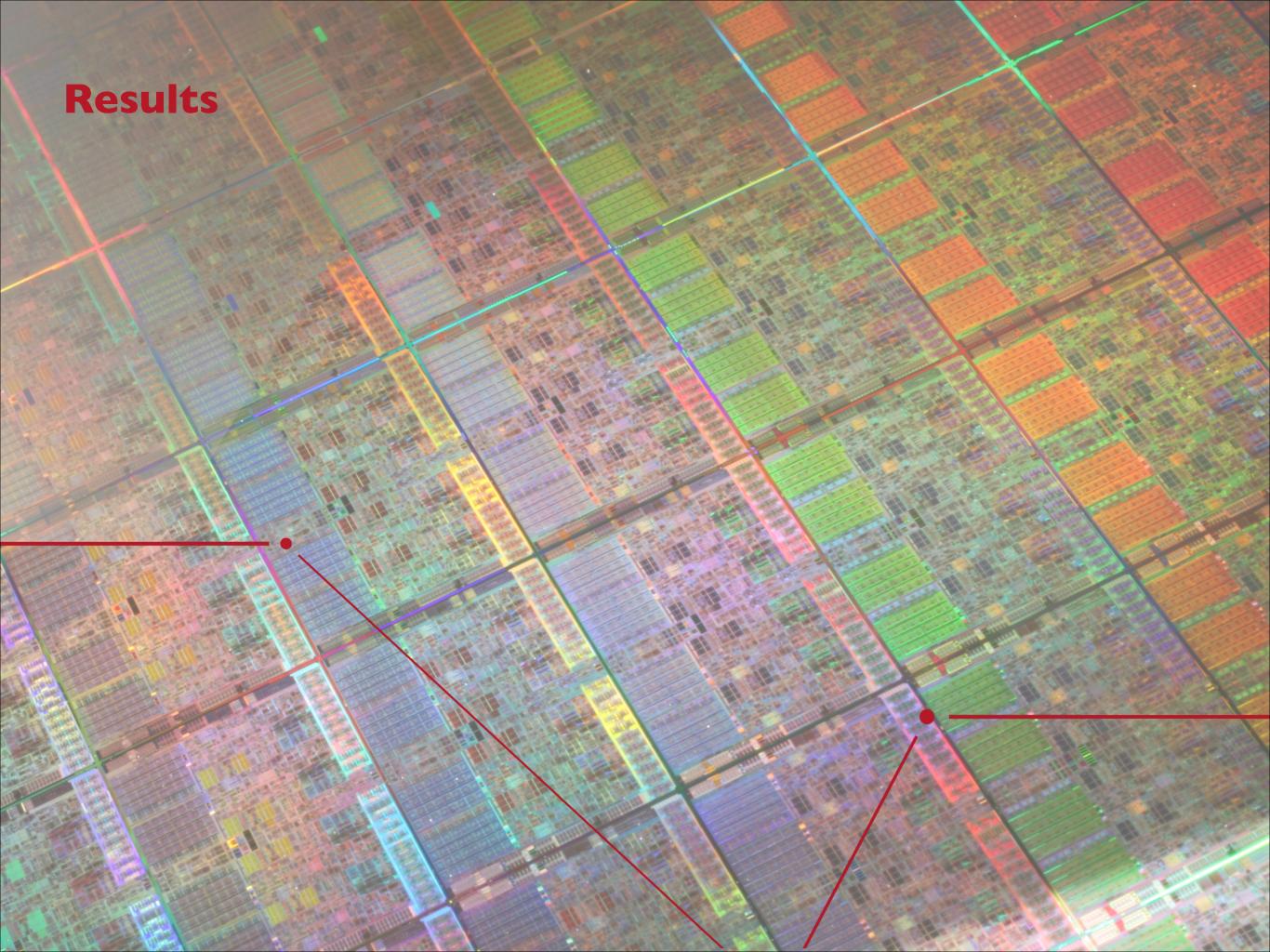
- Design: lock-free code during event-loop
- Thread-safety implemented via Thread Local Storage
- "Split-class" mechanism: reduce memory consumption
 - Read-only part of most memory consuming objects shared between thread: geometry, (EM) physics tables
 - Rest is thread-private



User-feedback



- Very strong interest from user community: 30 threads in new dedicated user-forum (not only HEP)
- CMS: interest in integration with TBB-based experimental framework. First simple TBB-based example provided (examples/ extended/parallel/TBB)
- ATLAS: interest in evaluation MT in ISF (Integrated Simulation Framework) **mixing different flavors of simulation** (e.g. fast and full) and possibly in parallel
- ALICE: strong interest running in MT already during this year
- Uni Manchester: use of G4 on Xeon Phi for imaging and treatment planning



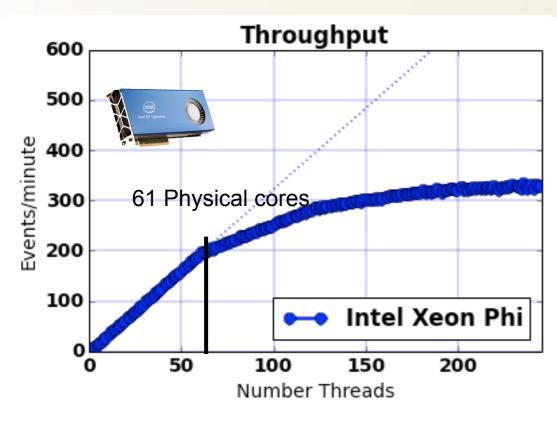
General considerations

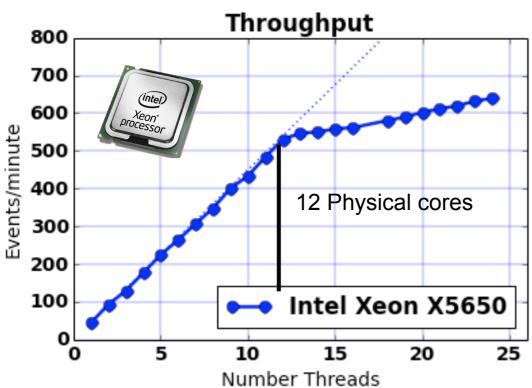


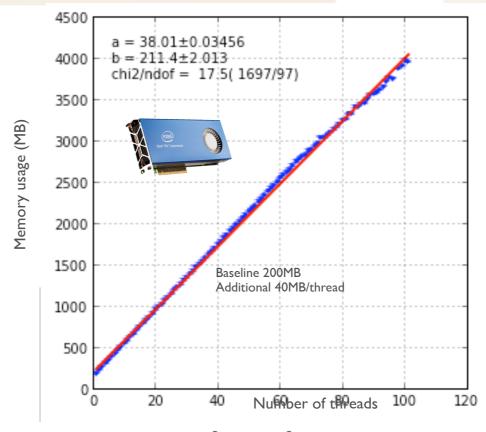
- Fully reproducible: given an event and its initial seed the RNG history is independent of the number of threads and order in which these are simulated
 - Corollary 1: given the seeds, sequential and MT builds are equivalent
 - Corollary 2: being able to reproduce a single event in a dedicated job (i.e. crashes)
- MT functionality introduces minimal overhead (~1%) w.r.t. sequential
- Very good linear speedup up to very large number of threads O(100)
- Good memory reduction: only 30-50MB/thread (depends on application)
- Hyper-threading adds additional +20% throughput
- Working out-of-the-box with success on **different architectures** ×86,

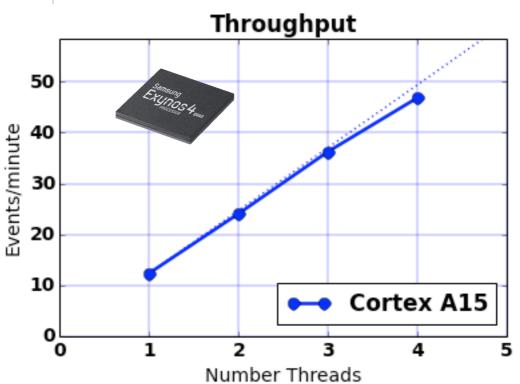
Results

SLAC



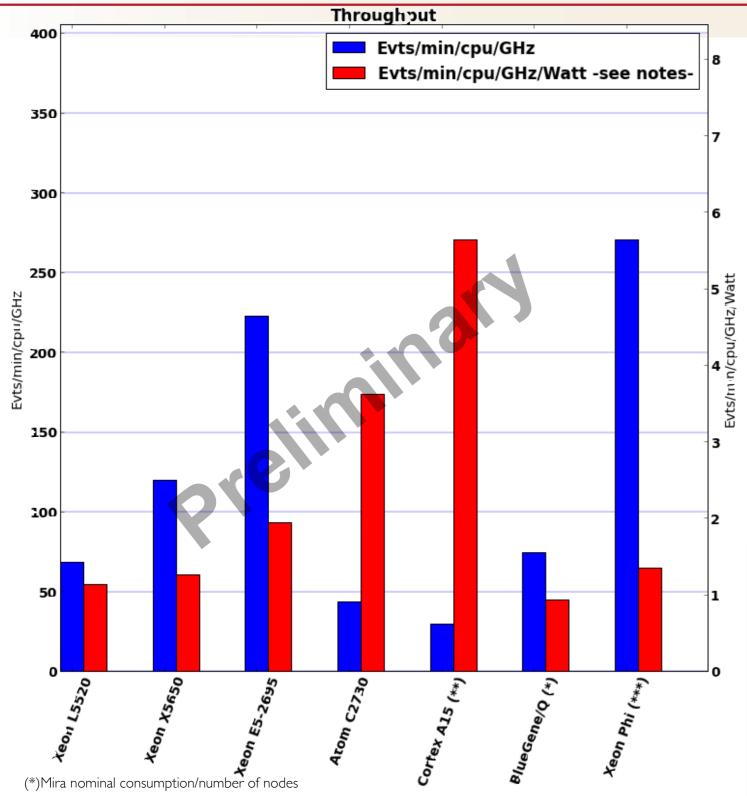






Cross-comparing architectures





- Throughput normalized per GHz and "socket" (or node / card)
- Not a measure of the absolute performance of a system
- Also reported Throughput/Watt: not realistic (mainly not counting server, very rough!) only to give an idea of what we are talking about
- What is the best "metrics" to compare different architectures?

Absolute performances:

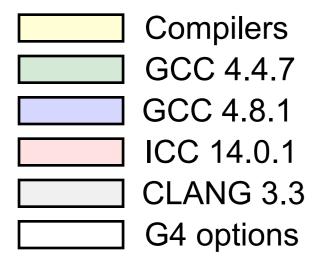
(**) Measured for a ODROID-XU+E evaluation board

(***) Power consumption measured via "Intel Xeon Phi Coprocessor Status Panel"

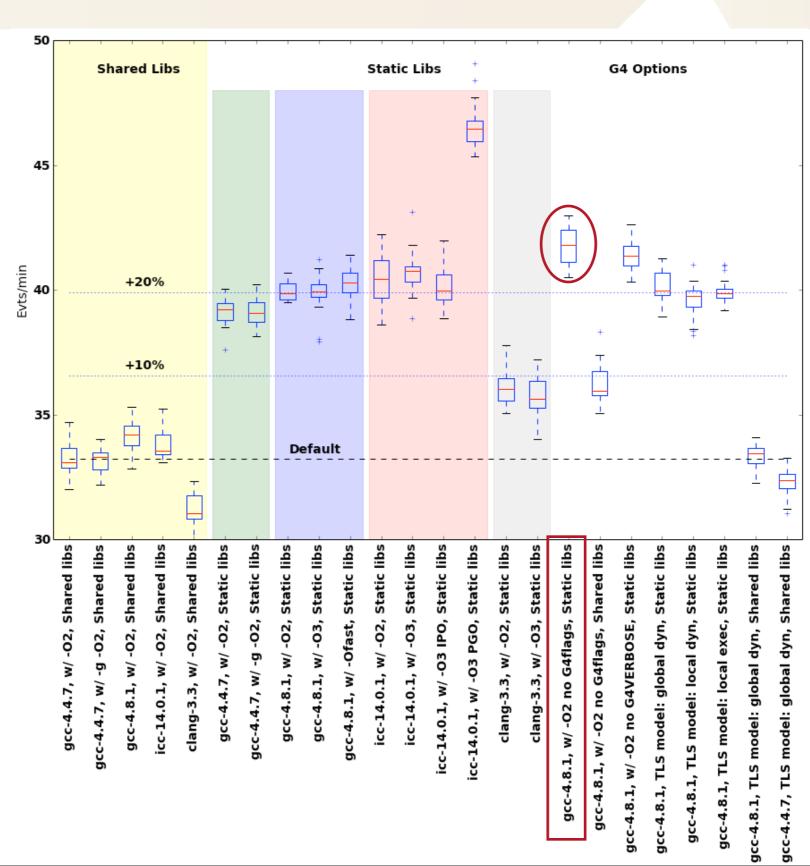
All other are max TDP specifications

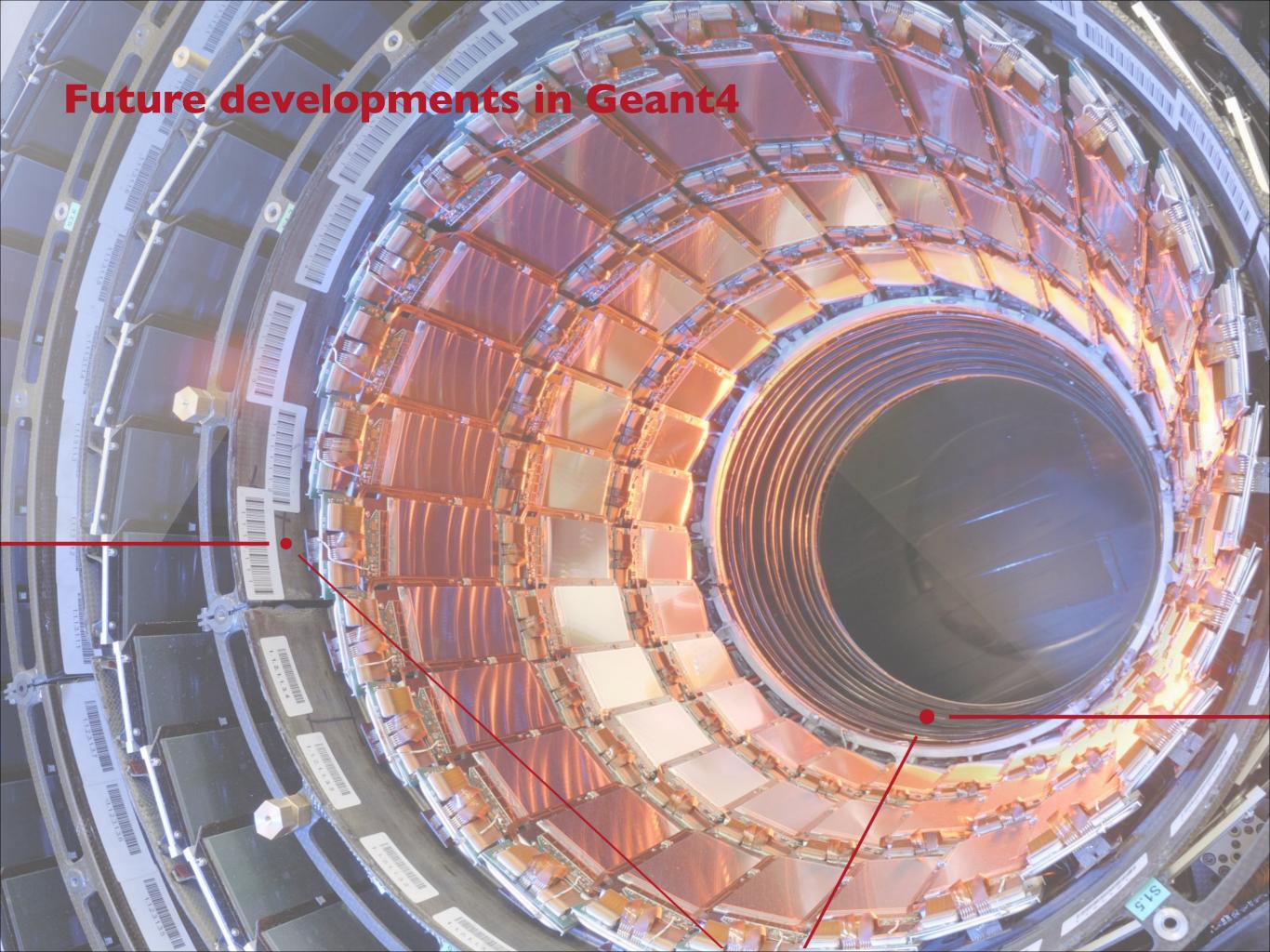
Comparison of compilation options/libraries





- Using to static libraries shows a 20% gain in performances
- Turning off some G4
 options for
 productions also
 additional brings 6-7%





Highest priority



- Further reduce memory consumption. Rule of the thumb: fit complex simulations w/ O(100) threads in O(GB) memory
 - e.g. typical computing power of accelerators
- In our experience: minimize memory usage can sometime **conflict** with other performance considerations (e.g. reduce memory "churn" via caching need special attention for thread-safety)
- Most memory consuming objects: geometry and EM physics
 - Efficient memory reduction already achieved in 10.0.beta
 - Next: need to **concentrate on Hadronics physics** (especially: cross-sections, specific models with large not-shared tables -BIC-)

Task-based model: CMS



- Current design assumes thread and worker are same thing...
- Not always easy to integrate with external frameworks based on **task** concept (no direct control of threads).
 - Strong interest from CMS on Intel's TBB, ATLAS is also considering it (at least as a level of study)
 - Important requirement: assume we have a pool of tasks of different nature (generation, simulation, digitization, reco, I/O) to be executed by a set of threads. We want to "occupy" only a fraction of the threads with simulation task at any given moment. This requires "migration" of simulation from a thread to another one ("clean up" is the difficult part)
- •Introduced concept of "workspace":
 - Encapsulate all thread/task private data in resource that can be exclusively requested, used and released
 - Currently only limited functionality for geometry module

"Splitting" of events: ATLAS



- ATLAS framework can already implement a simple sub-event parallelism:
 - Get a single generator event (hundreds primaries) and divide it (e.g. by region)
 - Each "piece" becomes a G4Event
 - Hand over to G4 each separately. Effectively split a huge HEP event in many G4Events
- Possible to use MT to parallelize
 - Once framework is made thread-safe: work ongoing

Heterogeneous parallelism: MPI based G4MT



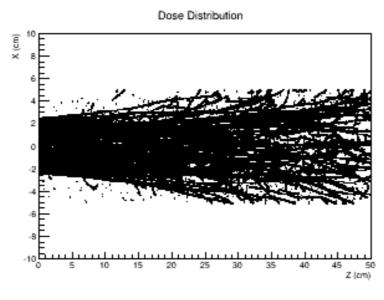
- MPI based parallelism available in Geant4
 - MPI works together with MT
 - Probably most interesting for non-HEP domains and/or SuperComputers

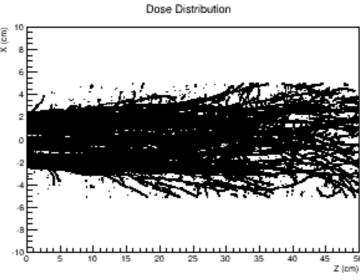
Example:

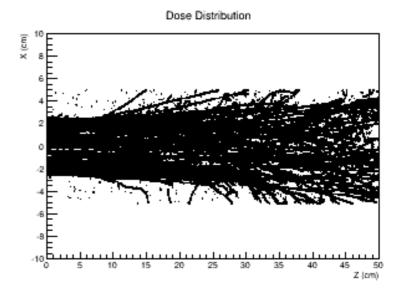
4 MPI jobs 2 threads/job MPI job owns histogram

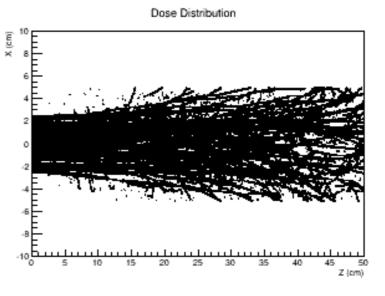
Next Step:

Host + MIC simulation Based on MPI









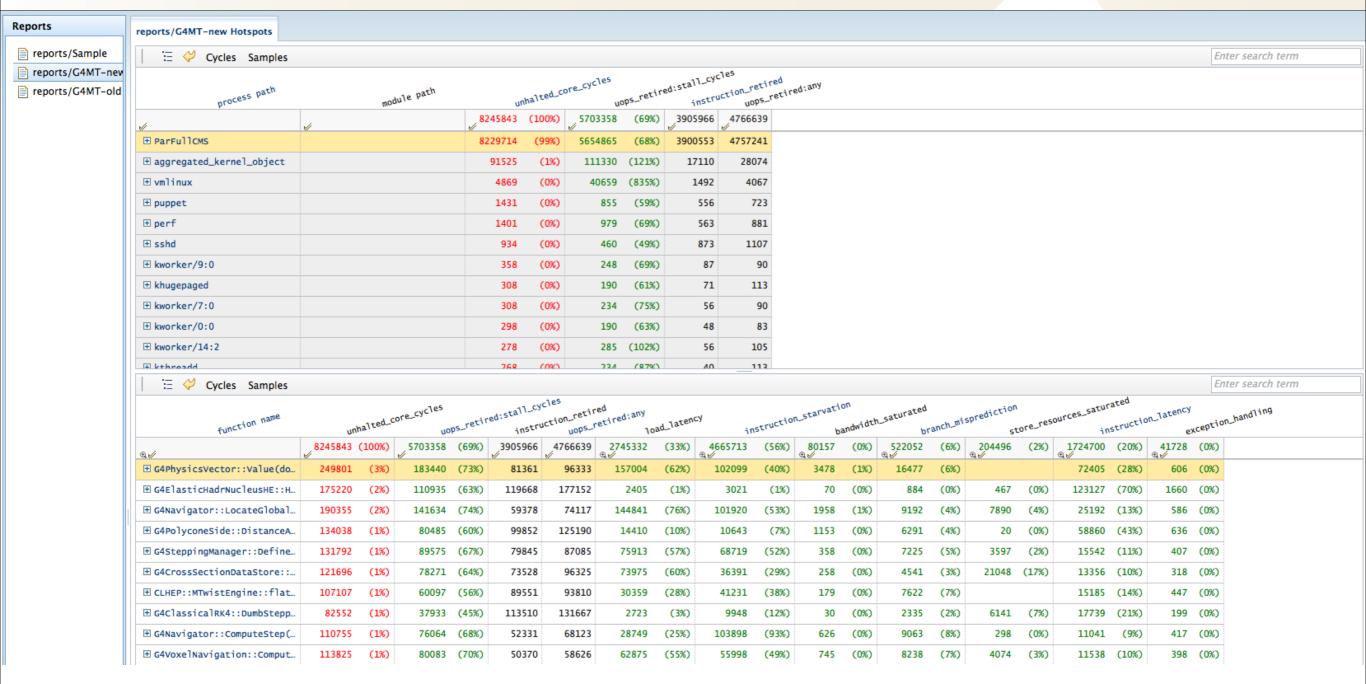
2014+ simplified work-plan



- We already have intra-node and intra-core parallelism efficiently in place
 - Algorithm implementations are the place to look to get more performance (examples: see G4em review from Krzystof and Had XS caching from Pedro)
- From profiling analysis:
 - G4 profile **is very flat**: top 5 functions take: 3%, 2%, 2%, 1%, 1%
 - For HEP use cases CPU-time is spent equally in geometry and physics (~30% each)
- From profiling we can see what to improve:
 - Complex algorithms: often they are "plain translations" of complex physics formulas: not CPU efficient (but easier to read)
 - Review use of (large) arrays and caching of numbers (especially true for MT)
 - Introduce modern **parallel** RNG engine (RNG takes ~1%) and use of RNG vector interfaces
 - Similarly look at other "mathematical" aspects: 3- and 4-vectors
 - Switching to fast G4Pow and G4Log brought several % improvements

Gooda Example (ParFullCMS)





Where do we spend time?

SLAC

	8229714	(99%)
/data/adotti/new/lib64/libG4processes.so	2862844	(34%)
/data/adotti/new/lib64/libG4geometry.so	2488445	(30%)
/lib64/libm-2.12.so	879001	(10%)
/data/adotti/new/lib64/libG4tracking.so	487678	(5%)
/data/adotti/new/lib64/libG4clhep.so	307310	(3%)
/data/adotti/new/lib64/libG4global.so	355528	(4%)
/data/adotti/new/lib64/libG4track.so	299122	(3%)

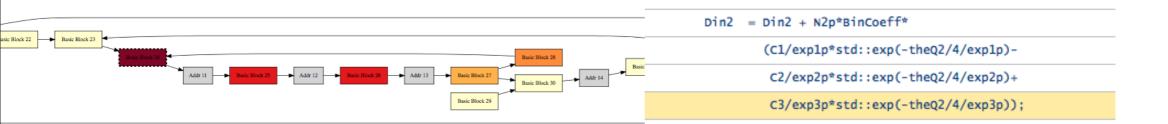
Physics Geometry

B-Field

/da ⊕√	8245843	(100%)
⊕ G4PhysicsVector::Value(double, unsigned long&) const	249801	(3%)
⊕ G4ElasticHadrNucleusHE::HadrNucDifferCrSec(int, int, double)	175220	(2%)
⊕ G4Navigator::LocateGlobalPointAndSetup(CLHEP::Hep3Vector const&, CL	190355	(2%)
	134038	(1%)
	131792	(1%)
	121696	(1%)
<pre>① CLHEP::MTwistEngine::flat()</pre>	107107	(1%)
⊕ G4ClassicalRK4::DumbStepper(double const*, double const*, double, d	82552	(1%)
⊕ G4Navigator::ComputeStep(CLHEP::Hep3Vector const&, CLHEP::Hep3Vecto	110755	(1%)
	113825	(1%)
⊕ G4Mag_UsualEqRhs::EvaluateRhsGivenB(double const*, double const*, d	109085	(1%)
⊕ G4SteppingManager::Stepping()	102486	(1%)
■ G4Transportation::AlongStepGetPhysicalInteractionLength(G4Track con)	99485	(1%)
■ G4PolyPhiFace::InsideEdges(double, double, double*, G4PolyPhiFaceVe	81826	(0%)

Specific HAD σ
EM physics tables
Geometry navigation
Specific geometry
Navigation / σ interrogation
HAD σ
RNG
B-Field
Geometry navigation
Geometry navigation
B-Field
Geometry navigation
Geometry navigation
Specific geometry

Example: our opportunities in the two top functions



Hadronic cross-sections (2%): two-level loop containing three std::exp and divisions between doubles

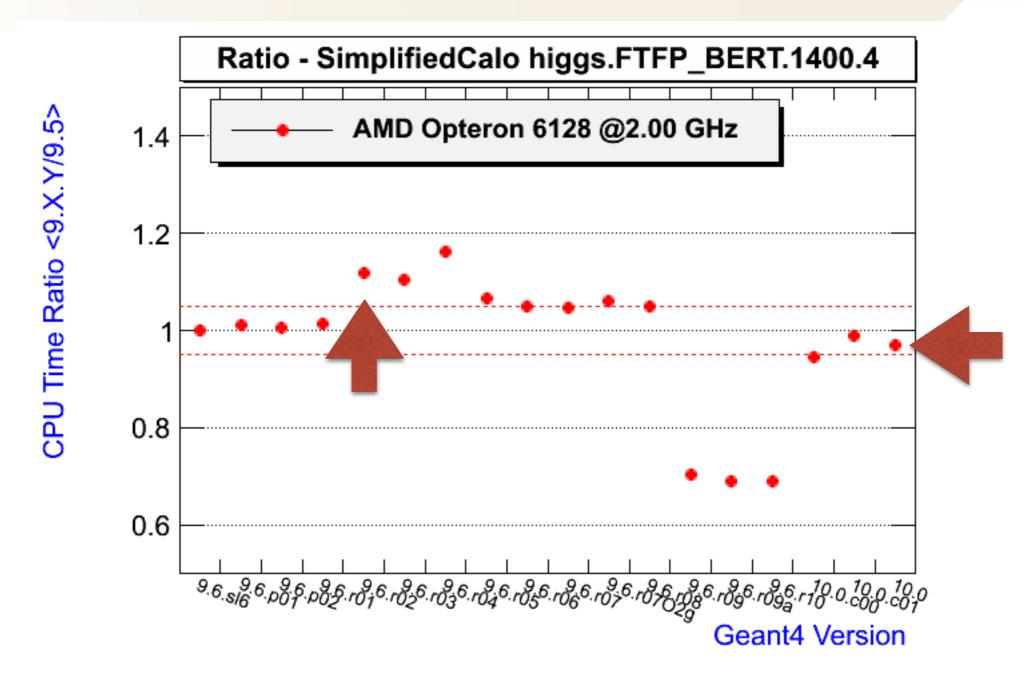
```
The Back State Sta
```

```
519    y = dataVector[lastIdx];
520    } else {
521        lastIdx = FindBin(theEnergy, lastIdx);
522        y = Interpolation(lastIdx, theEnergy);
523    }
524    return y;
525 }
```

EM tables (3%): search in large array resulting in low cache efficiency

Benefits of MT developments for sequential code



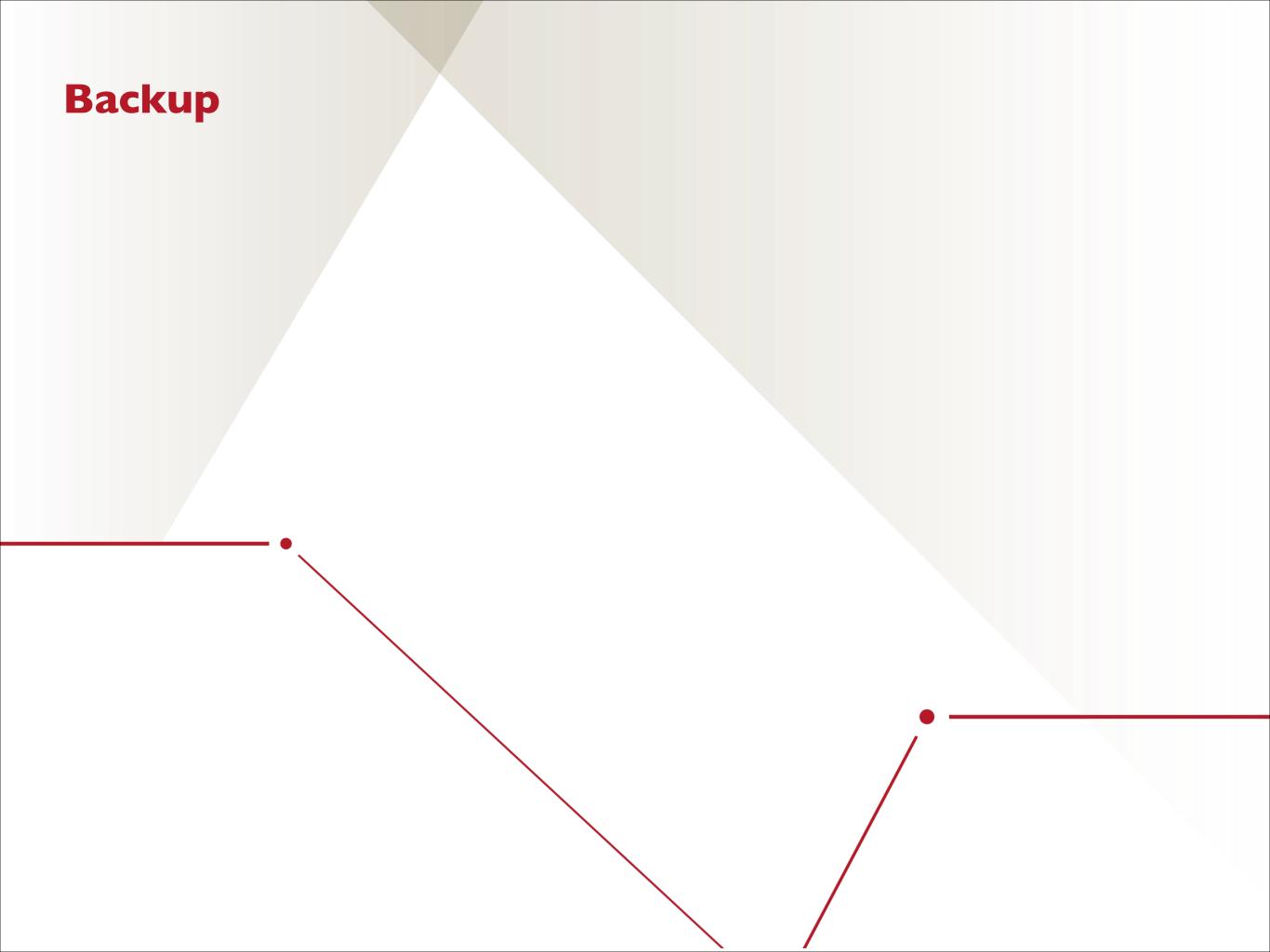


Very important lesson learnt this year: improvements in MT has given benefits also to sequential users!

Conclusions



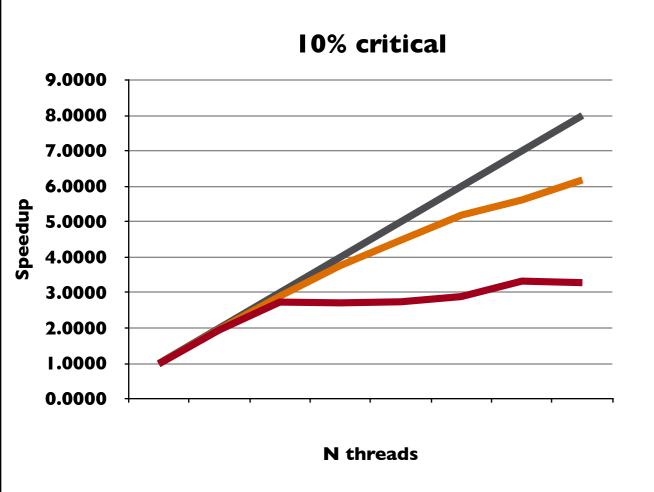
- Geant4 version 10 is the first large scale HEP software to massively employ parallelism through multithreading
- Thread-safe code is the most important precondition for parallel software: G4 code is now fully thread-safe
- Opportunities exists to speedup simulation (e.g. 20% from static libs)
 without need to modify code
 - We have seen clear trend in compiler generations in producing more efficient code. What else can we use better (e.g. PGO, auto-vectorization,...)?
- Large core-count and/or low-power consumption architectures can be used with HEP typical workloads
- Physics performance of G4 is demonstrated (e.g. Higgs discovery, treatment planning): improving the speed of physics algorithm would give greater benefit.



G4 on MIC



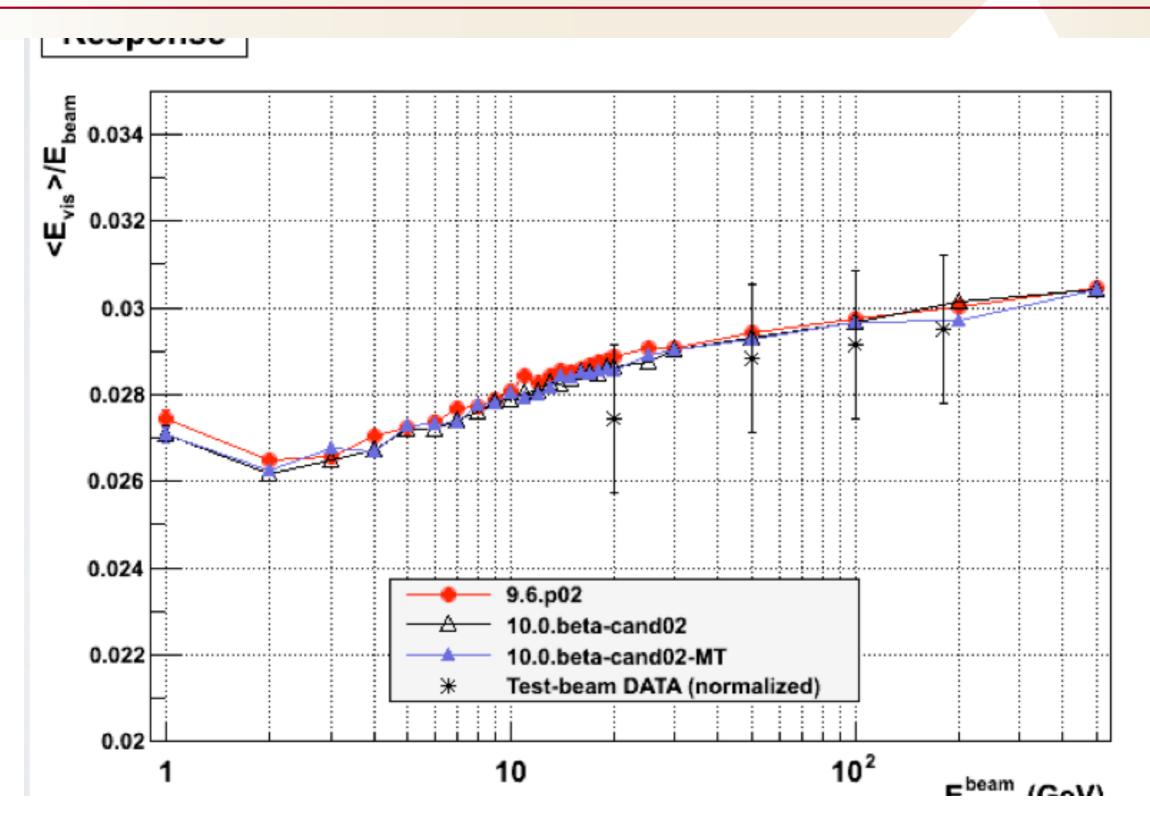
- Cross-compilation was relatively straightforward:
 - Adding -mmic to compilation flags via CMake
 - Modified couple of files implementing GNU specific pragmas
- Two ways of working:
 - Offload work to the card (via **#pragma**)
 - Native mode compile full application, start via ssh
- Only second option used so far: particularly attractive combining with MPI since minimizes data traffic over PCIe
 - Coordinate same program on host and card
 - Checkpointing successfully used to substantially speedup initialization from O(min) down to O(sec)
- Limitation was memory usage: only with top of the line MIC model can use all 244 threads



- Each (parallel) program has sequential components
 - Protect access to concurrent resources
- Simplest solution: use mutex/lock
- TLS: each thread has its own object (no need to lock)
 - Supported by all modern compilers
- Challenge: only simple data types for static/global variables can be made TLS
- Warning: hidden locks are important too (e.g. operator new, use of std::strstream)

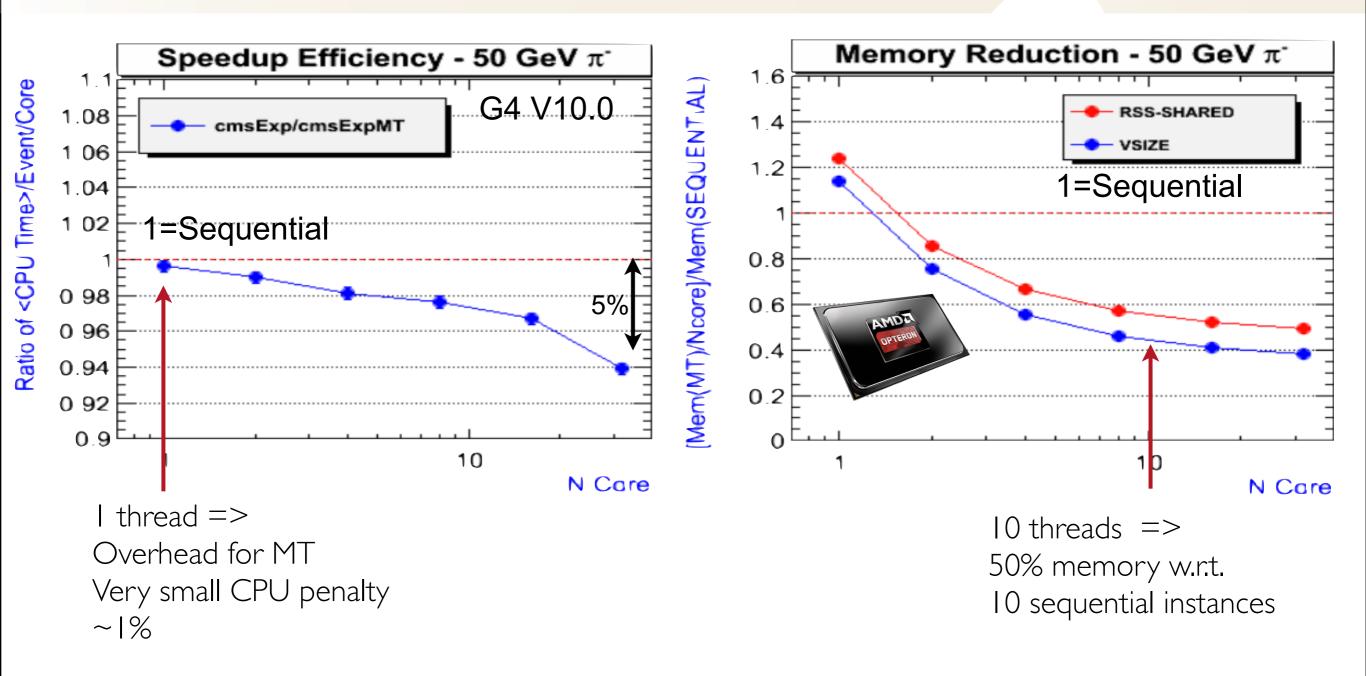
MT libs Vs SEQ libs





Comparing with sequential





Hadronic memory usage



- The hadronics most memory hungry (5MB) hot-spot is BIC model (even when not used). Some rework needed
- The second Hadronics components using more memory are cross-sections (2.2MB) stored in G4CrossSectionDataStore
- Models/processes account for about IMB of memory
- It is realistic to reduce memory footprint for Hadronics of a factor 2
- Note: other models have a completely different profile
 - HP models: currently each thread load all HP tables, test I I for HP uses several GB of memory. No work on this done yet
 - Requires strategy for sharing database files