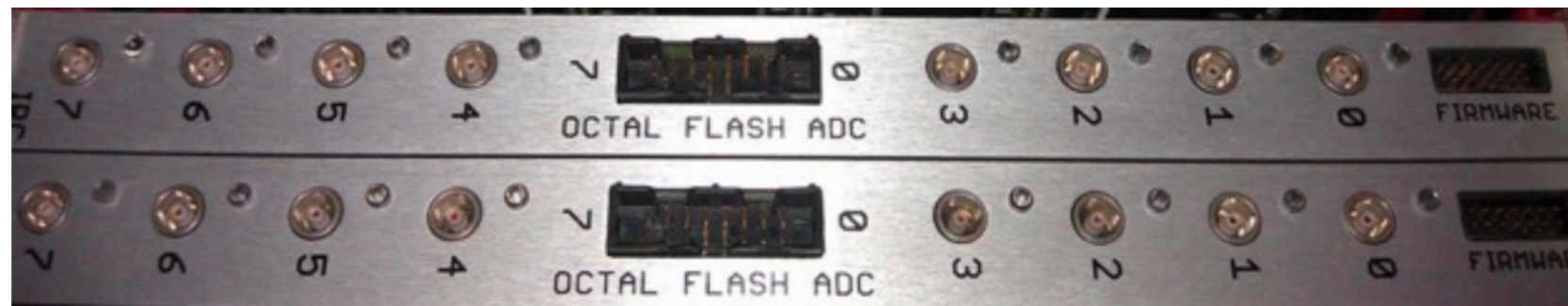


FADC: overview and performance

Joe Grange
ANL
3/24/14



Outline

- ▶ Gaining familiarity with FADC system
 - (growing pains)
- ▶ Quality control and utility in data analysis

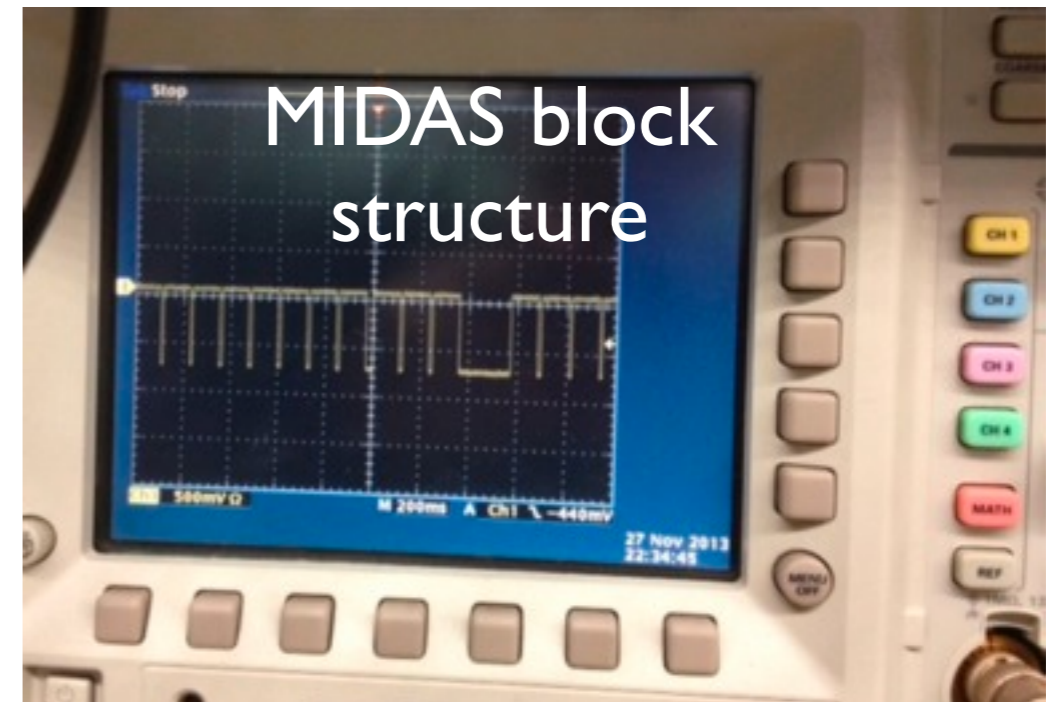
Early troubles

- ▶ Early FADC sanity check: inject pulser signal to two systems
 - MCA. Mostly standalone program with various benefits/drawbacks.
 - FADC. Data collected by MIDAS, analyzed by user modules.

Run #	FADC analysis	MCA
624	11069	14723
627	6467	8724

- ▶ Immediate rate discrepancy (~30% in this case!)

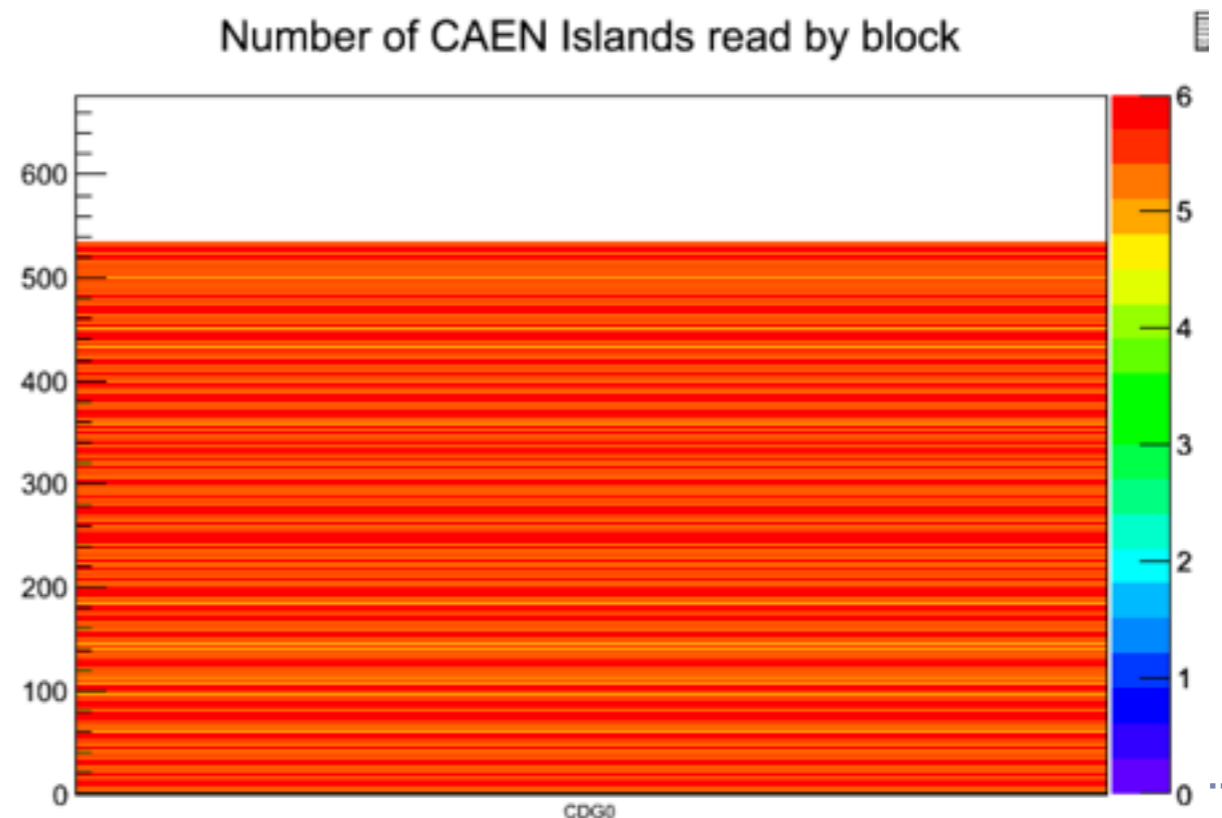
- ▶ Obvious difference between two methods: many steps between hardware and results for FADC. Andy, Ben and I spent much time w/ MIDAS blocks and deadtime



Early troubles

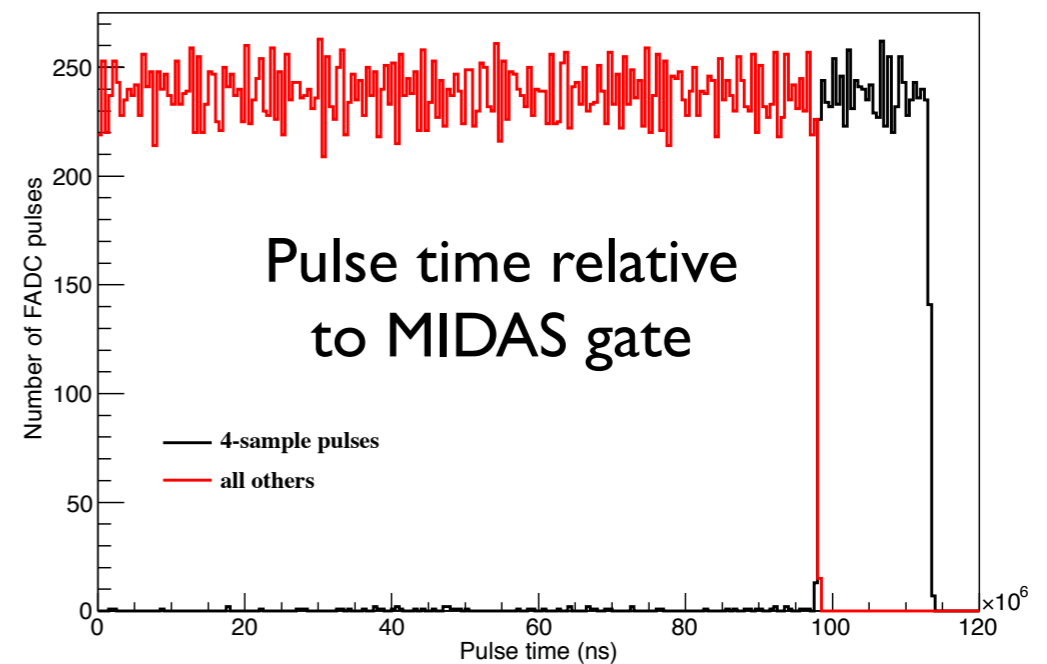
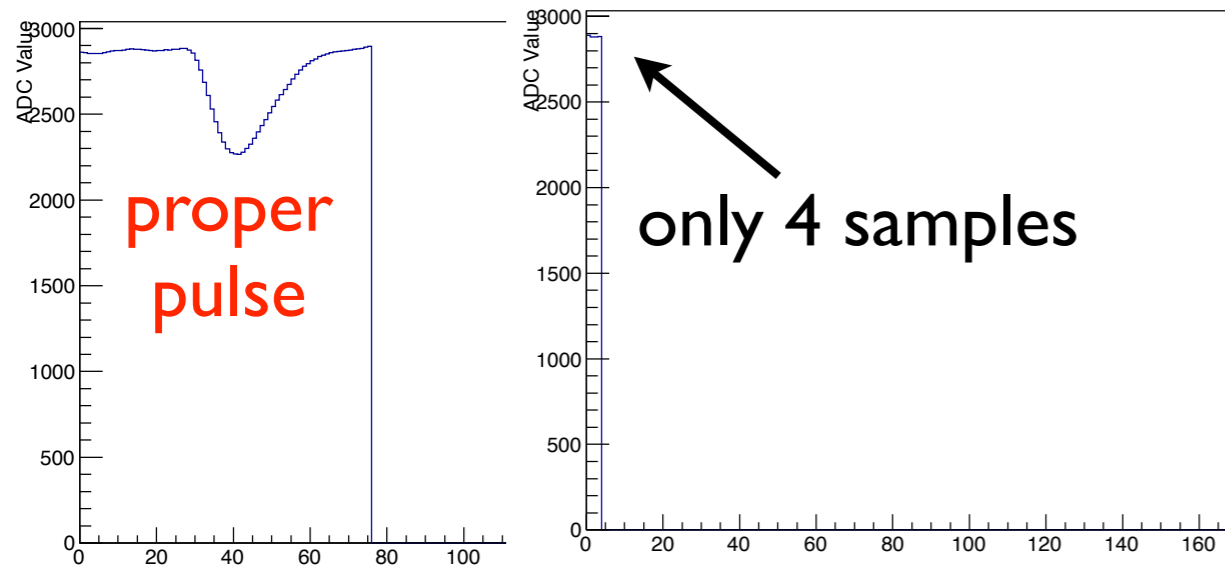
- ▶ Deadtime structure important to understand observed rates, but problem remained.
 - chosen structure: 110ms \uparrow , 10ms \downarrow = 8% deadtime.
- ▶ Ben had the great idea to *measure* the up-time using coincidence/anti-coincidence using scaler
 - still didn't do it, but continuing to learn valuable info: ~14% measured deadtime from MIDAS
- ▶ What about CAEN digitizer?
 - (same DAQ, diff. hardware, analyzer modules)

CAEN sees ~14% deadtime, expected number pulses per gate



Early troubles solved

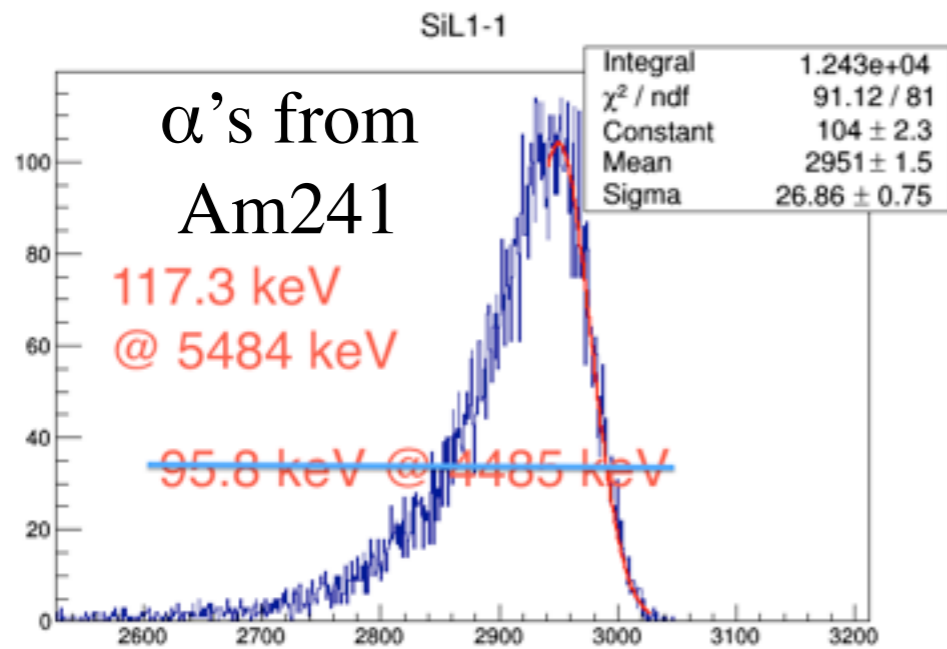
- ▶ Have control sample! Looked to correlate pulses observed in CAEN with FADC (when were lost pulses lost?).
 - Andy developed lots of timing analysis modules helpful for later beam/data correlations
- ▶ Simple software bug discarded final pulse in each MIDAS block, in its place created stubby four-sample pulses.



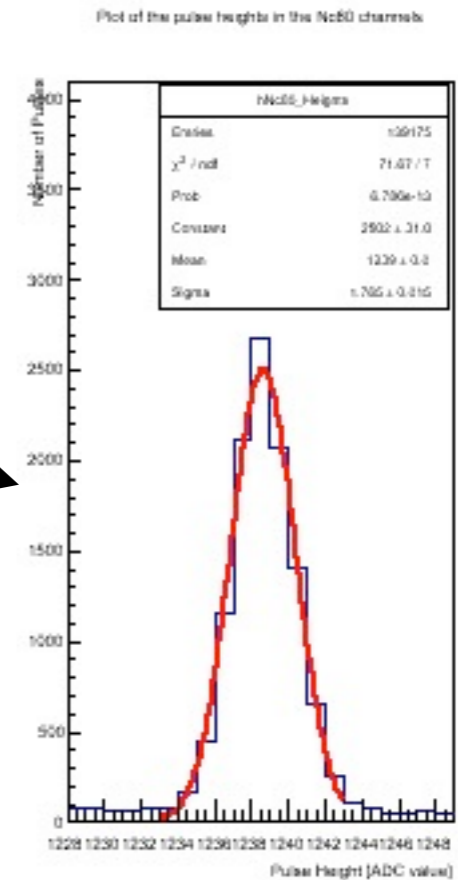
- ▶ Fred Gray provided the overseas assist, also provided us with updated FADC firmware (unrelated to these issues)

Calibrations

- ▶ Constrain FADC response with known radioactivity



Ge calib.
4 keV @
1.17 MeV



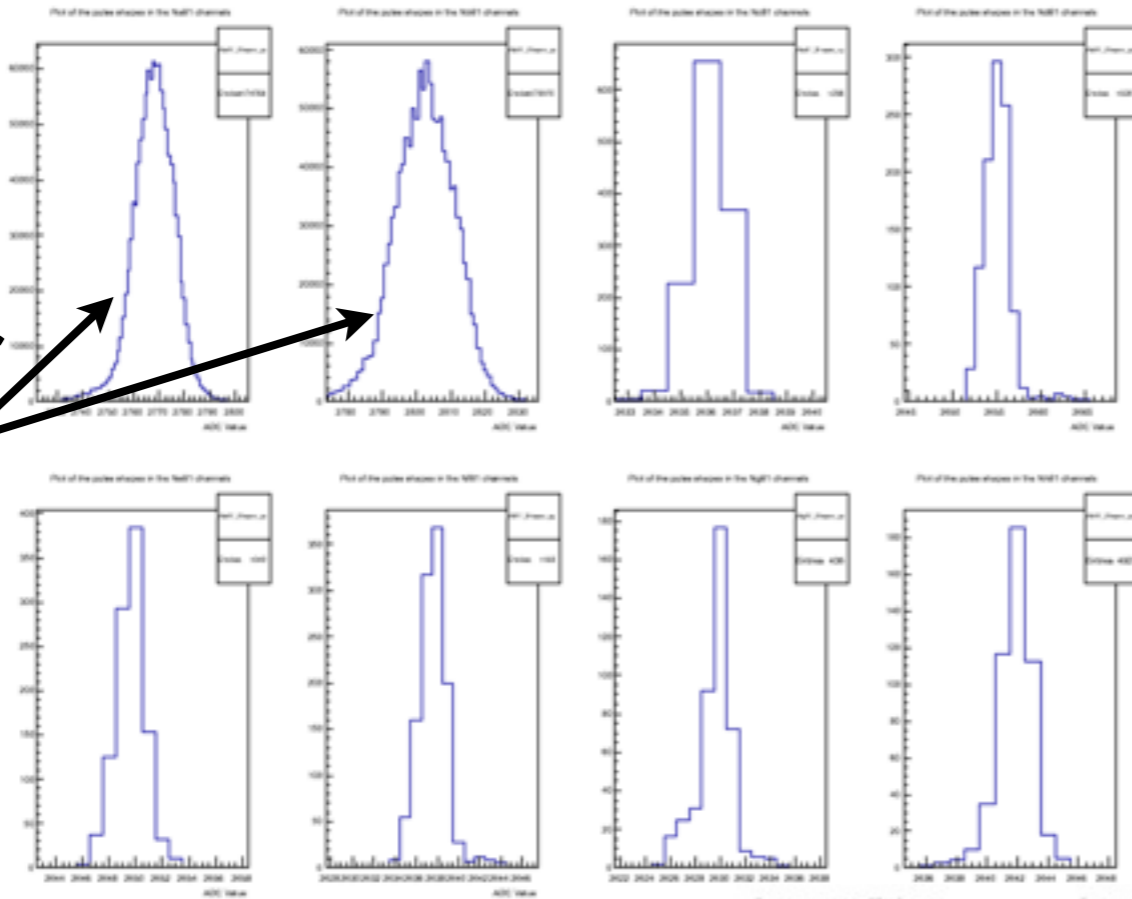
Bank	Pedestal [ADC]	Mean [ADC]	Height [ADC]	Sigma [ADC]	Resolution [keV]
Ne82	2631	590.9	2040.1	16.21	102
Nf82	2642	630.8	2011.2	21.62	138
Ng82	2631	588.2	2042.8	19.87	125
Nh82	2631	716.4	1915.6	18.79	126

↑
 α 's from
Am241

Noise

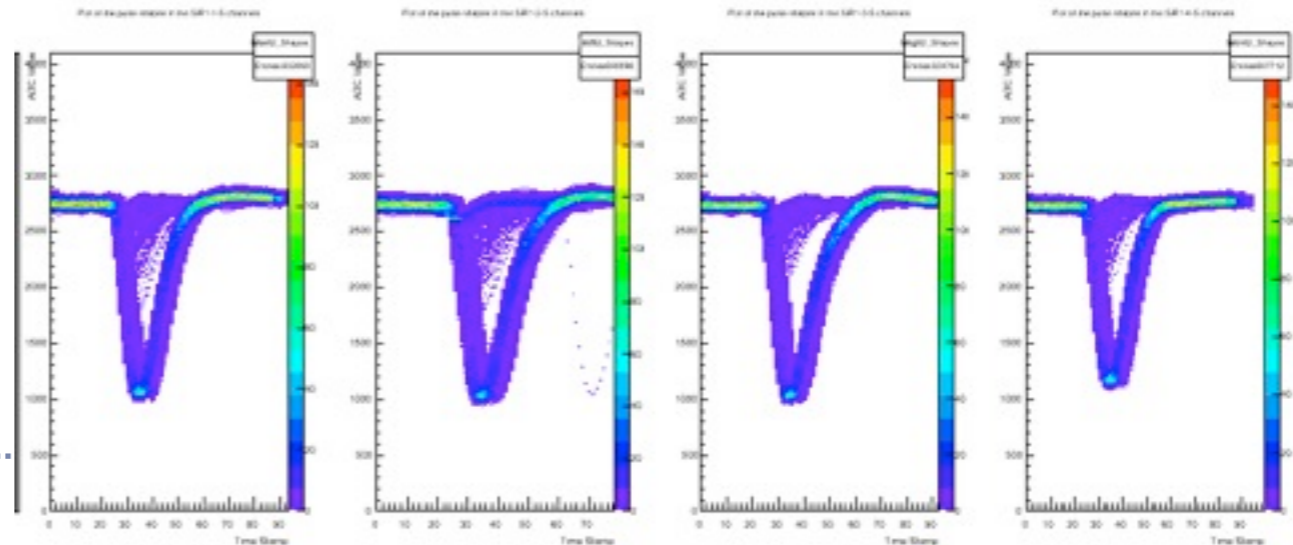
- ▶ FADC's very noisy early on

Self-trigger
~30 ct
noise



Other ch:
plugged in Si but
not turned on
~4 ct noise

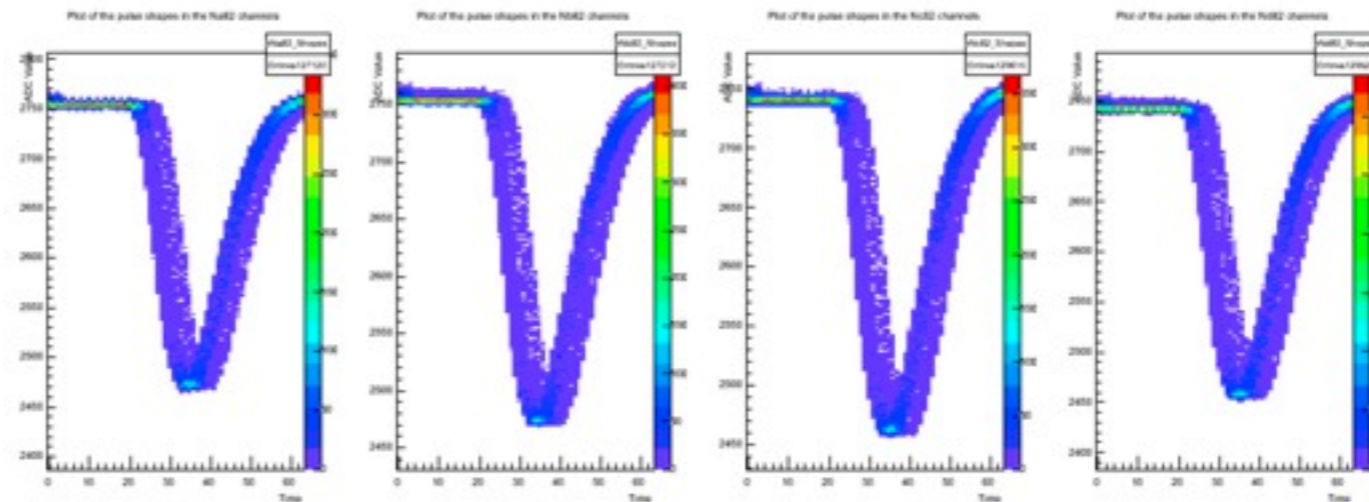
- ▶ Also, funny pulse shape from pulser:



Noise

- ▶ Suspected bad power supply swapped before serious beam runs. Changed to 120A MuSun power supply.

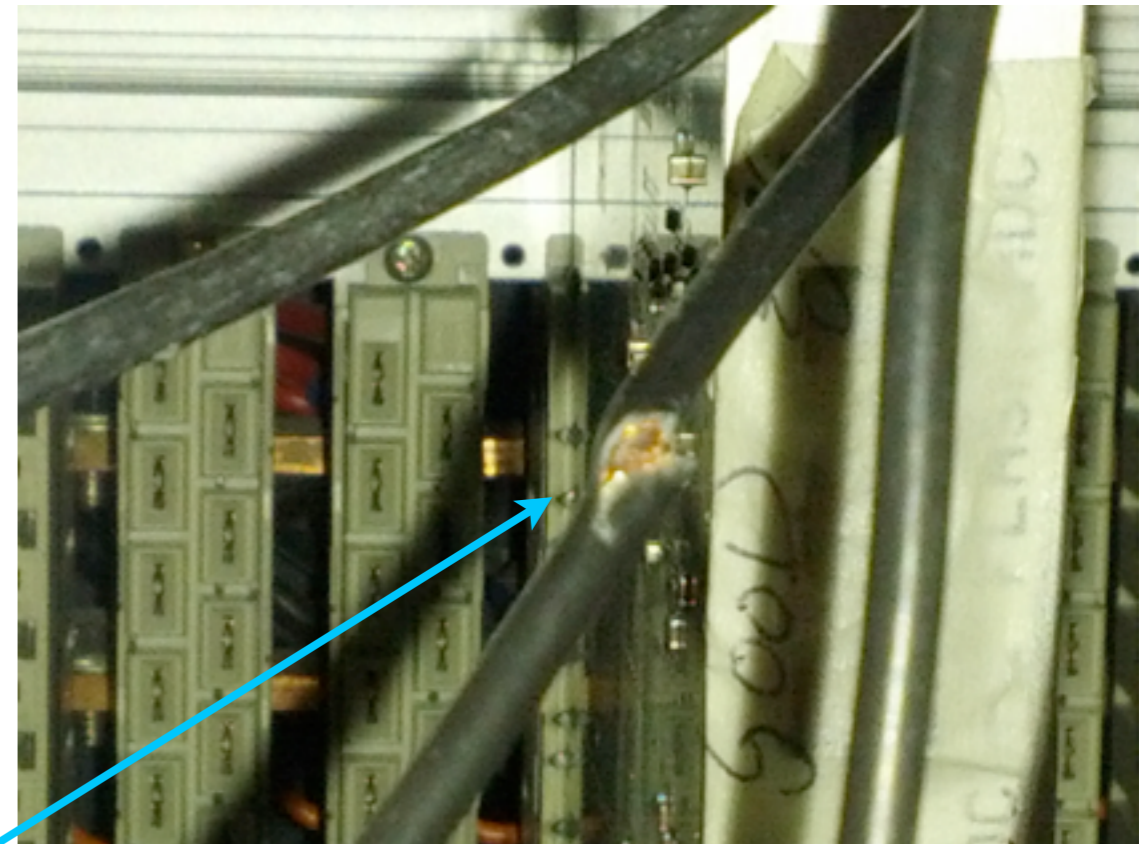
- ▶ Updated pulse shapes:



Board	channel	No detector			Detector connected	
		mean (ch)	sigma (ch)	FWHM (keV)	sigma (ch)	FWHM (keV)
x80	SiL-2	132.9	1.45	25.75	4.2	74.58
x80	SiR-2	151.0	1.91	29.87	2.6	40.64
x82	SiL-1-1	281.3	1.68	14.09	6.60	55.37
x82	SiL-1-2	278.9	1.56	13.20	11.3	95.62
x82	SiL-1-3	289.2	1.62	13.22	11.6	94.66
x82	SiL-1-4	295.0	1.66	13.28	29	232.00

Misc issues encountered

- ▶ Many, many MIDAS crashes and errors mysteriously solved by reloading .odb file from most recent successful run + much patience (power cycling)
- ▶ More serious FADC frontend crashes req'd DAQ reboots
- ▶ Cable woes
 - wiggling caused dramatic changes in signal/noise
 - damage prevented any signal transmission
 - ethernet connection to DAQ not secure



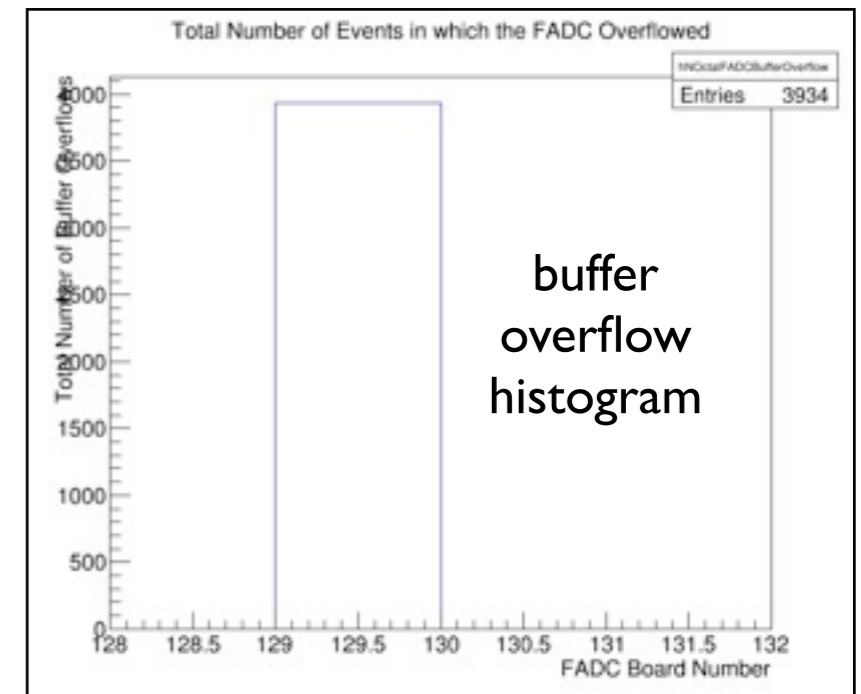
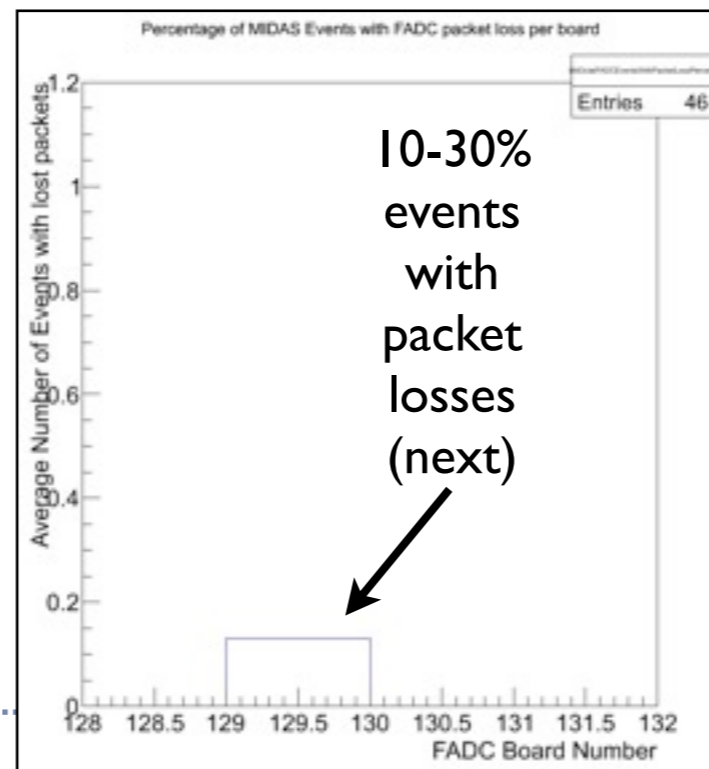
-
- ▶ Gaining familiarity with FADC system
 - (growing pains)
 - ▶ **Quality control and utility in data analysis**

FADC package losses

- ▶ Fred's updated firmware reports when internal FPGA buffer is full (**and so data may be missed**), very useful tool for real-time diagnostics
- ▶ PeterW added monitoring capabilities to FADC frontend:
 - as well as a FADC timeout message, indicating not all packages collected were sent

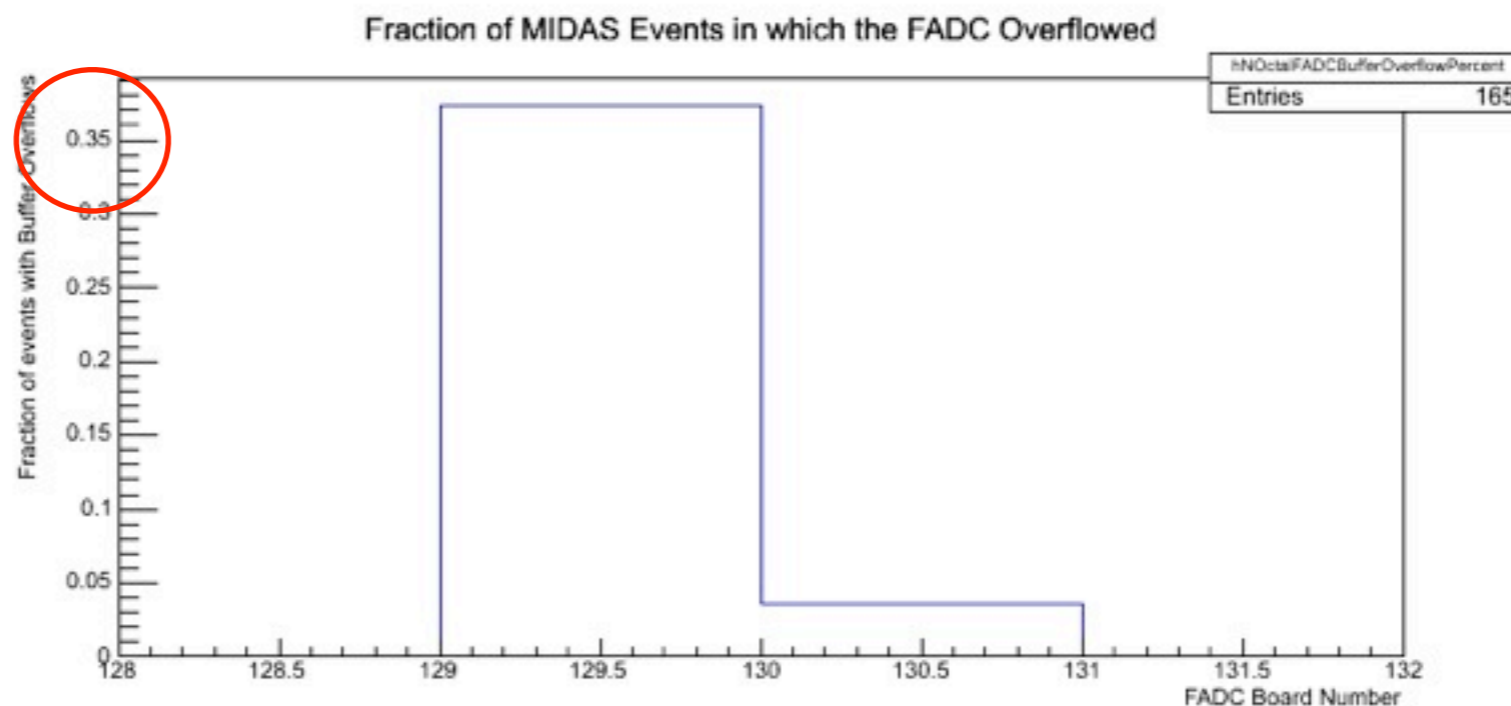
```
new_fadc_read
Board 0x81: start 16070 (+) - stop 16124 (+) - buffer full (+)
Board 0x82: start 16072 (+) - stop 16125 (+) - buffer full (+)
```

- ▶ Both these are stored in MIDAS banks, we choose how to handle at the analysis stage
 - (have we decided?)



FADC package losses

- ▶ Early on, bug in online monitoring root scripts prevented proper package loss monitoring
- ▶ When fixed, realized rates were (and presumably had been) too high (~30%)
 - unacceptable losses, combatted with increased thresholds, shortened def'n of pulse island.



- ▶ I see quantification of these rates with run numbers as a next step for myself (would this duplicate any efforts?)

Summary, next steps

- ▶ FADC system proved particularly sensitive and temperamental early on, smooth running reached when it counted
 - software bug
 - noise (power supply)
 - some troublesome cabling
- ▶ Track FADC packet losses/buffer health through physics runs to begin quantifying data/analysis confidence