Cold Electronics for Noble Liquid TPCs

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On behalf of the Cold Electronics Team

BROOKHAVEN NATIONAL LABORATORY

LArTPC14 – Liquid Argon TPC R&D Workshop

July 8-9, 2014

BROOKHAVEN NATIONAL LABORATORY

a passion for discovery

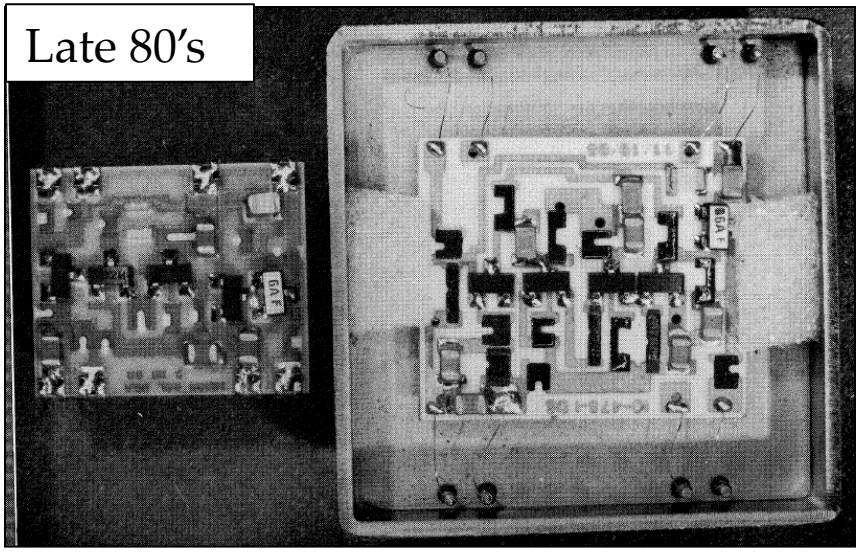
U.S. DEPARTMENT OF ENERGY | Office of Science

Outline

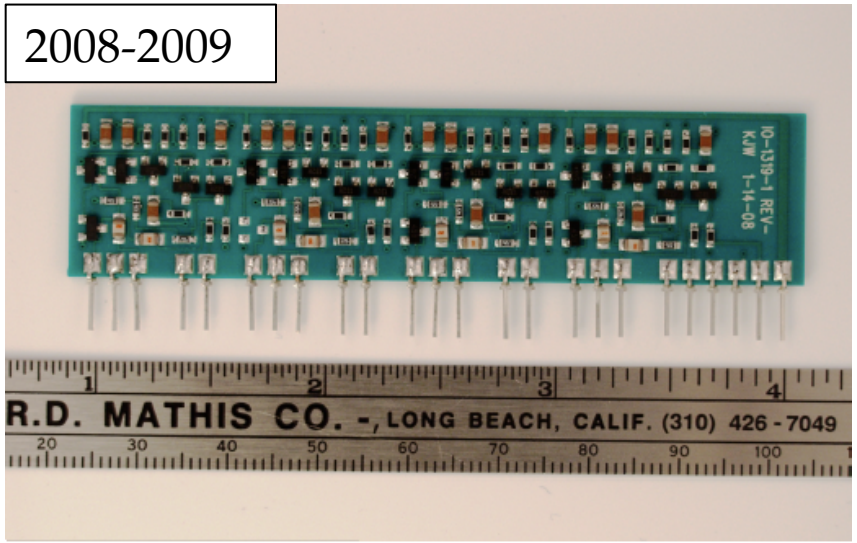
- A Brief History of Cold Electronics Development
  - From JFET to CMOS – A personal perspective
- R&D on CMOS Cold Electronics
  - Analog FE ASIC
  - ADC ASIC
  - FPGA & Cold Regulator
  - Front End Mother Board
  - Migration from Cold FPGA to Digital ASIC
- Summary

Cryogenics front-end based on JFET

Late 80's

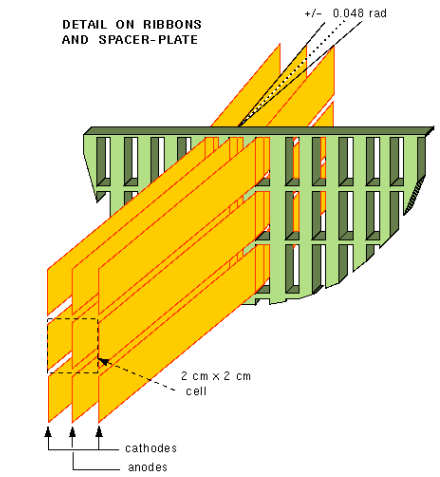


2008-2009



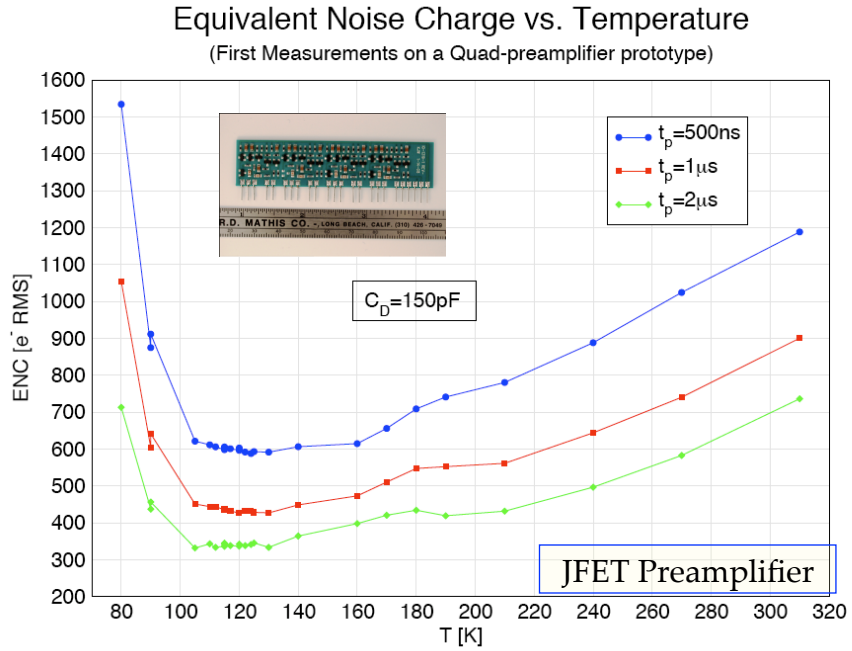
- Technology mature and available as of today
  - Reliability issues require a careful choice of component and high reliability assembly
  - Ceramic hybrid with co-fired traces and surface mount components properly tested
- Helios-NA34
  - Liquid Argon calorimeter
  - 576 preamplifiers
  - Operation: 4 years, multiple cool-downs
  - Failure: 1 caused by mechanical contact
- Several years of experience
  - MicroBooNE front-end design started from JFET as well

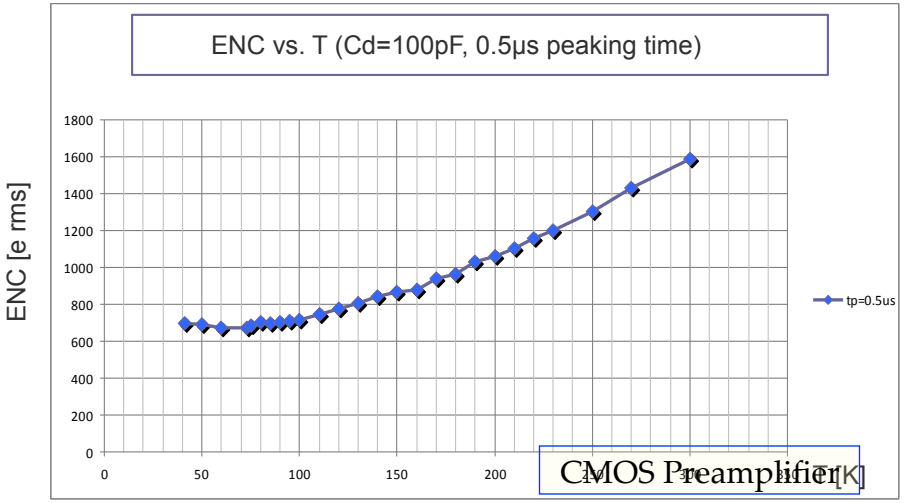
Cryogenics front-end based on JFET



- NA48
  - Liquid Krypton calorimeter
  - Preamplifiers in LKr: 13,212 channels
  - Operated at very high voltage
    - Tested up to 7kV, operated in 3kV
  - Failures
    - ~50 because of a HV accident in 1998
    - ~25 cold electronics failures after 1998, the failure rate is < 0.2%
    - The last failure recorded was more than 7 years ago
  - Always kept at cryogenic temperature since 1998
  - Operation
    - 16 years so far
    - Plan to run until 2015, expected to be in operation for 17 years

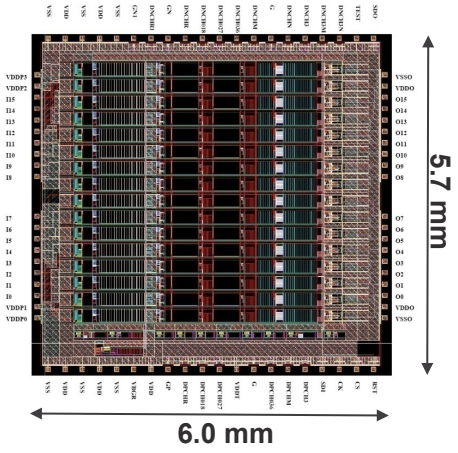
From JFET to CMOS

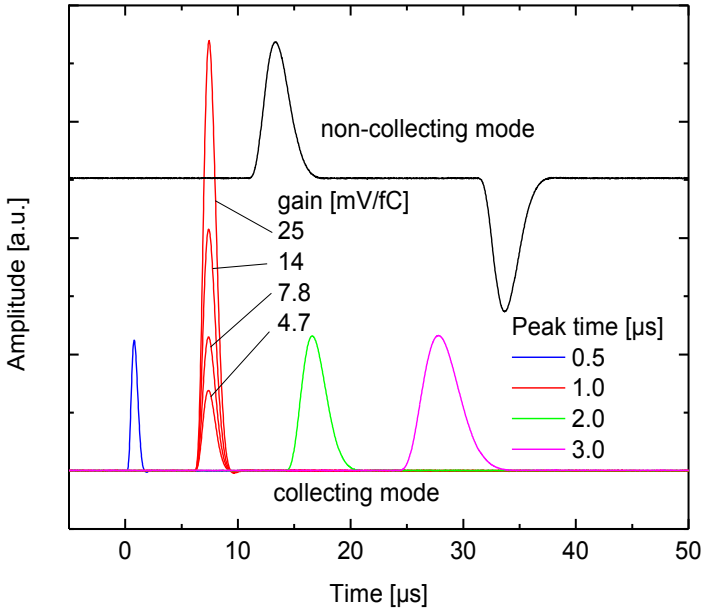




- JFET based preamplifier designed for MicroBooNE
  - Bulk mobility and transconductance increase as temperature decreases, carrier freeze out causes ENC increasing when temperature lower than ~100K
- CMOS technology – test result of an existing ASIC in 0.25 *μm (not designed for LAr)*
  - CMOS in LAr has less than half the noise as that at room temperature, higher mobility and higher transconductance/current ratio
- MicroBooNE has adopted the cryogenic CMOS analog front end ASIC developed for LBNE LAr TPC program

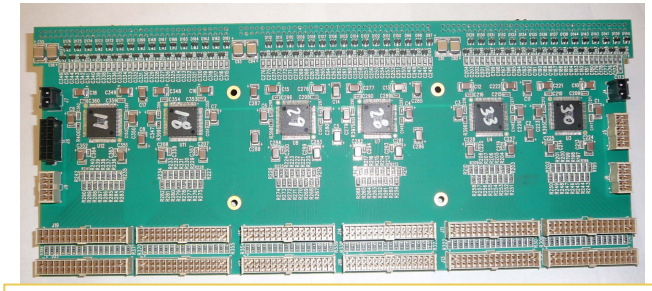
Analog FE ASIC



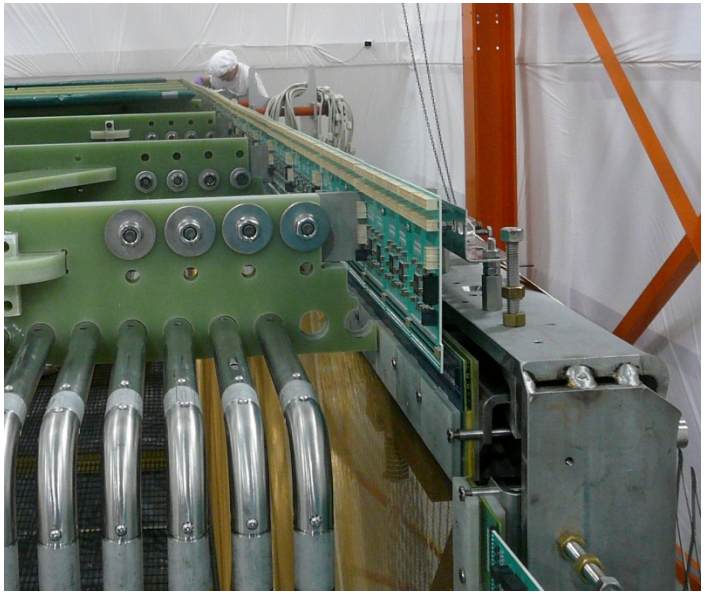


- 16 channels per chip
- Charge amplifier with high-order filter
- Adjustable gain: 4.7, 7.8, 14 and 25 mV/fC (55, 100, 180, 300 fC full dynamic range)
- Adjustable filter time constant (peaking time): 0.5, 1, 2, 3 µs
- Selectable collection/non-collection mode (baseline)
- Selectable DC/AC (100 µs) coupling
- Rail-to-rail analog signal processing
- Band-gap referenced biasing
- Temperature sensor (~3 mV/°C)
- 136 registers with digital interface
- 5.5 mW/channel (input MOSFET 3.6 mW)
- ~15,000 MOSFETs
- Designed for long cryo-lifetime
- Technology CMOS 0.18 um, 1.8 V, 6M, MIM, SBRES

Analog FE ASIC in MicroBooNE

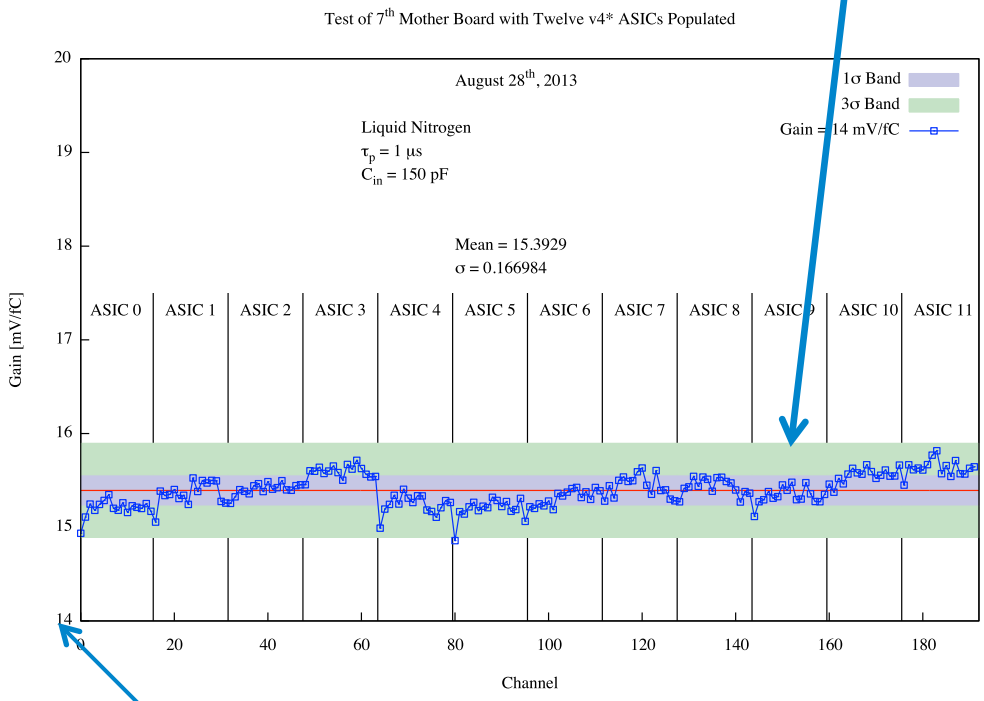


MicroBooNE cold mother board with 12 analog FE ASICs (192 channels)



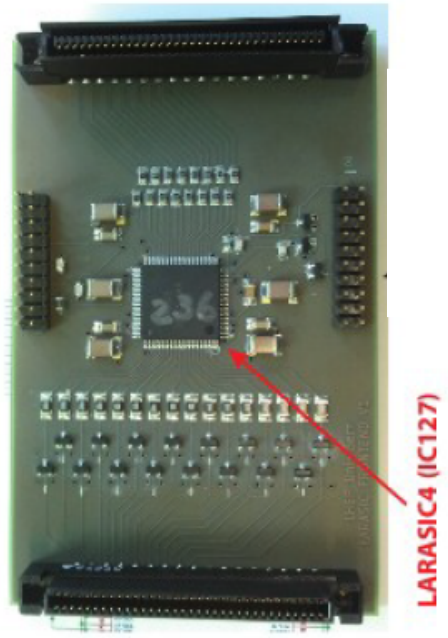
50 cold mother boards (8,256 channels) are installed on MicroBooNE TPC

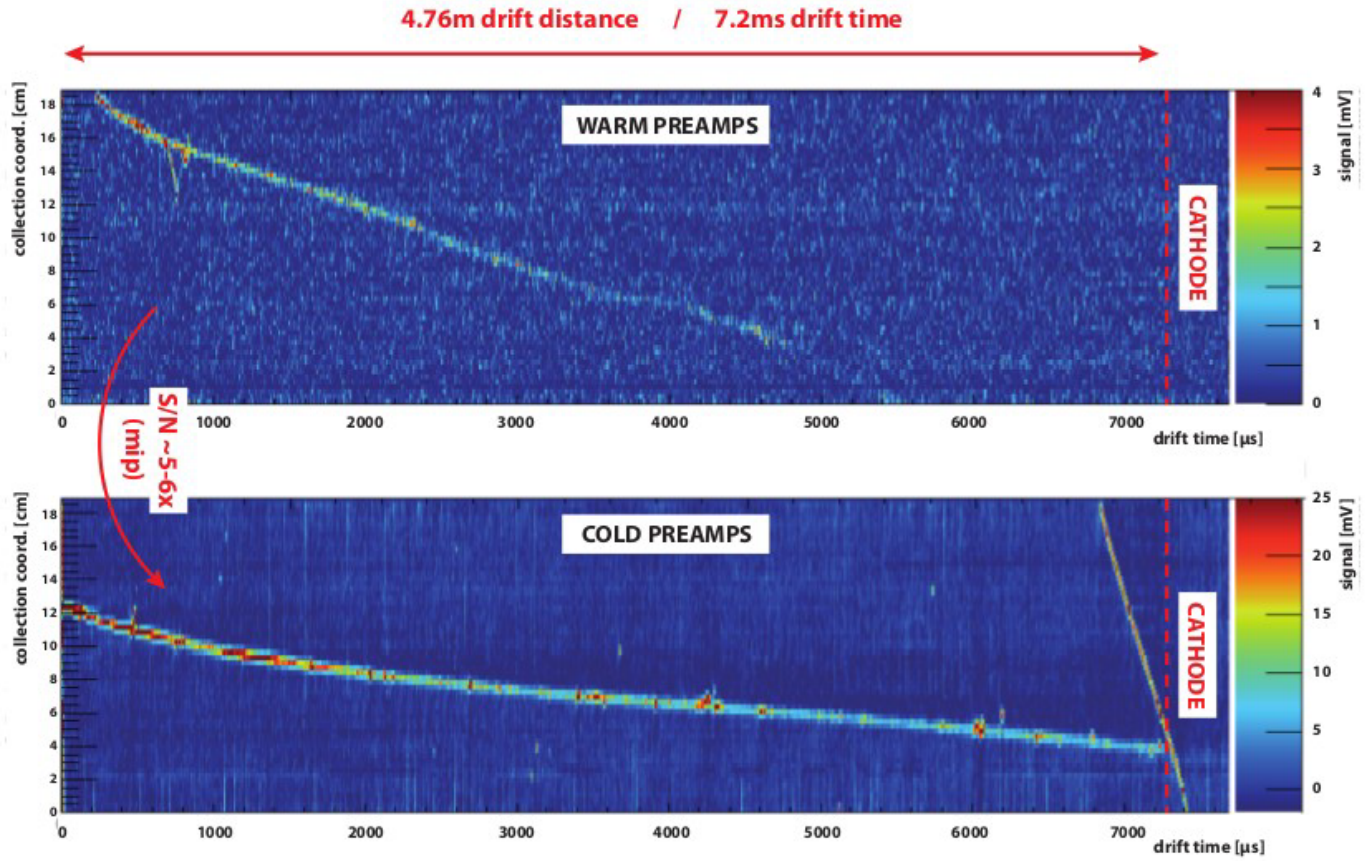
$\sigma_{gain} \approx 1\%$



Note: Offset scale

Analog FE ASIC in ARGONTUBE



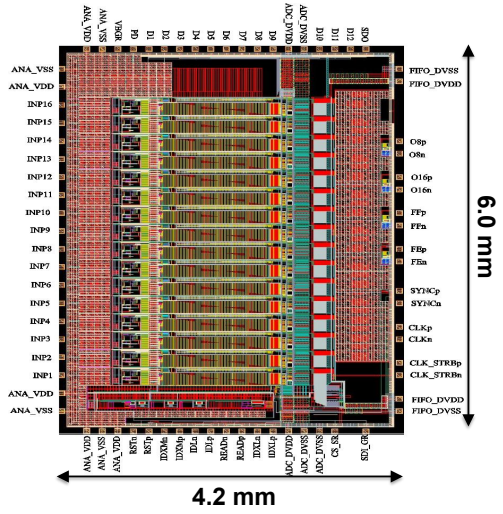


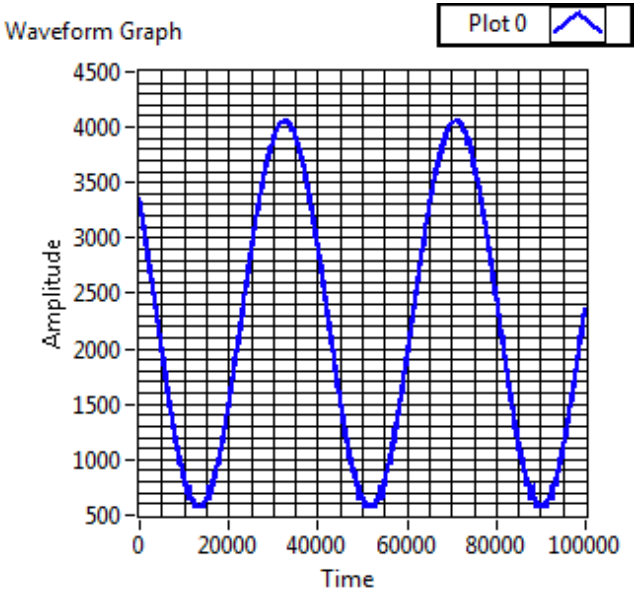
- N.B. different color scale on two plots
- Courtesy of Igor Kreslo @ University of Bern

Revision Plan of Analog FE ASIC

- Revision of FE ASIC will aim to further improve the robustness of chip and simplify the system design of the front end readout electronics
  - Revisions are limited to fine adjustments with low risk
- List of changes
  - Improve the input protection
    - Calibration pulse input (TEST)
    - Digital configuration inputs (CS, CK, SDI)
  - Implement smart reset
    - Use combination of CS and CK to generate reset internally
    - Eliminate the requirement of external reset pin
    - Circuit has been exercised in other ASICs (ADC, VMM etc.)
  - Implement internal pulse generator
    - To perform precision charge calibration
    - Calibration circuit levels will be derived from the BGR voltage
    - Calibration circuit will be programmable to accommodate the multiple gain settings and possibly perform some linearity tests
    - External high precision calibration is still accessible by bypassing internal calibration circuit
    - External calibration pulse input becomes an option, easy to scale to larger detector
  - Revision chip will be pin compatible with current design

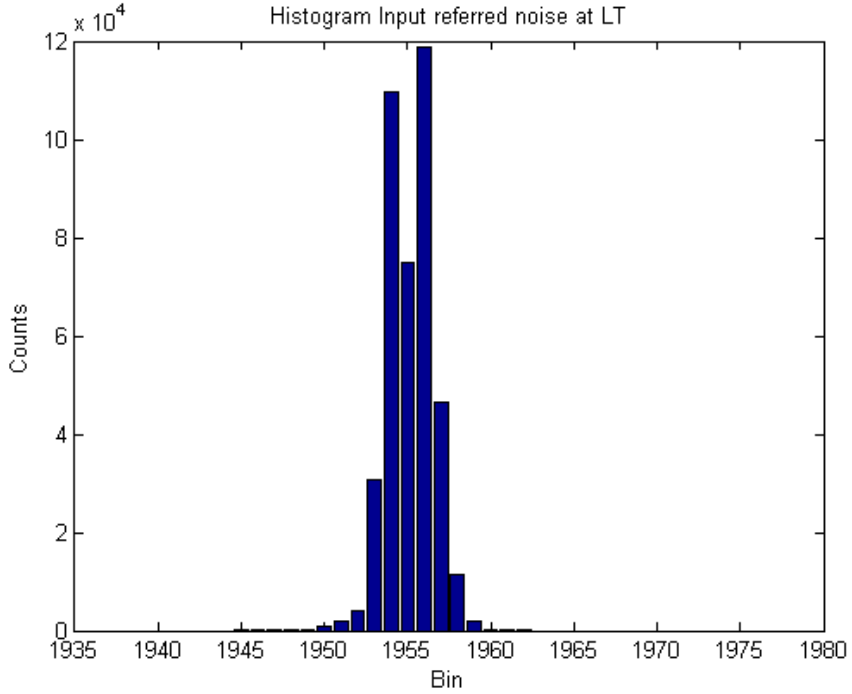
ADC ASIC

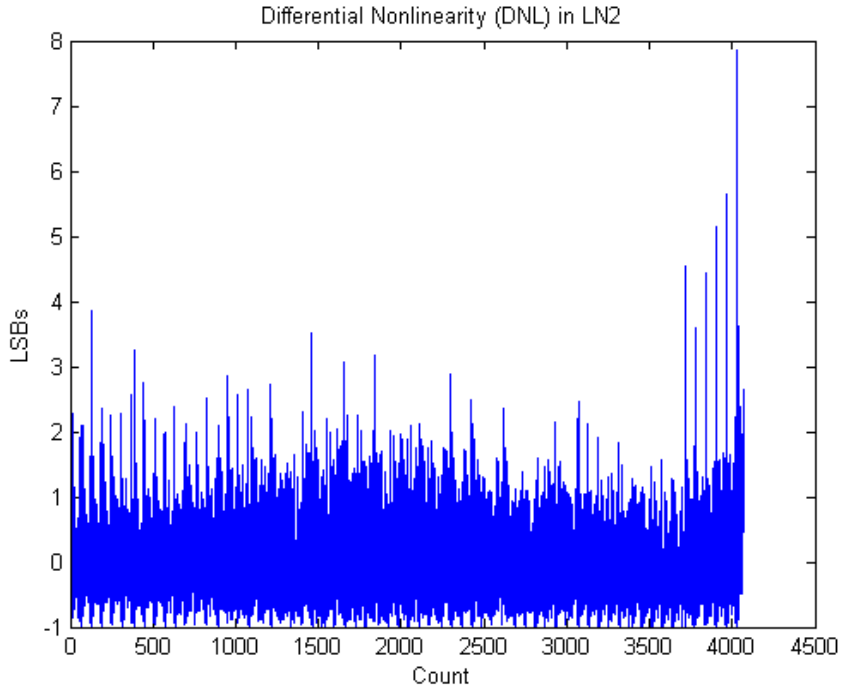




- 16 channels per chip
- Sampling rate up to 2 MS/s
- Resolution 12-bit
- Low power ADC, maximum 5 mW/ch
- Input range 0.2 V to 1.5 V
- Clockless operation, ideal for low noise operation
- Small area favorable for multi-channel system
- Low power mode with < 1 us wake-up
- Adjustable offset
- Multiple options for internal control signals
- ~315,000 MOSFETs
- Designed for long cryo-lifetime
- Technology CMOS 0.18 um, 1.8 V, 6M, MIM, SBRES

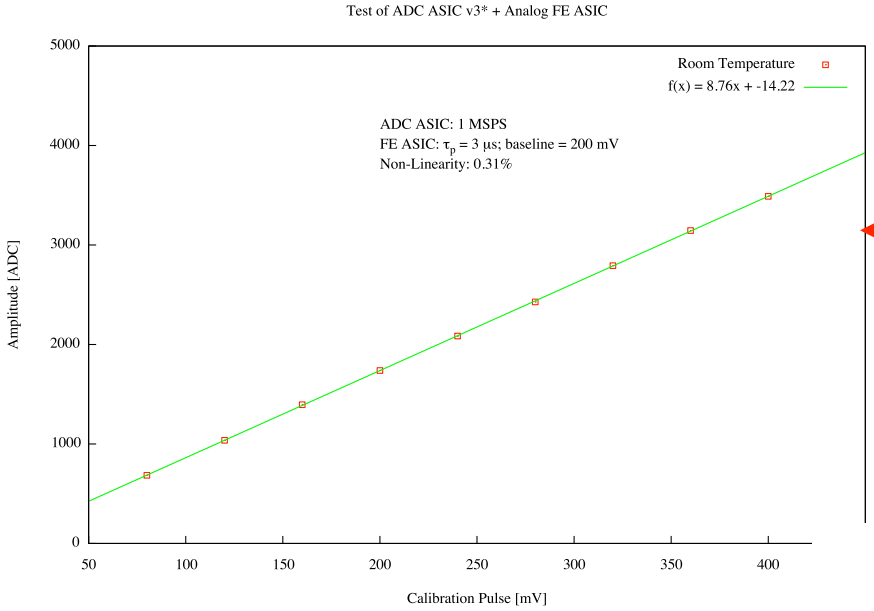
ADC ASIC





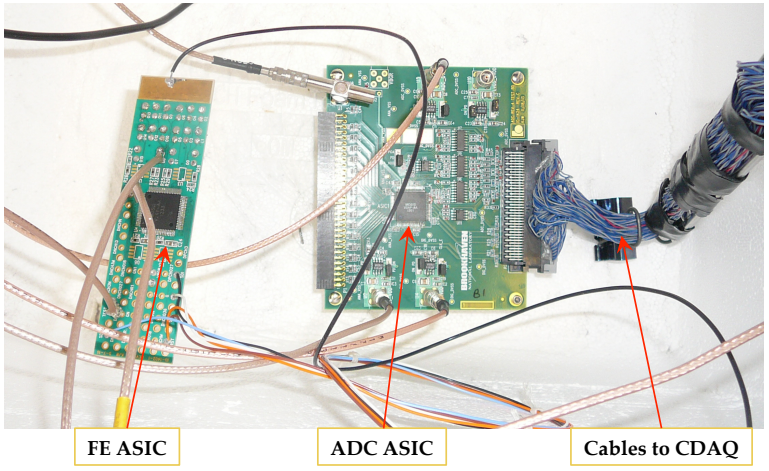
- Effective resolution w.r.t. input referred noise is ~11.6 bits at both 300 K and 77 K
- Differential non-linearity (DNL) is less than 4 LSBs for 99% ADC bins at both 300 K and 77 K
- 10-bit resolution meets the requirement of LBNE

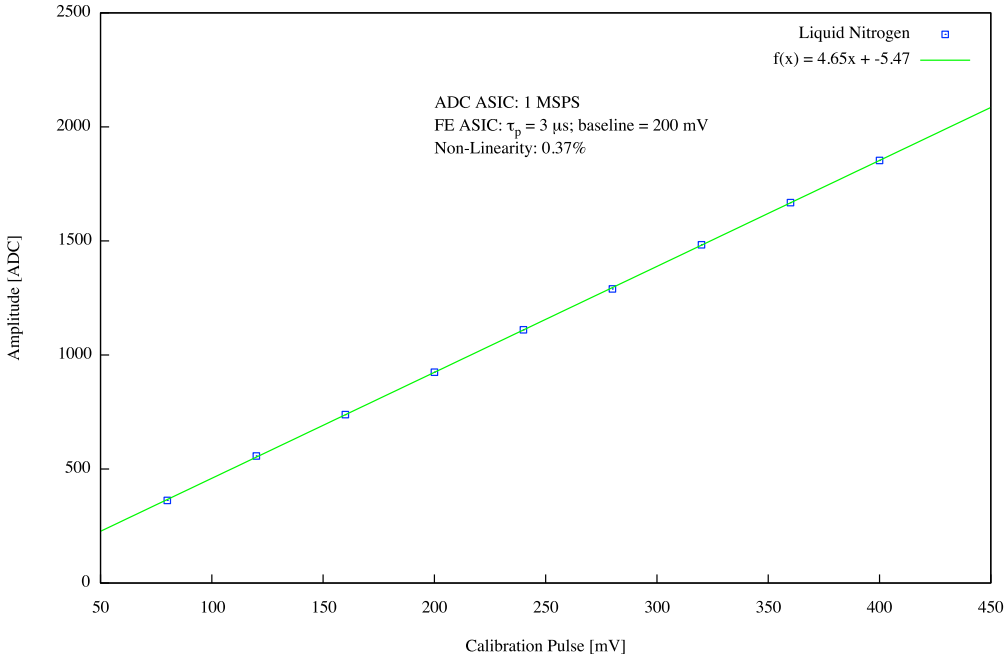
Analog FE + ADC ASICs



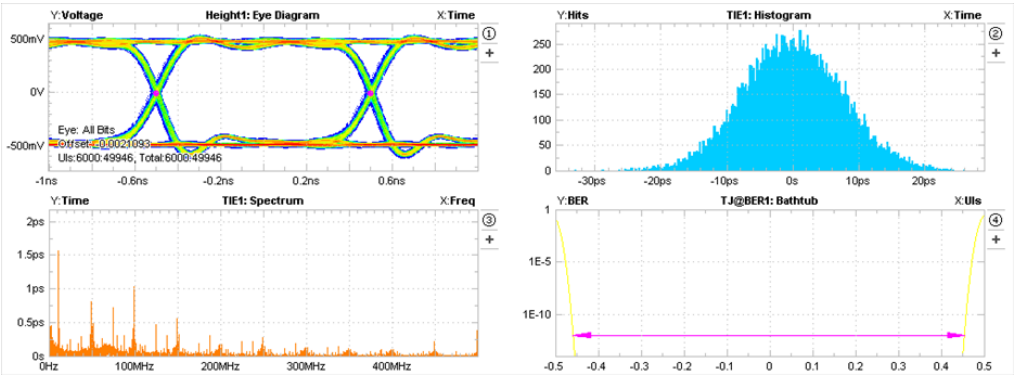
RT: Non-linearity ~ 0.31%

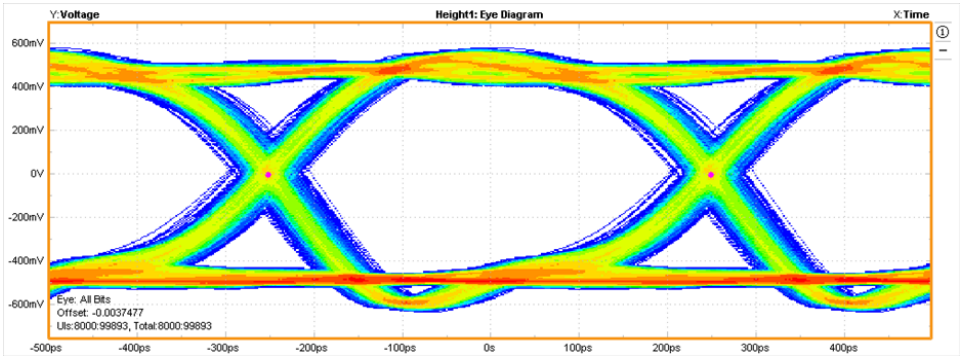
LN2: Non-linearity ~ 0.37%





Cold FPGA

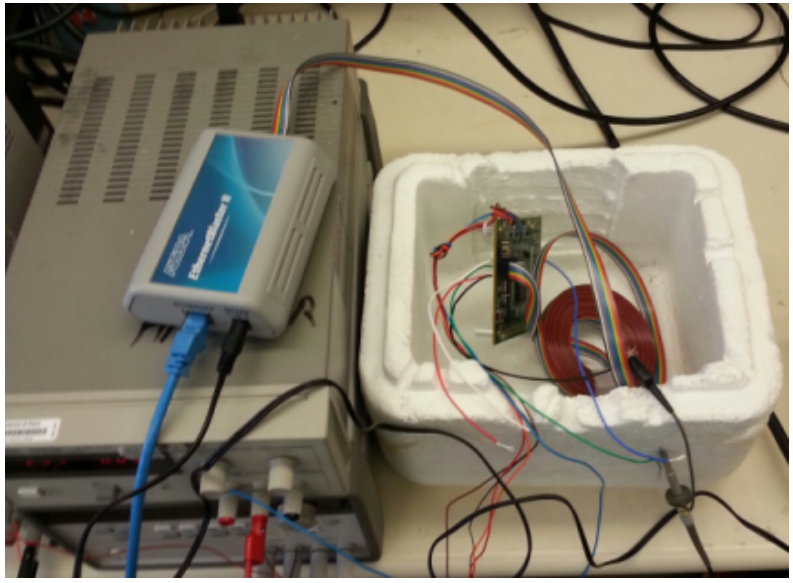




- Test of Cyclone IV GX Transceiver Starter Board in LN_2
  - Transceiver works well at both 1Gbit/s and 2Gbit/s
  - Height
    - 839mV @ 1Gbit/s
    - 823mV @ 2Gbit/s
  - Eye Width
    - 914ps @ 1Gbit/s
    - 357ps @ 2Gbit/s
  - On board SRAM works with BIST
    - 18-Mb SRAM from ISSI IS61VPS102418A-250TQL
    - Cyclone IV GX is running with Nios II processor and utilization of ~80% fabric resources

Cold FPGA

Vendor	Family	Technology	Speed of GTX [Gbps]	# of GTX	Memory [Mbit]	Core Voltage [V]	Status	
ALTERA	Arria GX	90nm	3.125	4 - 12	1.2 - 4.5	1.2	Tested by BNL	✔
ALTERA	Arria II	40nm	6.375	8 - 24	2.9 - 16.4	0.9	Tested by BNL	✗
ALTERA	Stratix II GX	90nm	6.375	4 - 20	1.4 - 6.7	1.2	Tested by SMU	✔
ALTERA	Cyclone IV E	60nm	N/A	N/A	0.3 - 3.9	1.0, 1.2	Tested by BNL	✔
ALTERA	Cyclone IV GX	60nm	3.125	2 - 8	0.5 - 6.5	1.2	Tested by BNL	✔
ALTERA	Cyclone V GX	28nm	3.125	4 - 12	1.2 - 12.2	1.1	Tested by BNL	✗
XILINX	Virtex 5	65nm	6.5	0 - 24	0.9 - 18.6	1.0	Tested by BNL	✗



EPCS4	4Mbit	✔
EPCS16	16Mbit	✔
EPCS64	64Mbit	✗
EPCS128	128Mbit	✗
EPCQ16	16Mbit	✔
EPCQ32	32Mbit	✔
EPCQ64	64Mbit	✔
EPCQ128	128Mbit	✔

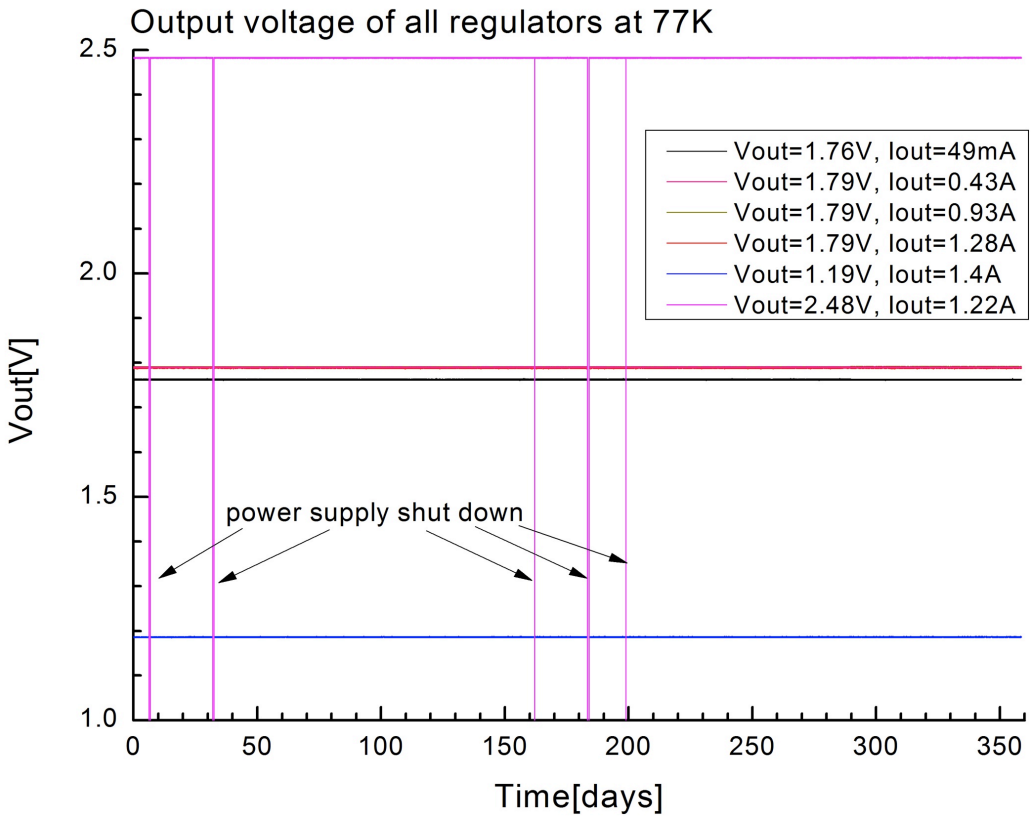
- FPGA Configuration Methods Tested in LN2
  - JTAG through ~50 feet of single ended cable
  - FPGA flash programming through I2C EPCS/EPCQ

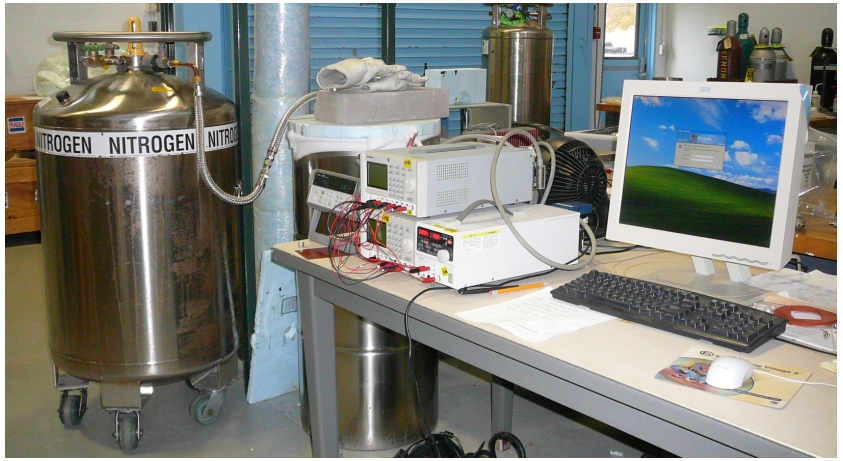
Cold Regulator

Vendor	Part Number	Iout	Vout	Vin	Note
ADI	ADP1708	1A	0.8V to 5.0V	2.5V to 5.5V	
ADI	ADP1741	2A	0.75V to 3V	1.6V to 3.6V	
ADI	ADP124ACPZ-1.8	500mA	1.8V	2.3V to 5.5V	
ADI	ADP130AUJZ-1.8	350mA	1.8V	2.3V to 3.6V	
ADI	ADP170AUJZ-1.8	300mA	1.8V	2.0V to 3.6V	
Globaltech	GS2915L18F	150mA	1.8V	2.3V to 6.0V	
Intersil	ISL9021	250mA	0.9V to 3.3V	1.5V to 5.5V	
Intersil	ISL80113	3A	0.8V to 3.3V	1V to 3.6V	
Linear	LTC3026	1.5A	0.4V to 2.6V	1.14V to 5.5V	
Linear	LTM4616	16A	0.6V to 5V	2.7V to 5.5V	POL Converter
Linear	LTM4619	8A	0.8V to 5V	4.5V to 26.5V	POL Converter
Maxim	MAX8517	1A	0.5V to 3.4V	1.425V to 3.6V	
National	LP38502TJ-ADJ	1.5A	0.6V to 5V	2.7V to 5.5V	
TI	TPS73701	1A	1.2V to 5V	2.2V to 5.5V	
TI	TPS78601	1.5A	1.2V to 5.5V	2.7V to 5.5V	
TI	TPS78618	1.5A	1.8V	2.7V to 5.5V	
TI	TPS78625	1.5A	2.5V	3.0V to 5.5V	
TI	TPS74201	1.5A	0.8V to 3.6V	0.9V to 5.5V	

- Cryogenic test of commercial voltage regulators that could be used to power LAr TPC cold electronics

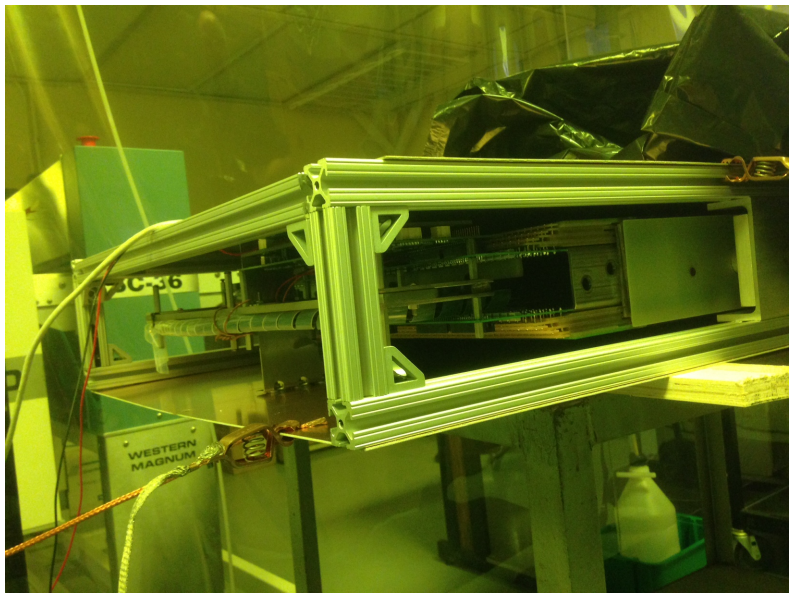
Cold Regulator

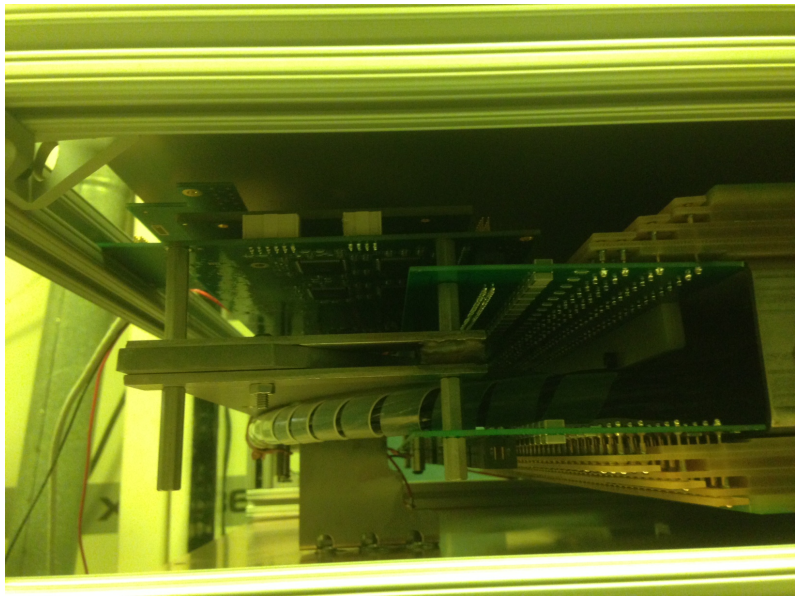


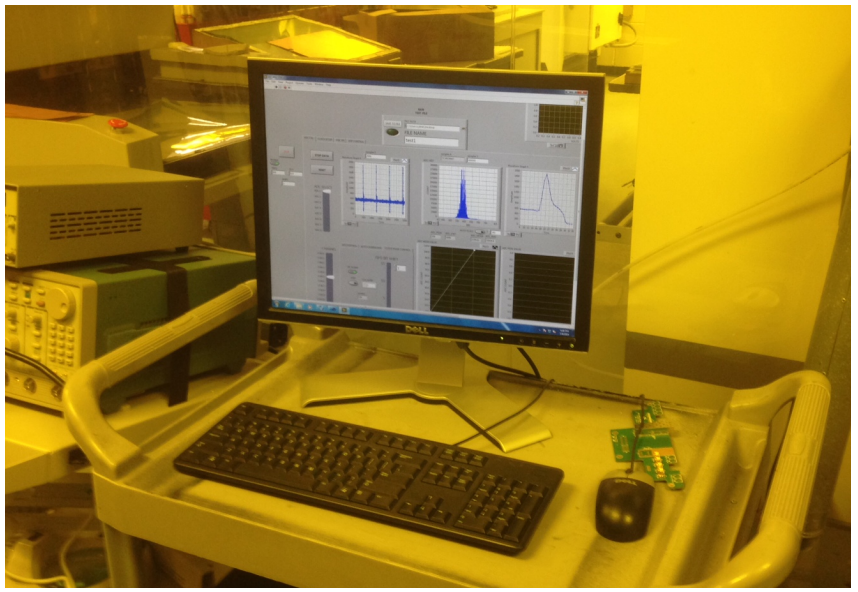


- A long term test of TPS74201 in LN2 has been going on since June 24th, 2013
  - Voltage regulators are working normally, the test is continuing …

Front End Mother Board for LBNE 35 Ton

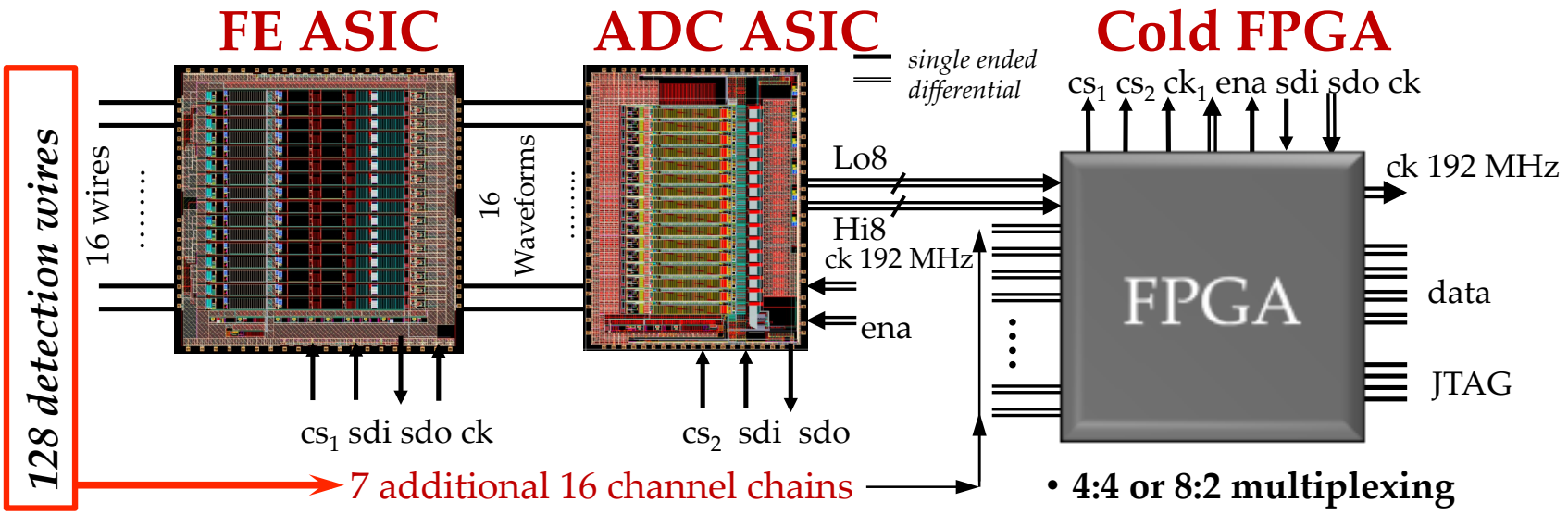






- Front end mother board is being used in the readout chain of APA test at BNL
- Full APA assembly with TPC readout
  - Analog mother board
  - FPGA mezzanine
  - SFP mezzanine
  - Slow control over I2C
  - GbE to a compact DAQ system

Migration from Cold FPGA

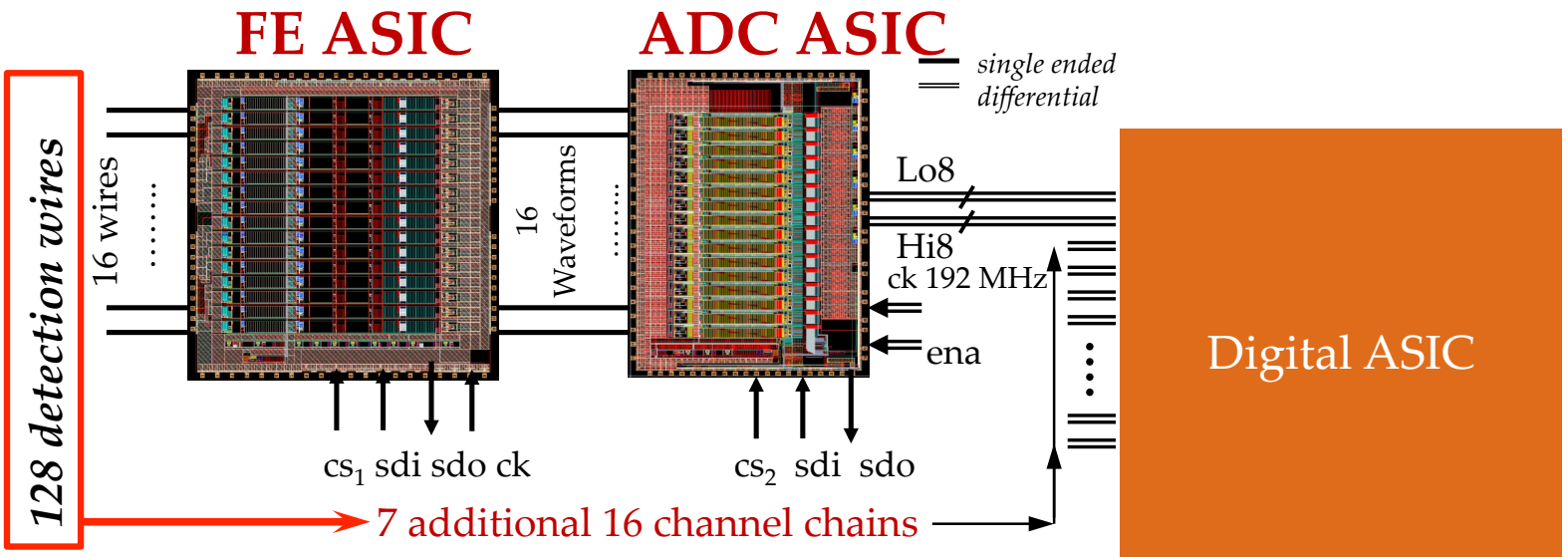


- low-noise analog amplification
- programmable gain, shaping, coupling, …
- charge calibration over all chips, channels and temperatures to 1%

- ADC 12-bit 2MS/s sampling rate
- built-in FIFO
- serialized outputs
- 2 x **8:1 multiplexing**

- **4:4 or 8:2 multiplexing** (total 32:4 or 64:2)
- timestamp
- compression
- zero suppression
- neighbor triggering
- ***support non-reduction transparent mode***
- ***max output data rate 960Mbit/s or 1.92Gbit/s with overhead of 8B/10B***

Migration from Cold FPGA to Digital ASIC



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- ADC 12-bit 2MS/s sampling rate
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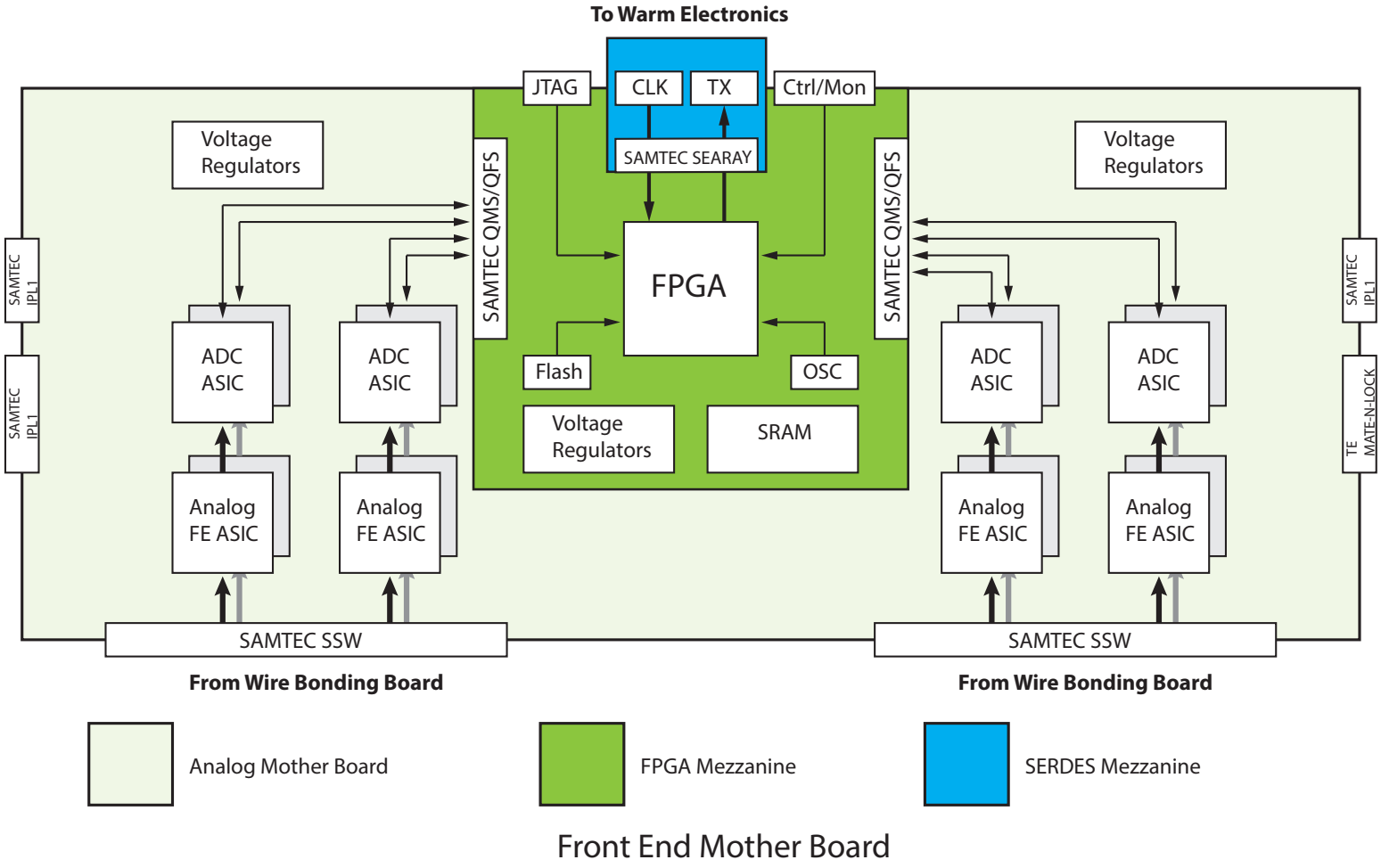
- 2 x **8:1 multiplexing**

See Gregory's talk

Migration from Cold FPGA



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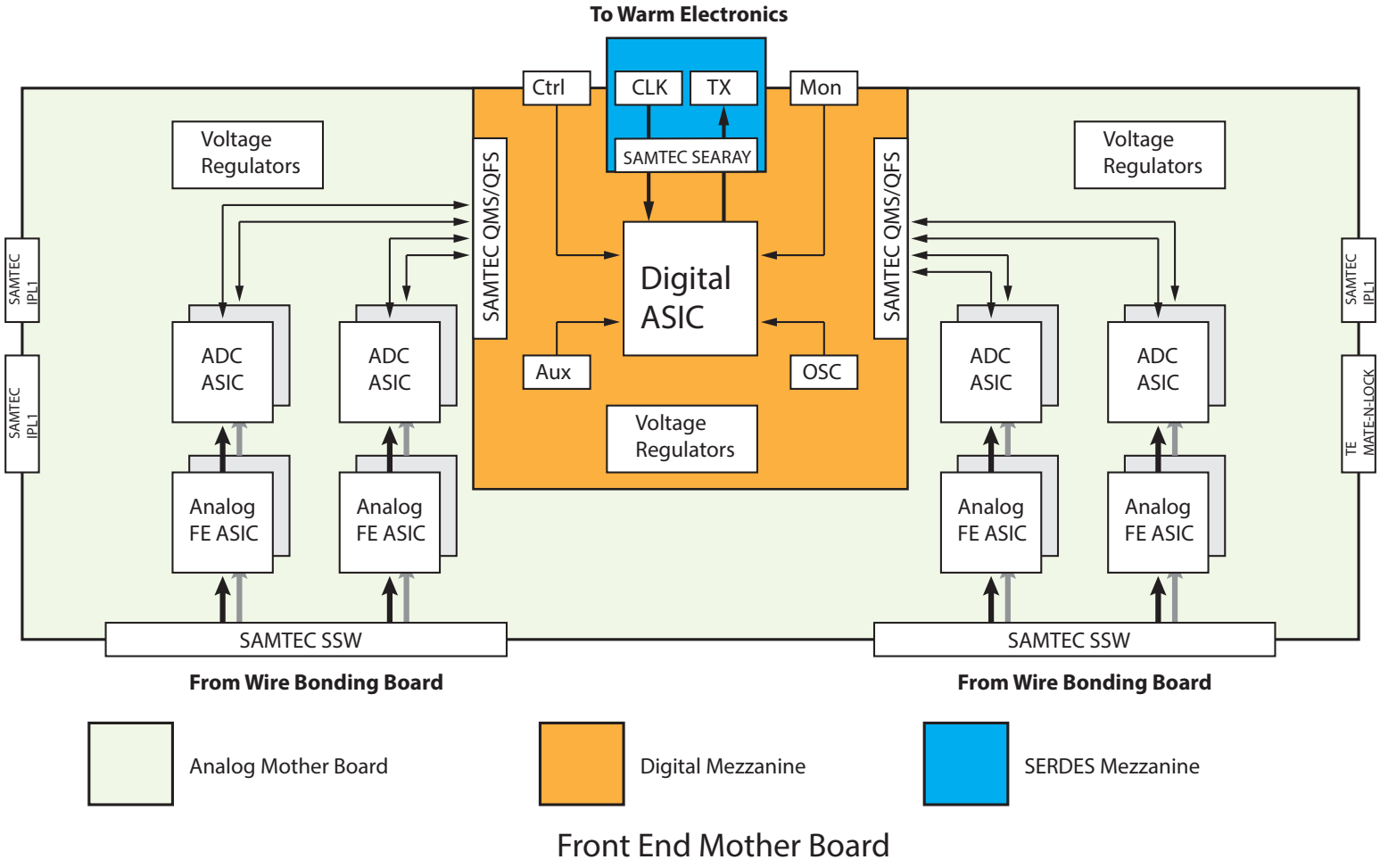


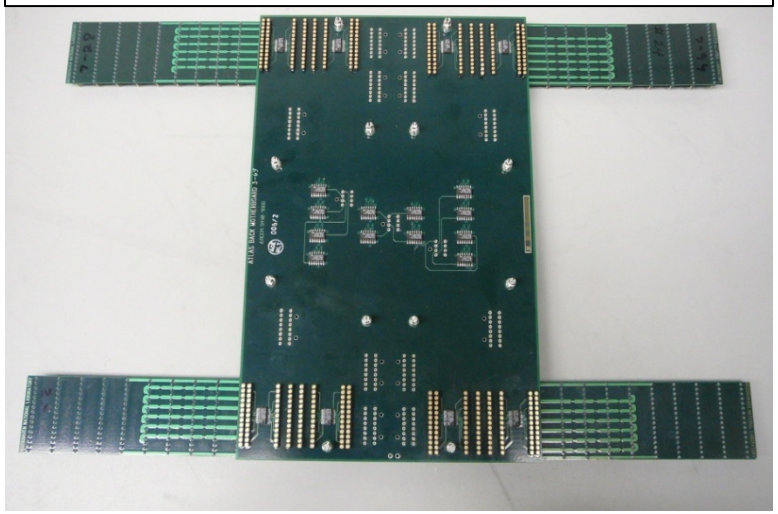
Summary

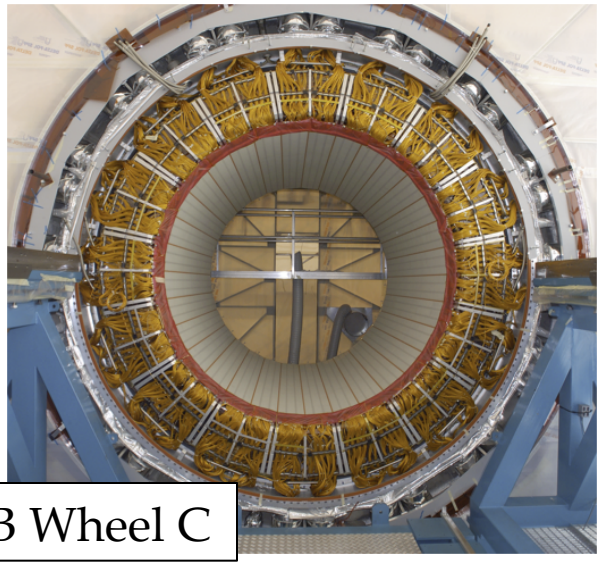
- R&D of CMOS cold electronics started in 2008
  - Analog FE ASIC was the first one developed, following by ADC ASIC development, studies of cold regulator and FPGA etc.
  - In parallel, studies of CMOS lifetime and reliability at 77 K were conducted
    - *"LAr TPC Electronics CMOS Lifetime at 300K and 77K and Reliability under Thermal Cycling," IEEE Trans. on NSci, 60, No: 6, Part: 2, p4737(2013)*
  - Gradually build up a full solution of cold front end readout electronics chain
- Projects using, and potentially will be using cold electronics:
  - MicroBooNE
  - ARGONTUBE
  - CAPTAIN
  - LArIAT
  - LBNE 35Ton
  - LAr1-ND
  - ICARUS, collaboration with CERN
- ***R&D on cold electronics started before most of these projects were anticipated or in existence***

Backup Slides

PCB and Cold Electronics in ATLAS

EMB Mid/Back MB+SB Assembly

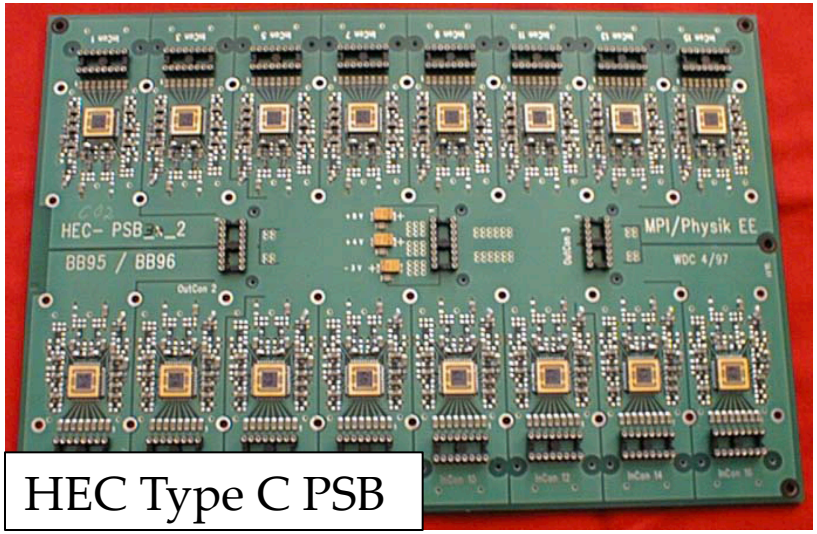




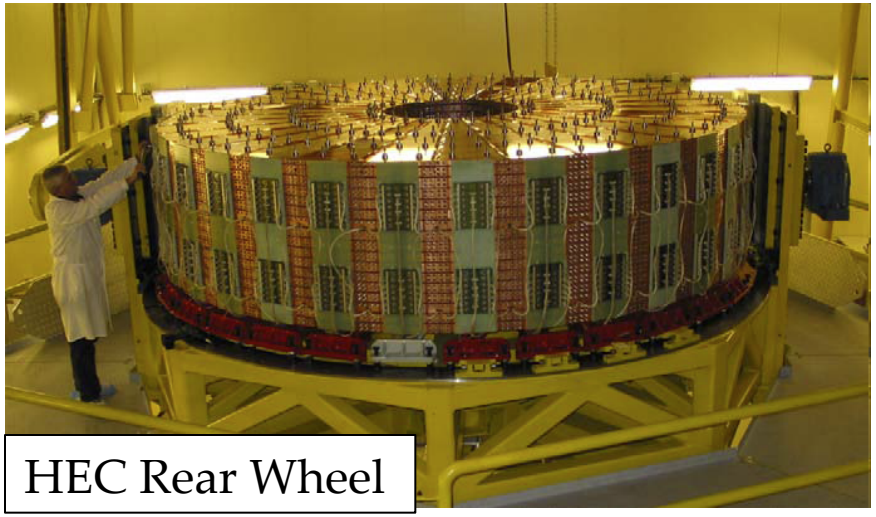
EMB Wheel C

- ATLAS LAr Calorimeter
  - 182,468 readout channels
- EM Barrel Mother Board and Summing Board
  - EMB has ~110,000 detector channels read out by 896 128-ch FEBs
  - 960 Mother Boards, 15 different types
  - 7,168 Summing Boards, 4 different types
  - 20,480 resistor network chips on Mother Boards, 5 different types
  - ~110,000 protection diodes on MB/SB assembly
- EM Barrel Calorimeter has been cooled down since 2004
  - Operation: 10 years so far
  - MB/SB will remain in operation without upgrade for HL-LHC

PCB and Cold Electronics in ATLAS



HEC Type C PSB


HEC Rear Wheel

- ATLAS LAr Calorimeter HEC preamplifier ASIC based on GaAs
  - HEC has ~5,600 detector channels read out by 48 128-ch FEB
  - 320 PSBs installed on HEC wheels, 5 different types
  - Total ~35,000 cold preamplifier channels, each preamplifier ASIC has 8 channels
- HEC Calorimeter has been cooled down since 2005
  - Operation: 9 years so far
  - HEC cold electronics will remain in operation, the need for upgrade will be determined by radiation effects in HL-LHC

LBNE Front-end Electronics

- Readout chain ASICs are integrated with the TPC electrodes in LAr to minimize the capacitance and noise
- On chip **digitization** to convert to digital signals inside detector cryostat
- **Multiplexing** to high speed serial link, to reduce cable plants, minimize outgassing, make possible the scalability to larger detector volumes
- **Cold FPGA** to house the flexible algorithms for data processing and data reduction
- Industry standard serial link interface to connect directly to back end system minimizing conventional DAQ hardware

Summary

- Readout electronics developed at BNL for low temperatures (77K-300K) is an enabling technology for noble liquid and mixed phase detectors for neutrino and dark matter research.
- Cold electronics decouples the electrode and cryostat design from the readout design. With electronics integral with detector electrodes the noise is independent of the fiducial volume (signal cable lengths), and much lower than with warm electronics.
- Signal multiplexing results in large reduction in the quantity of cables (less outgassing) and the number of feedthroughs/ cryostat penetrations.
- MicroBooNE will be the first running experiment instrumented with CMOS cold electronics
- Full cold readout chain with FE ASIC, ADC ASIC and FPGA being prototyped for the “35 ton” and being proposed to SBN program