TDAQ for Liquid Argon Detectors

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- This report is a collection of ideas from discussions that I have had with many people in both the LBNE and NOvA communities

- These include G. Barr, K. Biery, M. Graham, J. Klein, R. Kwarciany, R. Rechenmacher and R. Van Berg

- My apologies to anyone that I have forgotten

- This is NOT a report on a design for the far detector

- The title is called TDAQ because the trigger and DAQ are tightly coupled in this system

Outline

- Data Rates
- Triggers
- System Architecture
- Timing System
- Event Building

Data Rates

- From C. Thorn
- **Ar^{39}** ~120 KHz/ APA depending on APA size and the drift distance.
    - Mean ionization is ~0.3 MIP and mean range is 0.28 mm
- **Kr^{85}** ~30 KHz/ APA
    - Mean ionization is ~0.4 MIP and range is 0.39 mm
- Low noise and good zero suppression should allow a trigger rate of a few KHz or less

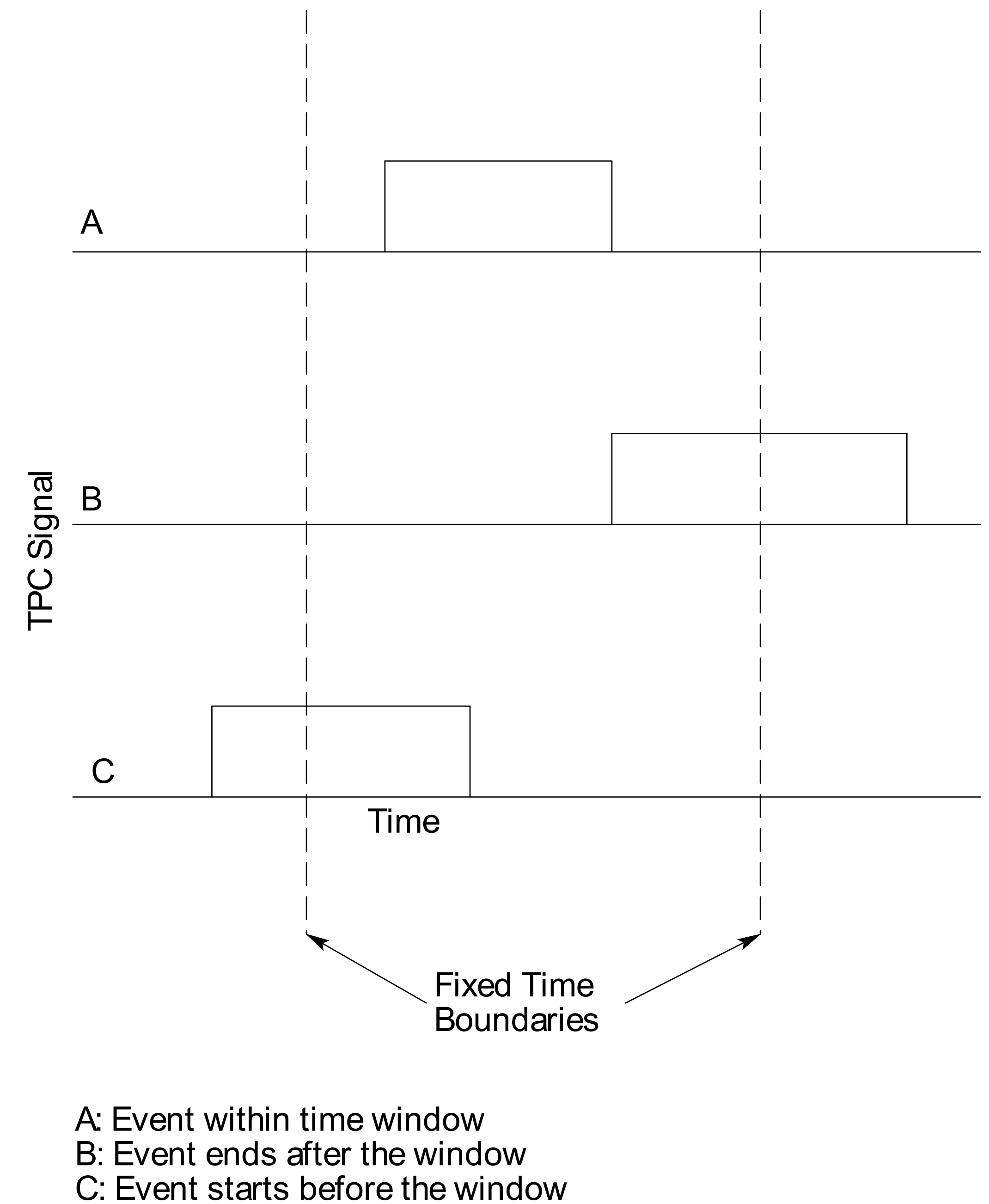
Triggers

- Low rate allows the use of either a hardware or software trigger
  - Hardware trigger is what most experiments use.
    - Specialized hardware searches for patterns in the various detector elements.
    - Pattern match causes a full detector readout
    - Requires temporary data storage while trigger decision is being made
    - Major changes often require new hardware

Software Triggers

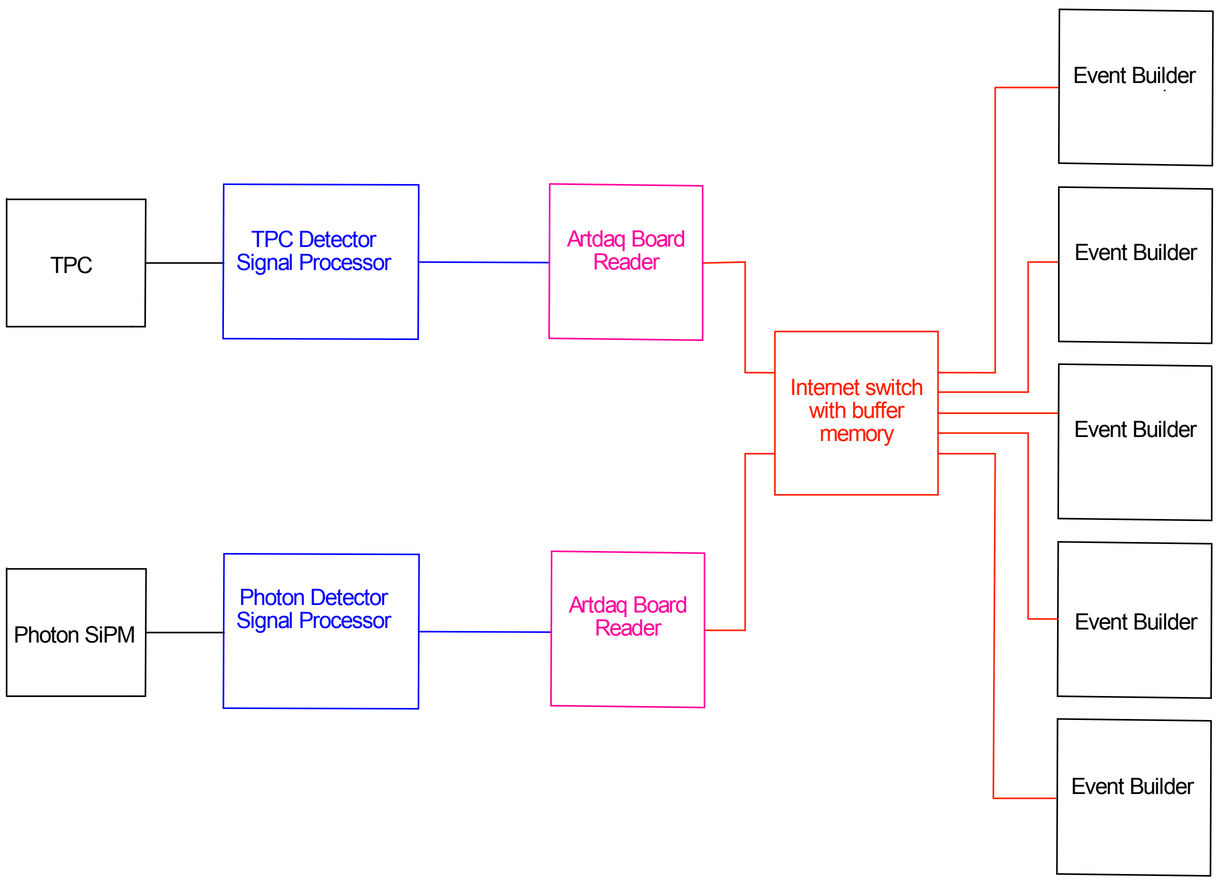
- All zero suppressed data for one or more drift times is sent to a single processor
- Entire event is used for event selection
- This is best described as a filter process rather than a trigger

- A hardware trigger defines the start time of an event
    - Event data is simply read out from this start time.
- Software filters do not have a starting time so an event can be split across time boundaries.
    - If no photon signal, start time must be reconstructed from TPC data
- Hardware triggers still require time stamping and matching
    - Matching to accelerator spill
    - Continuous non zero suppressed reading on all channels for detector studies etc.
    - Many second long records for a few channels for diagnostics



System Architecture

- Four Main elements
  - Detector Signal Processor
    - Zero suppression
    - Data time stamping
  - ArtDAQ board reader
    - Assembles data packets for event builder
  - Internet switch with buffer memory
  - Event Builder
    - Event data processing and filtering



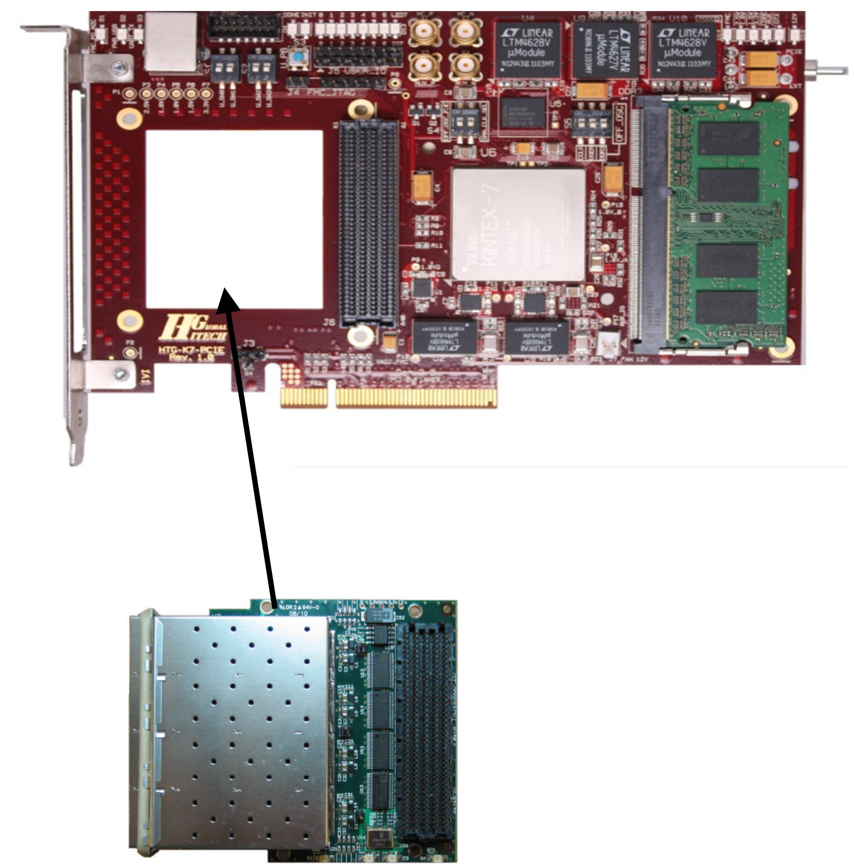
GPS timing links are suppressed for clarity

TPC Signal Processor

- Can be either in the LAr, at the feedthrough port or in a counting house
- No need for it to be cold
  - 128 channels of 12 bit ADC digitizing at 2 MHz generate 3 Gb/s
  - Single 20 meter copper cable is adequate
  - 20 cables per TPC
  - Power, bias voltage, clock and control dominate the cable count

TPC Signal Processor

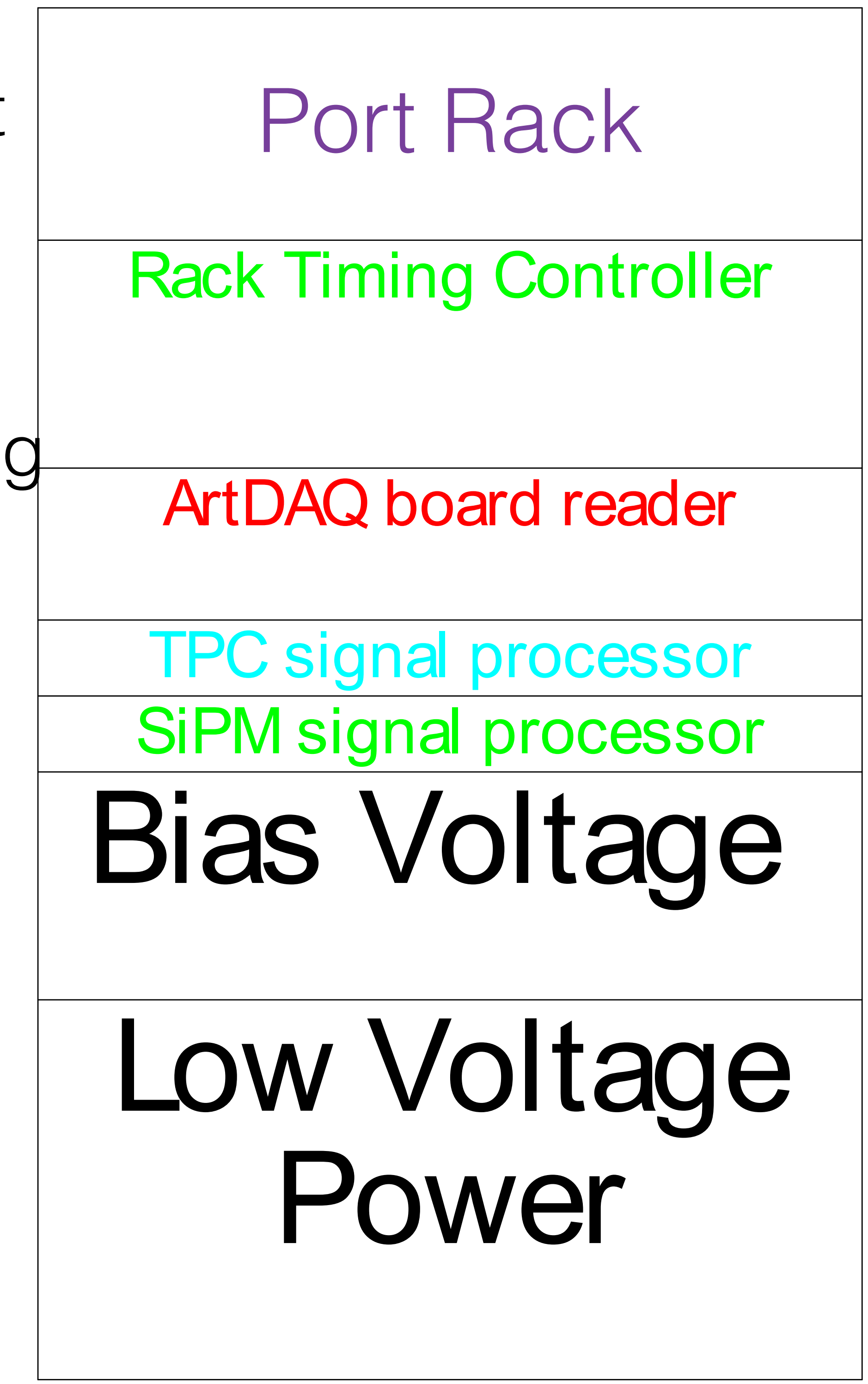
- Must be FPGA based device
  - Need ~20 channels of 3 Gb/s input data plus timing input
- Provides zero suppression and time stamping
- Provides diagnostics and other test features
- Custom design is currently needed for the ~20 lines per TPC
  - PCIE cards are nearly competitive



PCIE card with Kintex 7 FPGA and eight 10 GB/s ports

Photon Signal Processor

- Custom board for low noise SiPM readout
- Located at the signal port for low noise
- Board reader could be remote but locating a computer at the port has several uses
    - Board reader for Photon and TPC processors
    - Processor for slow controls and monitoring
    - Timing system control and monitoring



Internet Switch

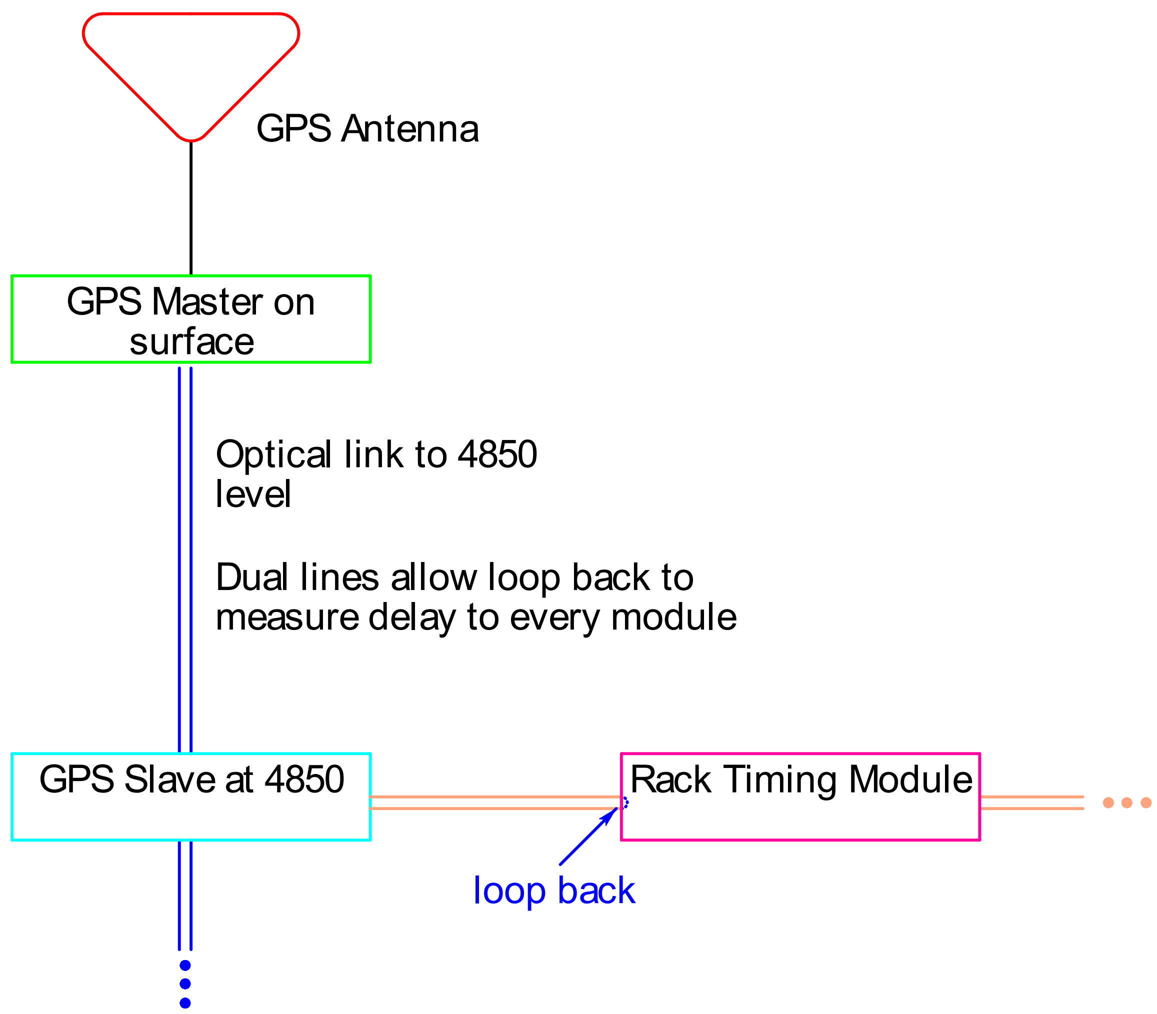
- Commercial Switch with buffer memory
    - 10 Gb/s ports
    - Buffer memory stores packets if they arrive faster than they can move through the switch
    - Eliminates any need for buffer management in the board readers
- Event builders are located on the surface so switch output drives long distance fiber lines.

Timing

- Far detector timing system is needed for several tasks
  - Need link to accelerator to know when the fast spill occurs
  - Need link to world time to correlate super nova events
  - Need to correlate data between detector elements
- Time stamp should be unique for entire run of the experiment
  - Choose 56 bit time stamp with 30 ns least count
  - 30 ns is adequate for photon system
  - 68.5 year duration

Timing System

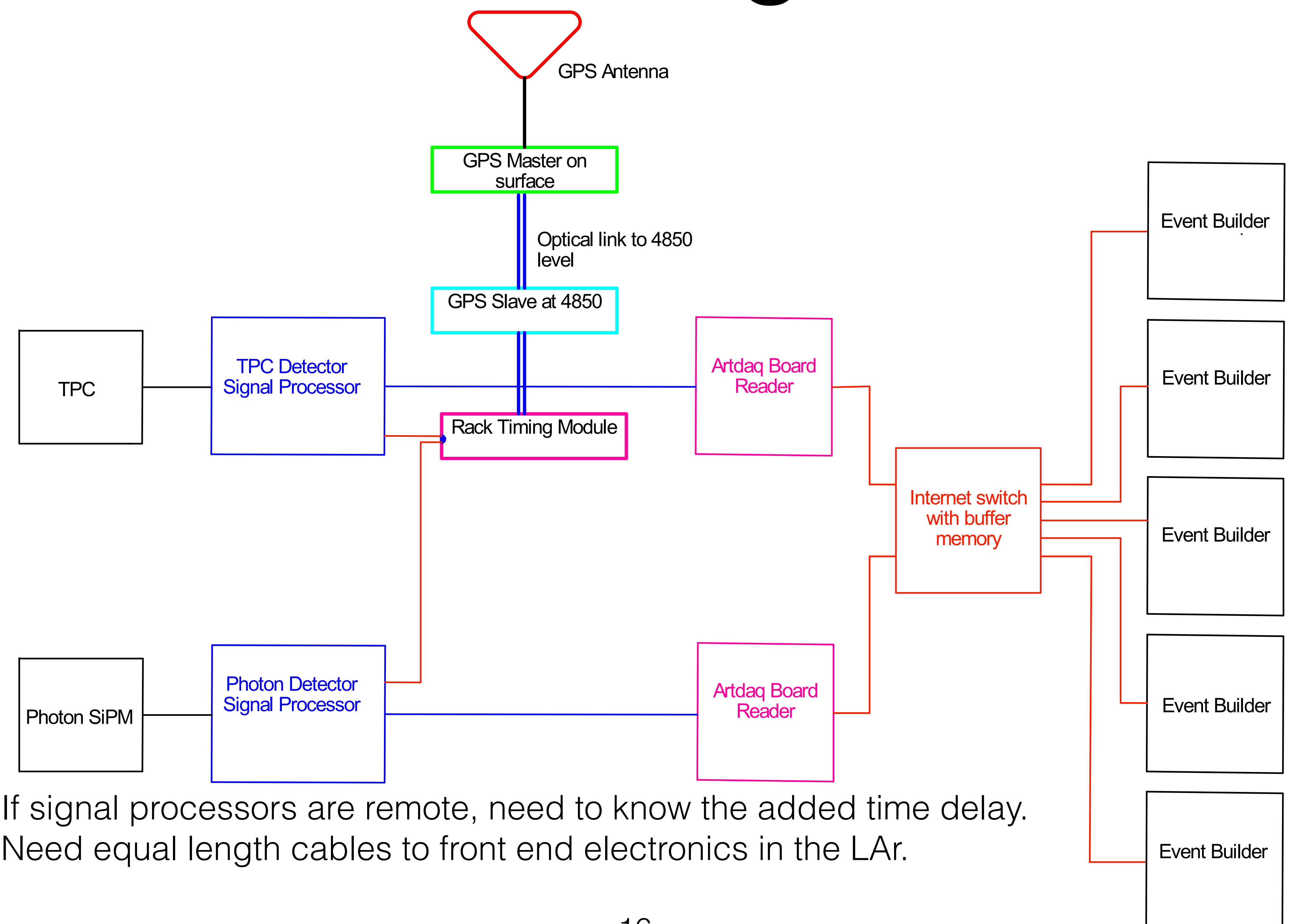
- Similar to NOvA system
- Surface antenna and timing master
- Optical link to 4850
- Optical daisy chain to more slaves
- Copper to timing unit located at every port
- Loop back in all modules to measure time delay



Setting the Time

- Works like the old telephone time system
- Preloads a digital time number into all timing registers
- Issues a chime signal that loads the time number into the active time register
- Easy to compensate for cable delay
  - Add internal (digital) delay at each rack module so that the total delay at every rack module equal the longest delay.
  - Load the desired time into every module
  - Master subtracts the delay from the desired time and sends the chime at the earlier time

System Architecture with Timing



If signal processors are remote, need to know the added time delay.
Need equal length cables to front end electronics in the LAr.

Event Building

- Define a Nano slice as one ADC sample time (~6 ns for photon or ~500 ns for TPC)

- Define a Micro slice as a readout block length

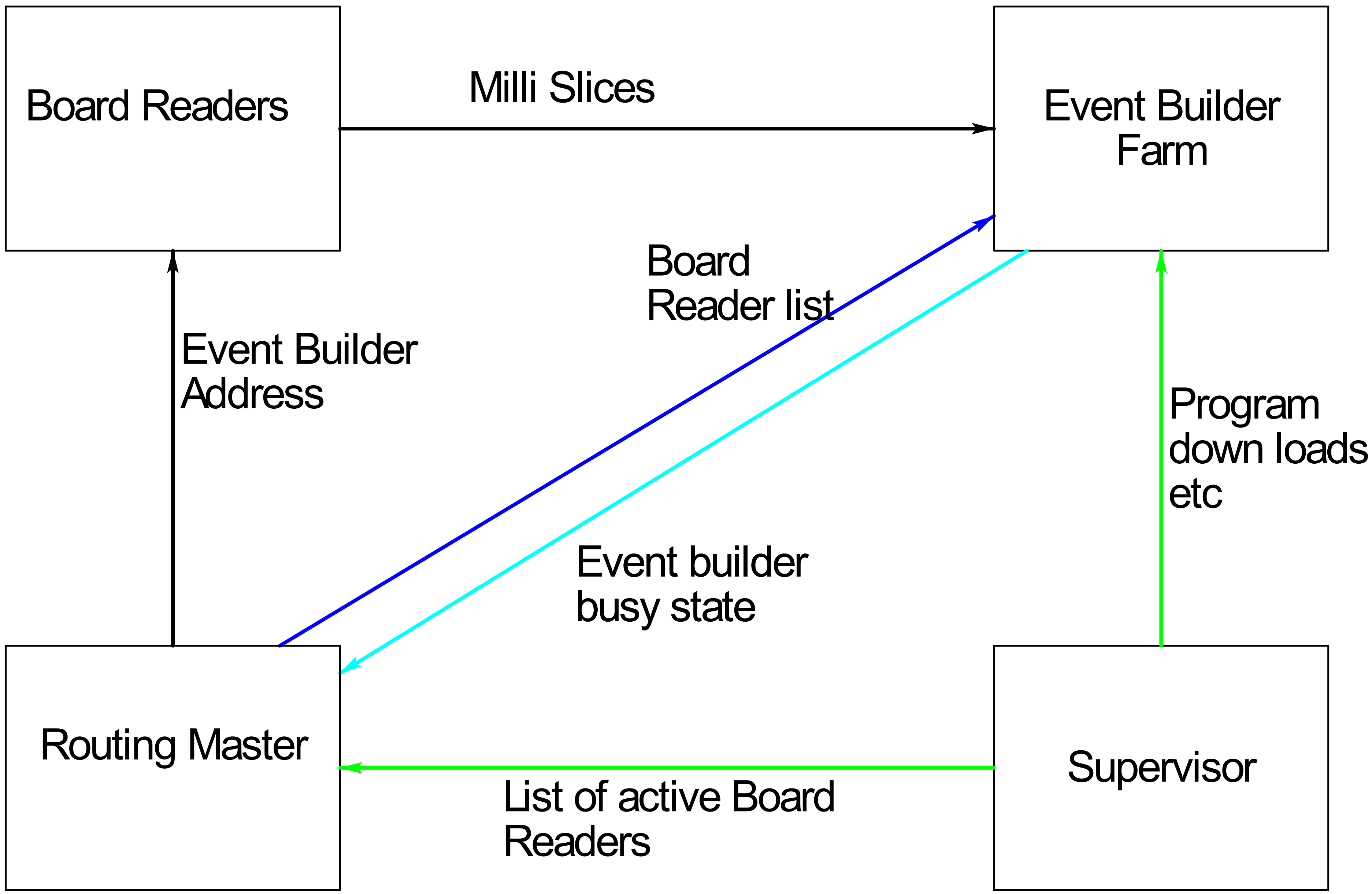
    - For example, a 1 K block for the photon system would be 6 μs so a micro slice would be 6 μs.

- A Milli slice is an ArtDAQ board reader transmission block to the event builder

Board Reader

- Board reader gathers micro slices from several signal processors
- It has a fixed size milli slice with a specific start and stop time that it is filling
- It gathers micro slices until it has received an end-of-micro-slice signal from all of its channels for all micro slices in the current milli slice
- It then sends its data to the next event builder process

Data Routing to Event Builder



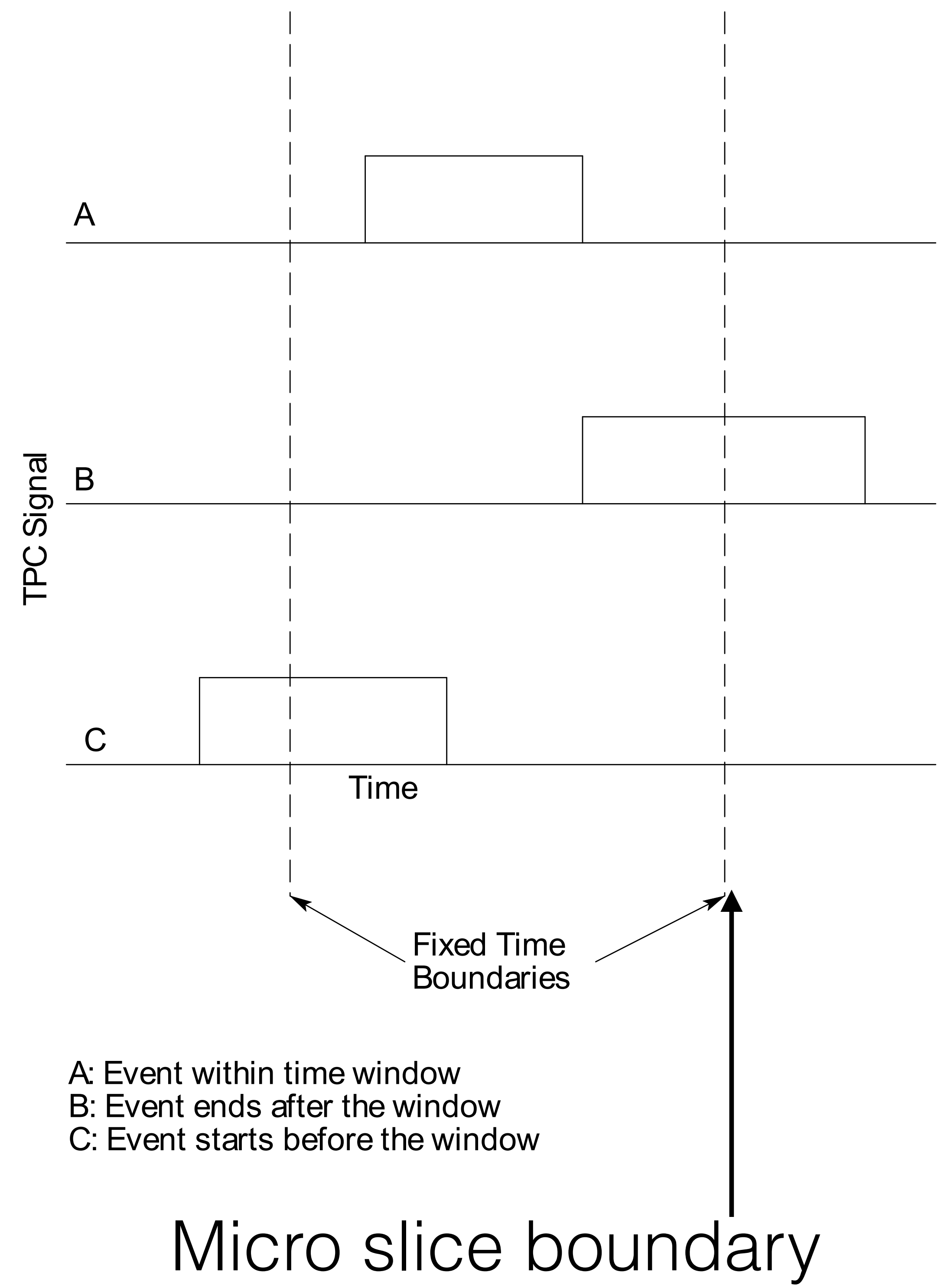
Round robin scheduling eliminates the routing master.
Supervisor connects directly to board readers

Event Builder

- Waits for a milli slice from all board readers
    - An empty milli slice is sent if there is no data
- Searches data for an event start and looks for suitable data pattern
- If found, it packs the data into a data block suitable for Art processing and sends it of to the next filter process

Data Blocks

- A milli slice time block must be an integral number of micro slices
  - Board reader assembles micro slices into a milli slice
- One time stamp per data block (record)
- Blocks need not fill a micro slice but they cannot be longer than a micro slice
  - Line A shows a short block contained in a micro slice
  - Lines B and C require record breaks at the micro slice time boundaries



Multichannel Data Blocks

- Data from multiple channels can be in a data block but each requires its own time stamp
    - Only one channel can cross a time stamp boundary
- An end-of-data flag is required when all data for a given micro slice has been sent to the board reader
    - Tells board reader that it has all the data for this micro slice

Zero Suppression

- Zero suppressed data most likely requires some leading digitizations that are below threshold.
  - Time stamp must reflect this earlier time
  - Simple way to do this is to implement a circular buffer with read pointer lagging write pointer
  - Time stamp is then current time minus the lag time
- Nearest neighbor read out adds additional complexity
  - Track angle may cause neighbor data to be ahead or behind of the main channel
  - One possibility is to have a second circular buffer with a lag time equal to the largest possible time difference between the two channels

Summary

- Software trigger looks feasible for a big LAr TPC
- The ArtDAQ readout system should meet the detector requirements
- A GPS based timing system similar to the NOvA design should work well
- Time stamps and equal length time blocks are needed for either hardware or software triggers