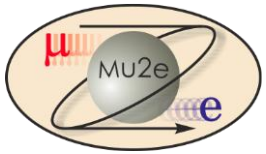
Fermilab

U.S. DEPARTMENT OF ENERGY Office of Science

Mu2e Tracker Front End Electronics



Vadim Rusu

Front End Electronics L3 Manager

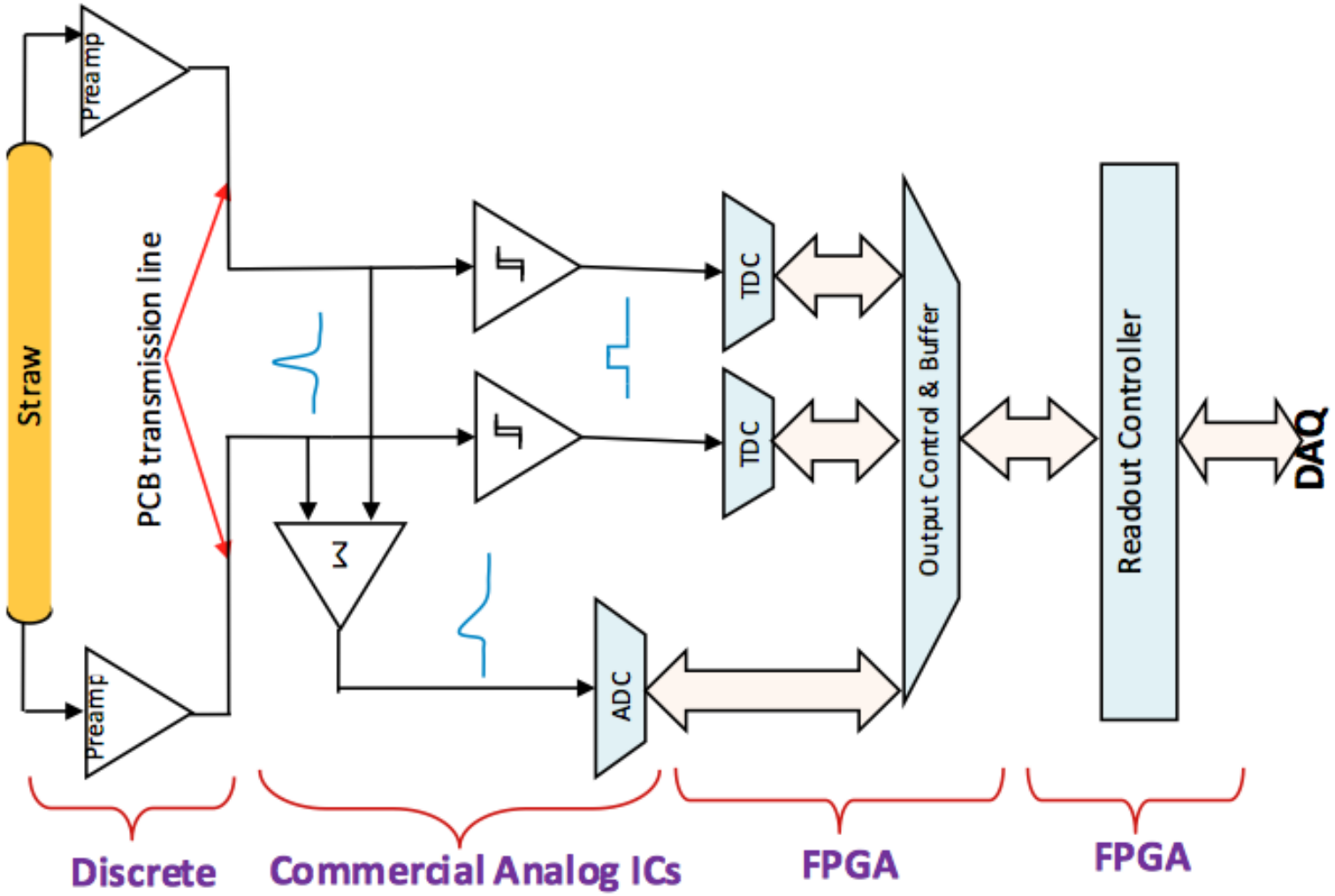
7/8/2014

Tracker Front End Requirements

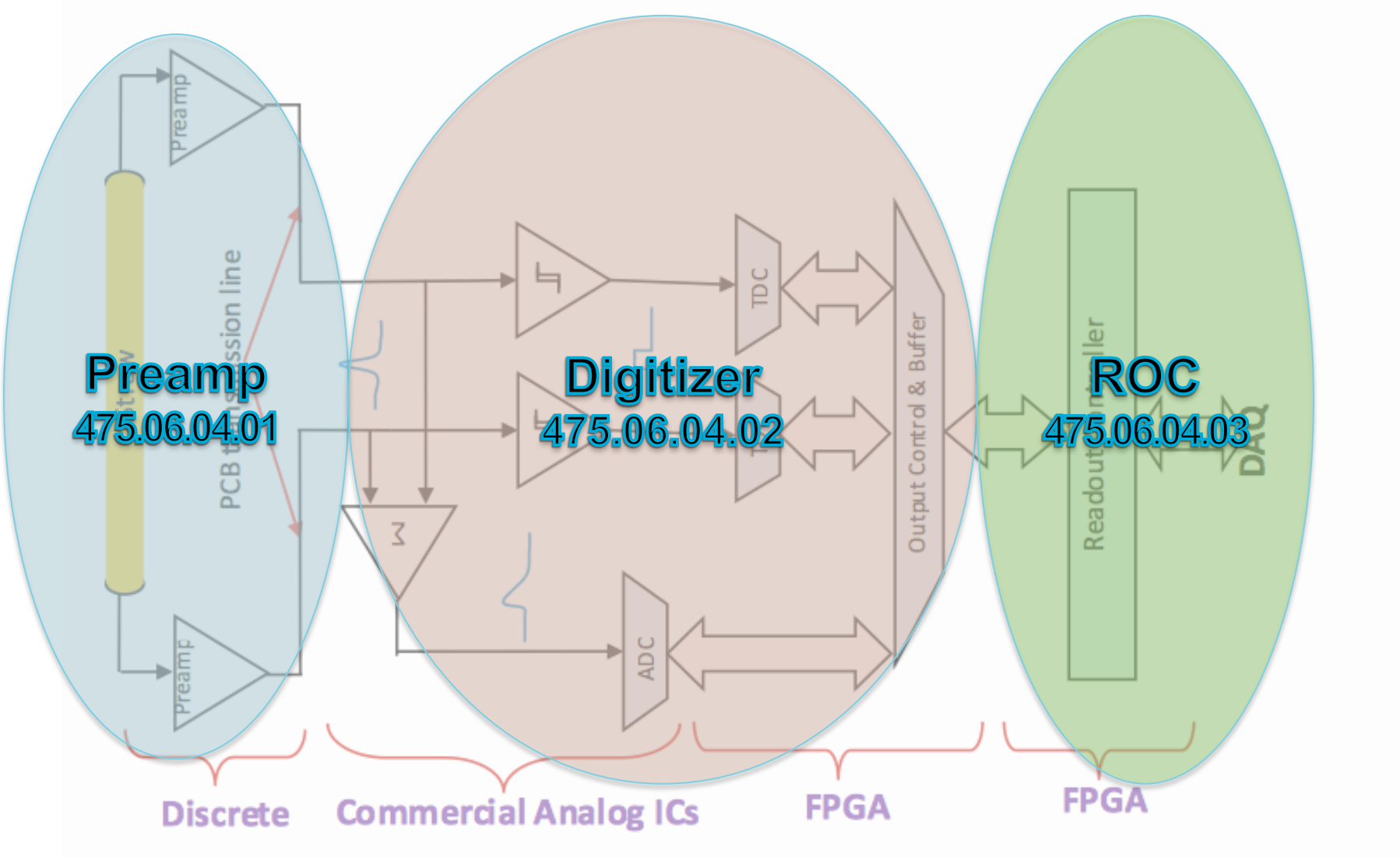
- Amplification and digitization of the straw signals
- Transmit the digitized data to DAQ
- Record both ends of the straw (time division – 3cm resolution)
- Measure pulse height for dE/dx
- Supply HV to anode wires (and HV disconnect)
- Run triggerless mode (soft trigger may be implemented at the DAQ level)
- B field perturbation <1G in the active region
- Rad hard (2×10^{12} n/cm^2)
- 10kW power (limited by CDF SUVA cooling system)
- $<12 \times 96$ dead channels in 5 years at 90% CL

Doc-db 3879

Tracker Front End Scheme



Tracker Front End Scheme



Implementation

- Entire electronics chain implemented in commercially available components
  - Reduced risk
  - Reliable cost estimates (manufacturer quotes and catalog)
  - Upgradeable (ride technology wave)
  - Flexibility
    - All key functionalities implemented in FPGAs
    - Reconfigurable

Preamp requirements

- Bandwidth 100-300MHz
- Typical electron pulse >5x noise floor
- Dynamic range x10 typical electron pulse
  - Clip larger pulses to avoid x-talk downstream from large proton pulses
- Shaping – return to baseline <200ns
  - >50% efficiency for typical electron pulse after a typical proton pulse
- >100kOhm R from the HV bus
  - <1nA leakage through blocking capacitor
  - HV remote disconnect

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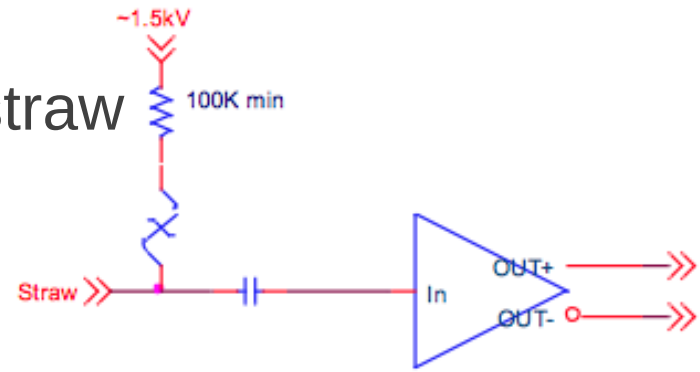
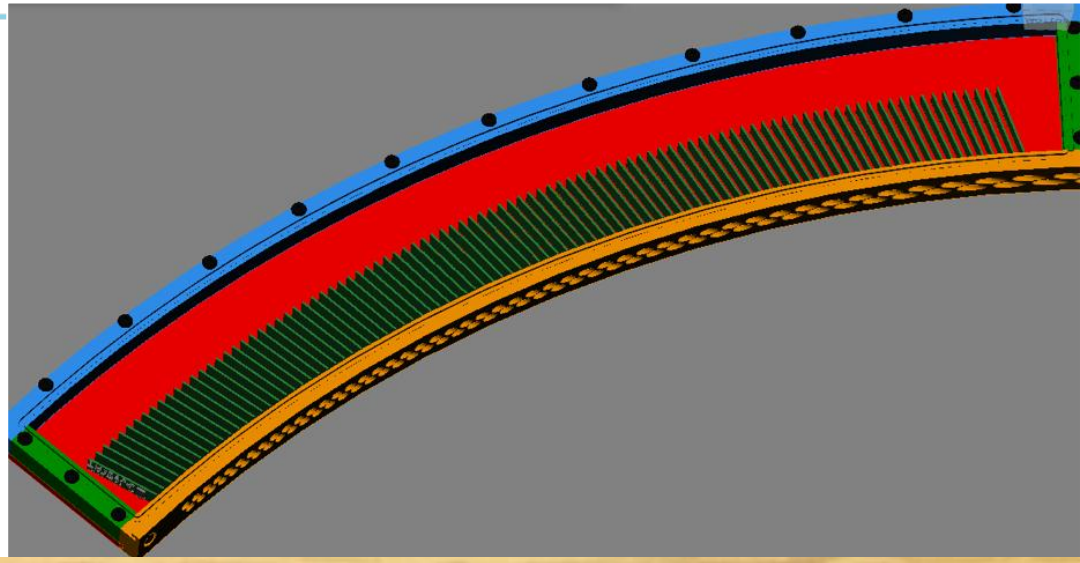
Preamp implementation

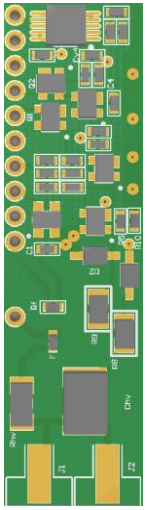
- 46080 preamps (2x straws)
- Small/simple PCBs at the end of the straw
- Low power (~15mW)
- Configurable gain and threshold
- Input stage
  - Low noise/high f_T SiGe technology discrete BJT
  - Active 300Ohm termination to avoid reflections
  - ESD Transient protection
- Output stage
  - Differential output (good CMRR avoids ground loops)
  - Termination and pull-up at digitizer input
- Advanced stage of prototyping



Preamp performance

- 250MHz -3dB point
- 2mV RMS output noise
- 10mV typical electron pulse response
- Dynamic range 150mV
- ~50ns shaping time





Digitizer requirements

- <70ps ΔT resolution (time division)
- 1ns drift time resolution
  - 1700ns range (at least a microbunch)
- 7 bits ADC resolution
  - X10 typical electron pulse range
- 50MS/s sampling rate
- LVDS data to ROC (200Mb/s line)
  - Data to ROC
    - Header, 2x TDC, 8 ADC samples
- 150mW/straw

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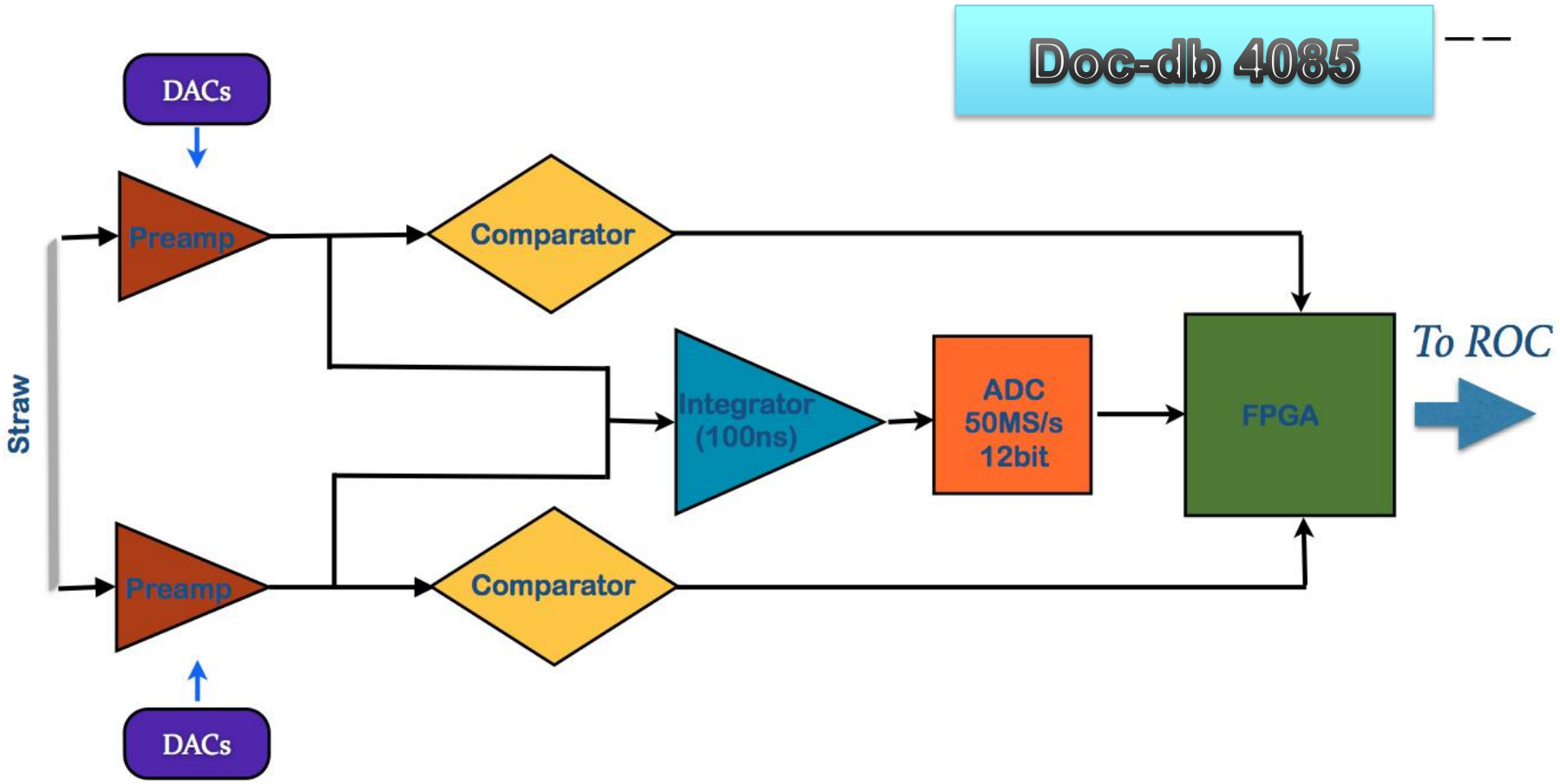
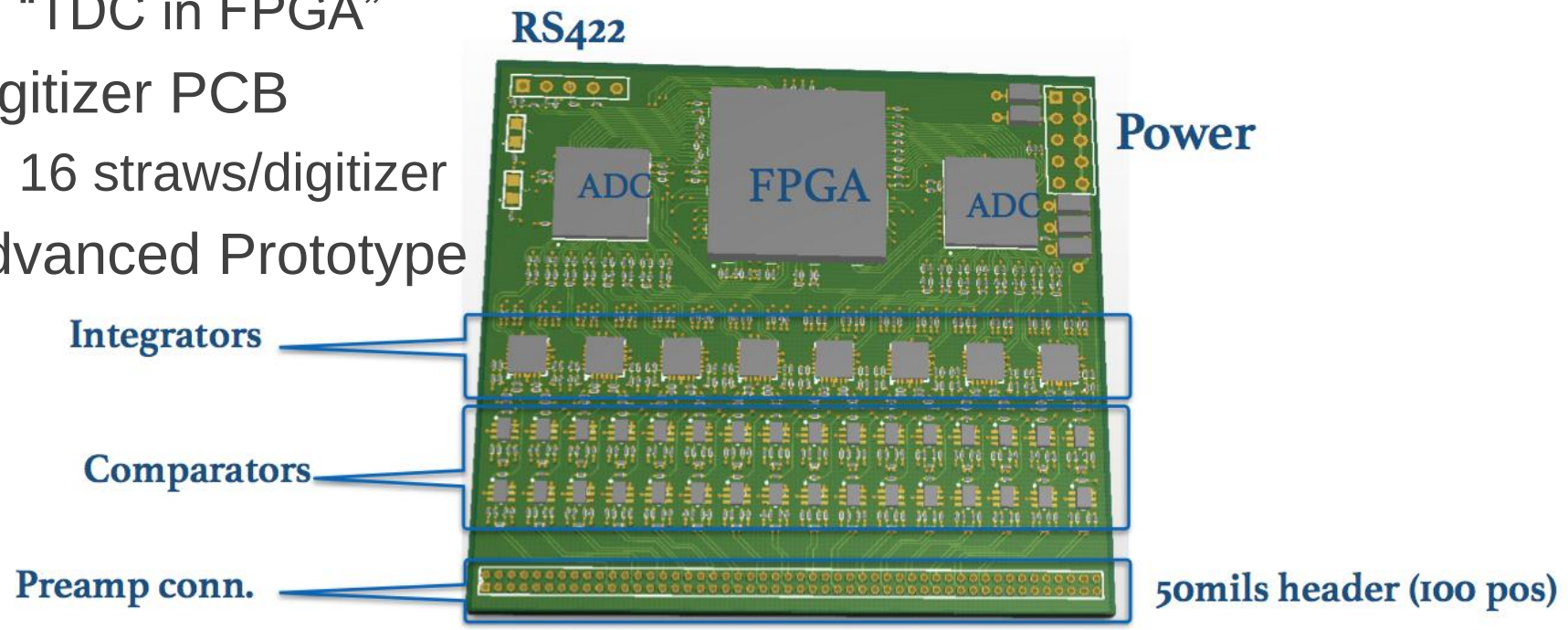
Digitizer scheme



Digitizer implementation

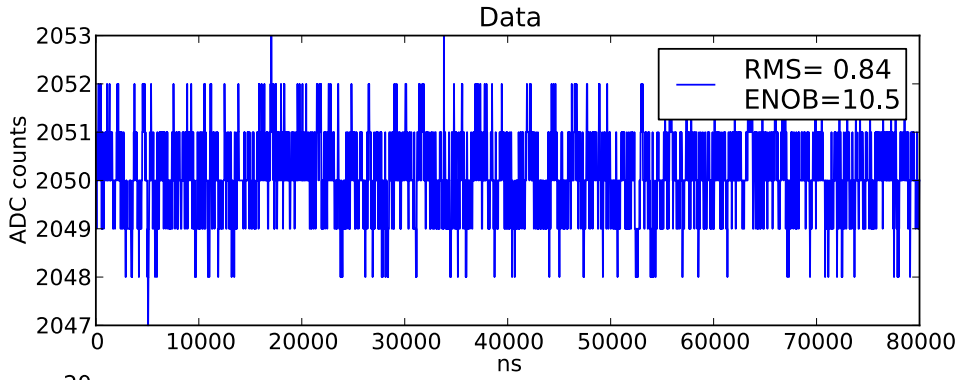
- 46080 TDC channels and 23040 ADC channels
- Commercial off-the-shelf components
  - Fast comparator and shaper
  - ADC (Maxim19527)
  - “TDC in FPGA”
- Digitizer PCB
  - 16 straws/digitizer
- Advanced Prototype

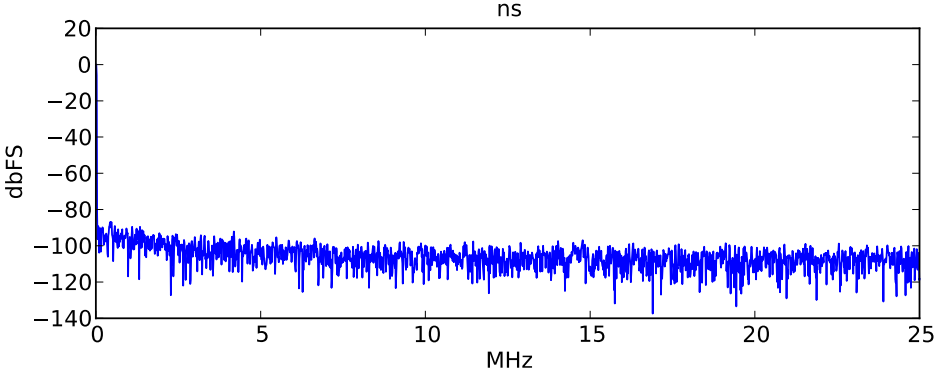
Doc-db 4085

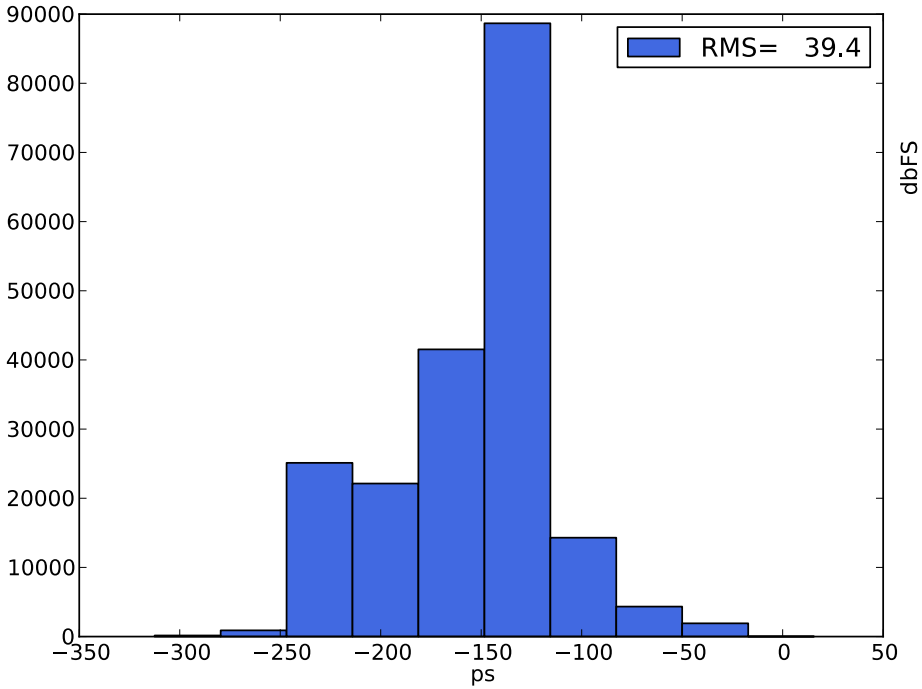


Digitizer performance

Test bench measurements







Doc-db 4085

Readout Controller Requirements

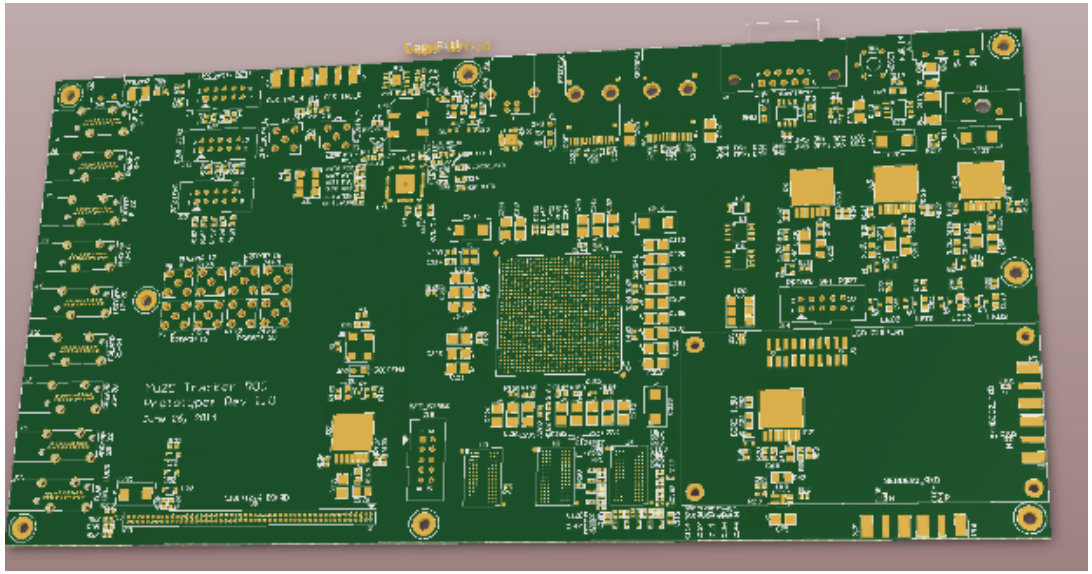
- Received data from Digitizers
- Buffering
  - Continue data transfer in inter-spill time
- Transmits to DAQ
  - 230Mbps each ROC to DAQ
- Relies slow controls to front-end
  - Preamp settings
  - HV control (fuses)
  - Monitor environmental variables

Doc-db 3973

ROC Implementation

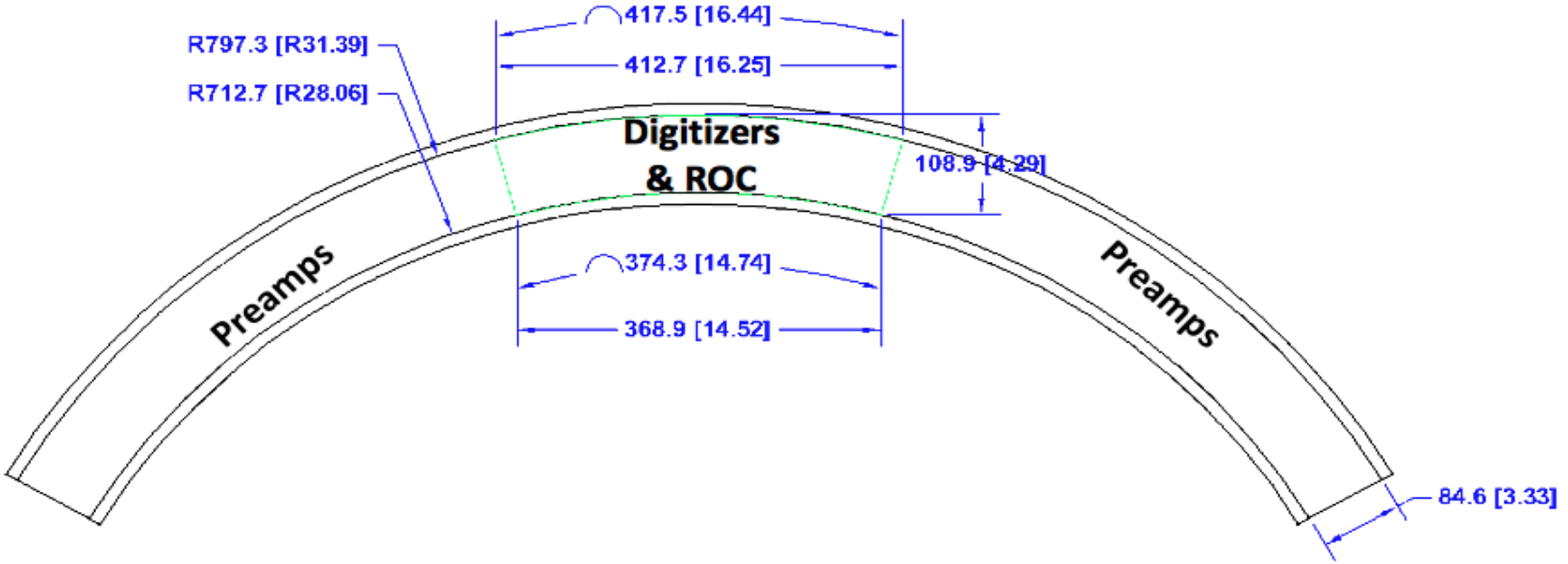
Doc-db 3973

- U. of Houston (Ed Hungerford)
- SmartFusion FPGA (rad hard line from Microsemi)
- DDR3 on board for buffering
- 2.5 Gbps full-duplex fiber optics
  - Ring architecture
- Prototype being manufactured



Infrastructure (Signal transmission)

- Pursuing a long (55”) motherboard
  - Recommendation from Digitizer Review (April 2014)
  - Effectively a transmission line board
    - All components (preamp, digi, ROC) mezzanines
    - HV, soft controls on board
  - Rice U. (Marj Corcoran)

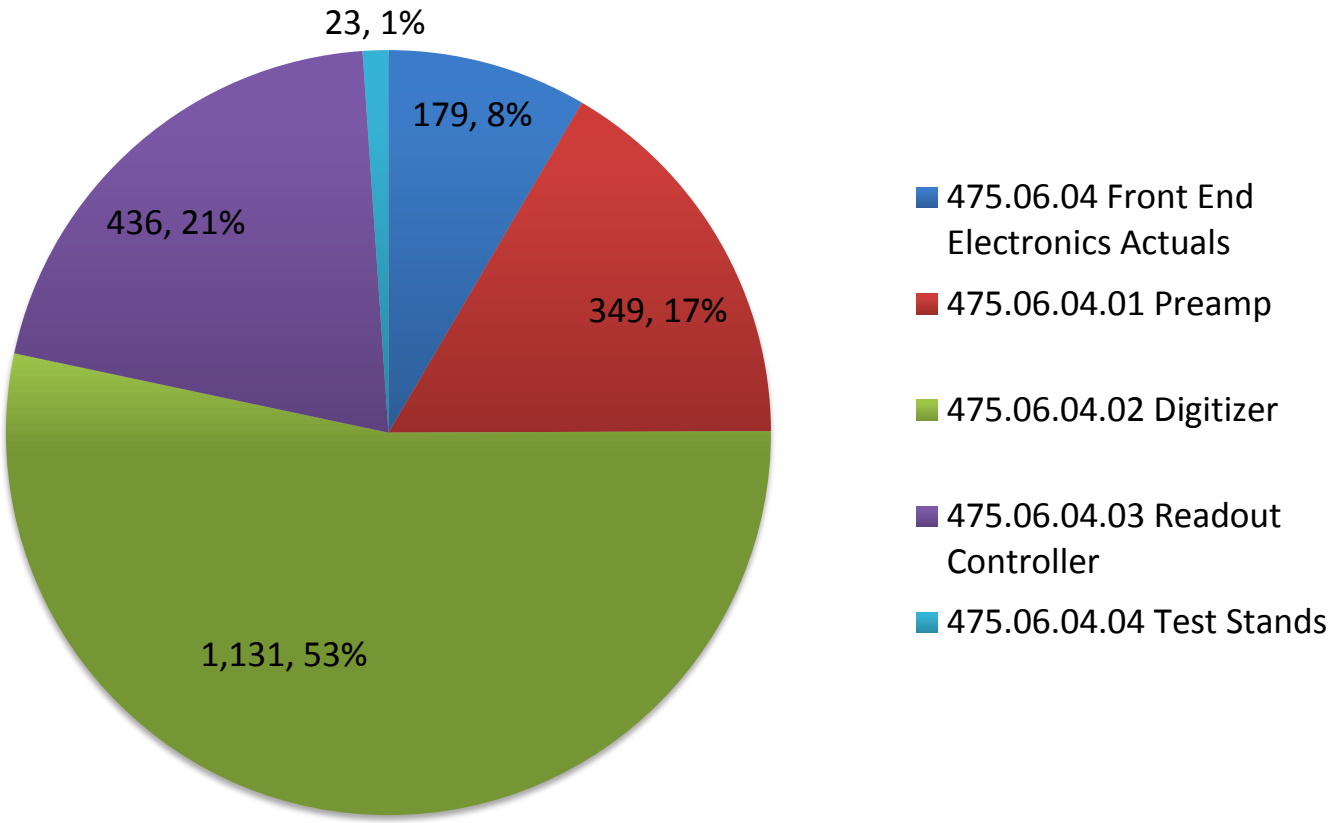


Infrastructure (Power distribution)

- Five low voltage levels needed (<5V)
- 48V power line from outside the cryostat
  - Allows for lower current (B field)
- DC-DC converters outside the stations step down to a suitable voltage
- Regulators inside the gas volume for actual distribution

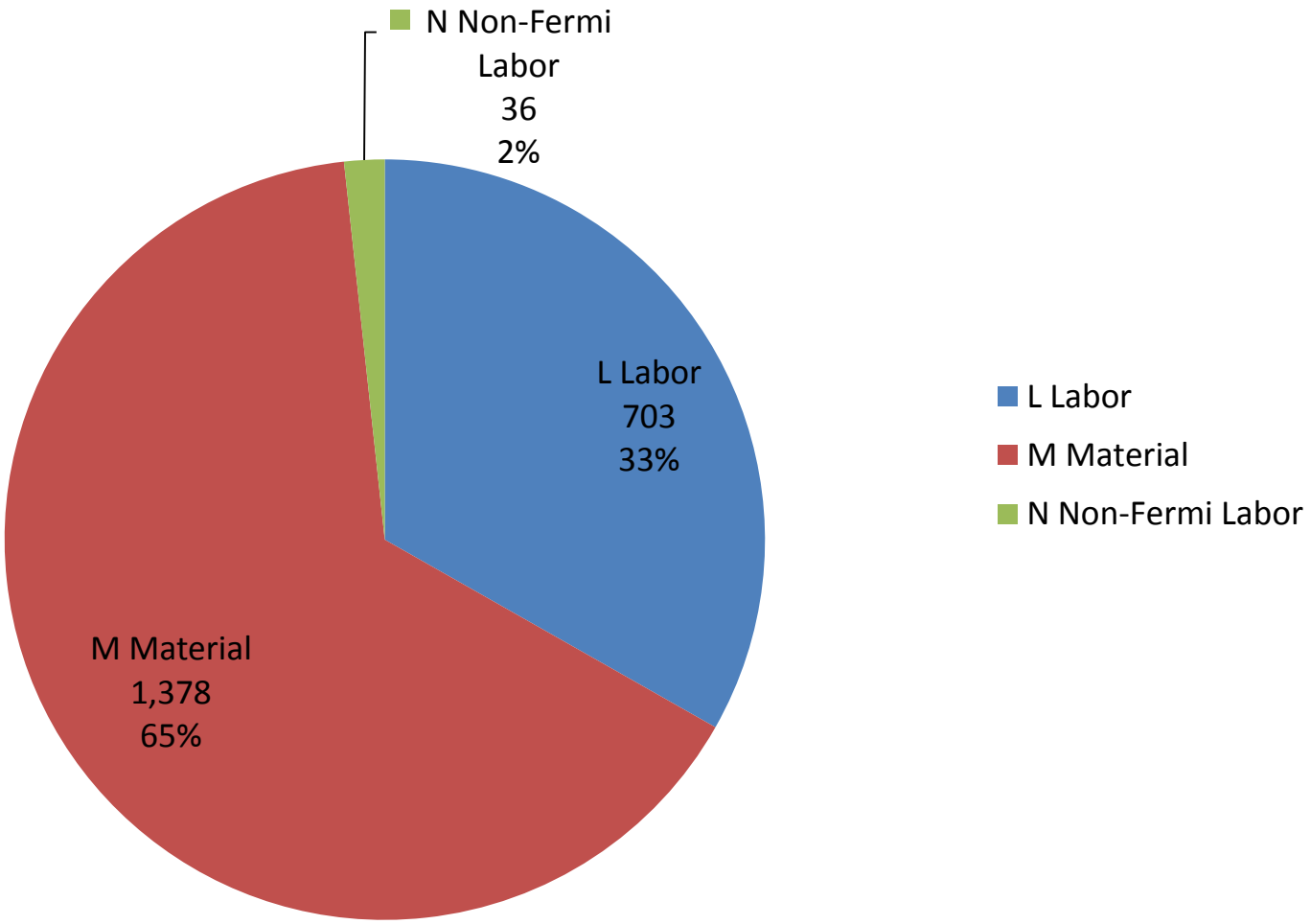
Cost Distribution by L4

Base Cost by L4 (AY $k)



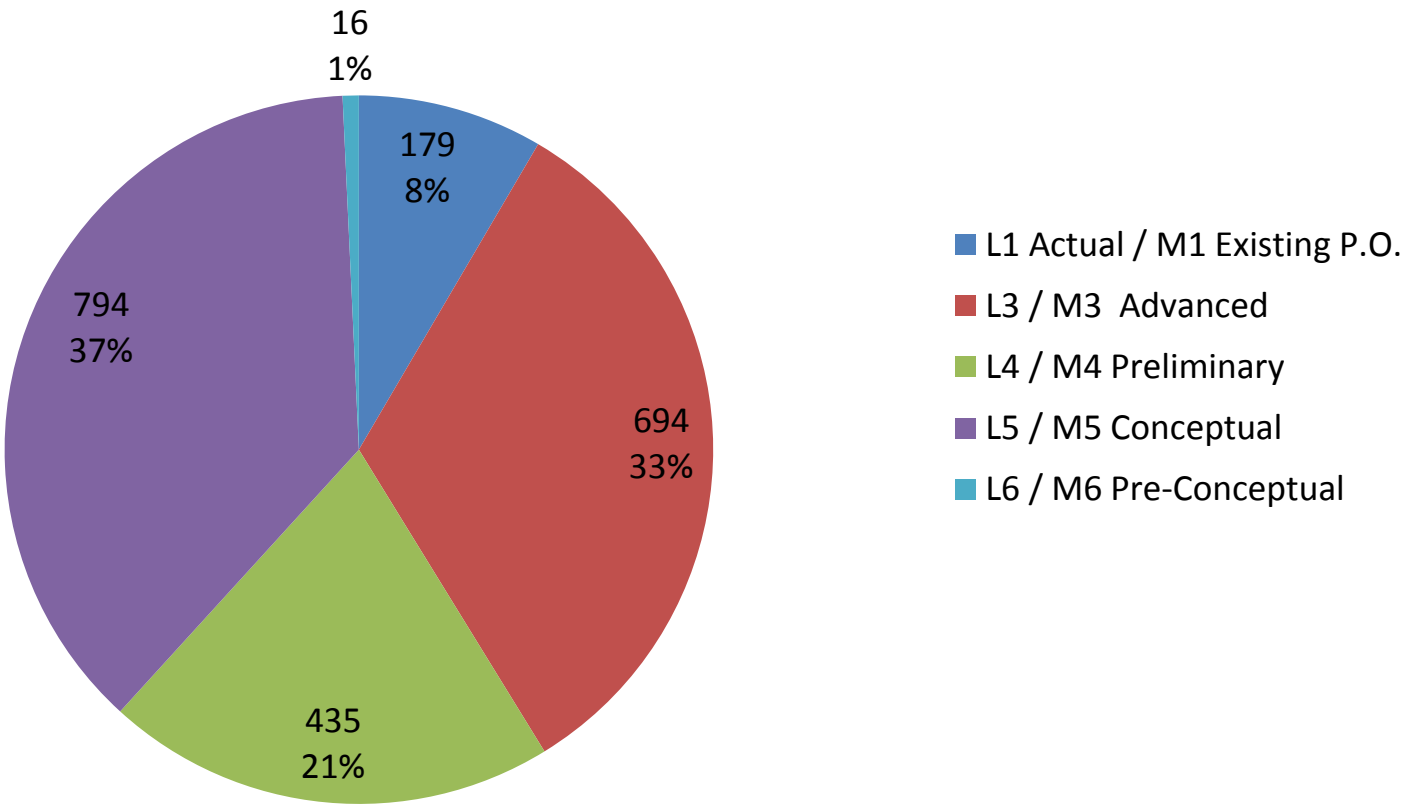
Cost Distribution by Resource Type

Base Cost (AY $k)

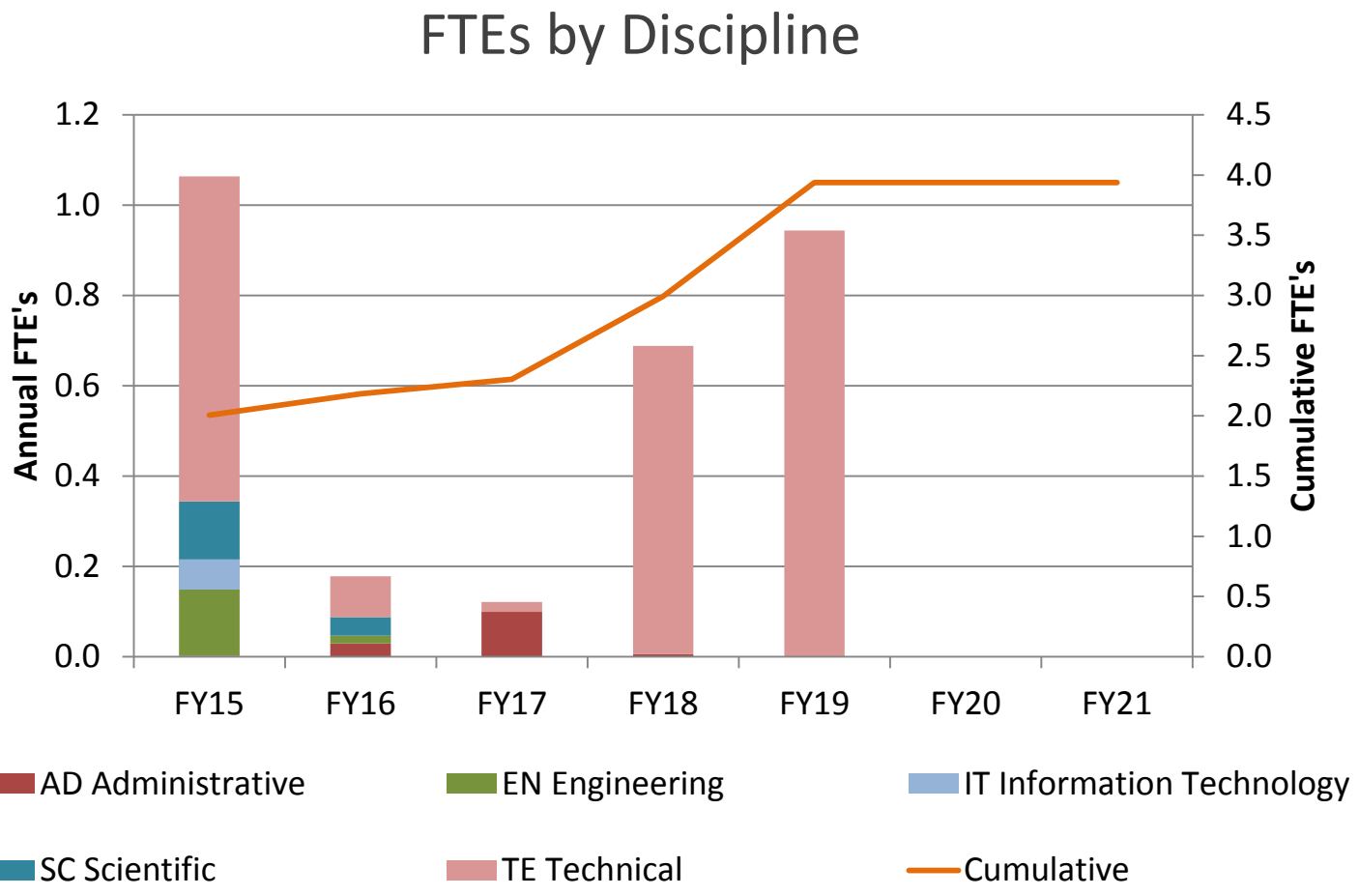


Quality of Estimate

Base Cost by Estimate Type (AY$k)



Labor Resources



Cost Table

Costs are fully burdened in AY $k

	Base Cost (AY k$)					
	M&S	Labor	Total	Estimate Uncertainty (on remaining costs)	% Contingency on ETC	Total Cost
475.06.04 Front End Electronics Actuals	42	137	179			179
475.06.04.01 Preamp	249	100	349	170	49%	519
475.06.04.02 Digitizer	772	358	1,131	287	25%	1,417
475.06.04.03 Readout Controller	346	90	436	173	40%	609
475.06.04.04 Test Stands	4	19	23	11	50%	34
Grand Total	1,414	703	2,118	641	33%	2,759

Summary

- Mu2e Tracker Front End electronics fulfills the requirements for the experiment
- Based on commercially (low cost) available components
- Flexible design
- Advanced prototyping stage on all fronts
- First integration stage using an 8-straw prototype chamber to be completed by the end of the summer