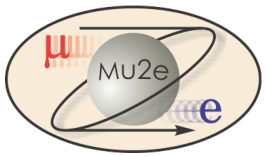
Fermilab

U.S. DEPARTMENT OF ENERGY Office of Science

Mu2e CD-2 Calorimeter 475.07.05 FEE and Digitizer



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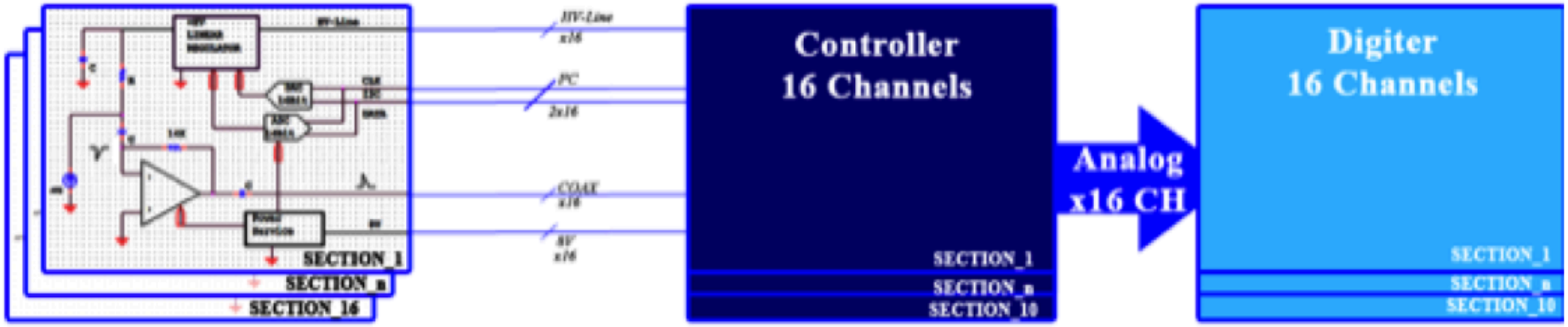
July 9, 2014

Design – Calorimeter FEE and Digitizer

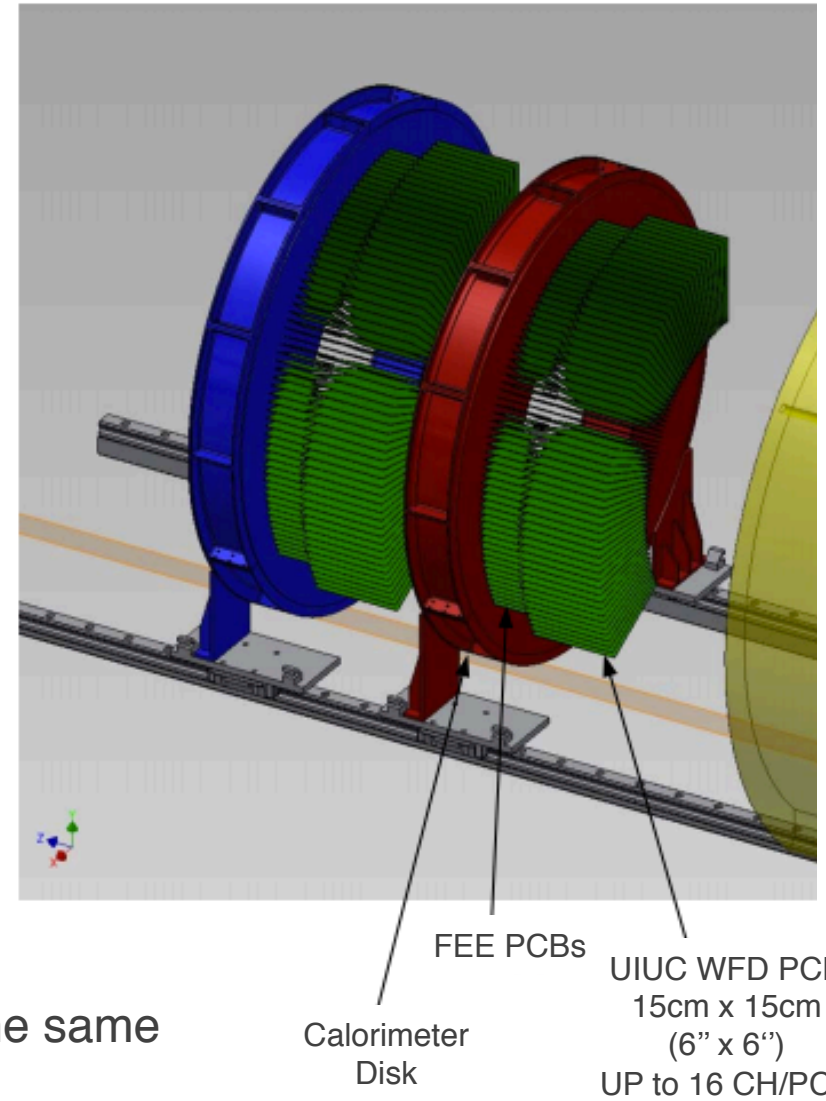
- Overall scheme for the calorimeter readout electronics: each disk (930 crystals per disk) is subdivided into 12 similar azimuthal sectors



  - Groups of 16 left (right) Amp-HV chips are controlled by a dedicated ARM controller that distributes the LV and the HV reference value, while setting and reading back the locally regulated voltage
  - Each sector is therefore controlled by 2 x 5 ARMs
  - Groups of 16 amplified signals are sent to a digitizer module where they are sampled and processed before being optically transferred to the DAQ system
  - 10 WFD digitizer boards go to a single crate

CALORIMETER DETECTOR CONCEPTUAL DESIGN

- There are therefore 12 crates per disk, hosting 10 sets of AMP-HV and WFD boards.
- The crates are placed in the outermost region of each disk.
- The crates are mounted on a pneumatic cartridge that allows them to be extended radially, thereby completely exposing the area behind the crystals when required.
- The crates are designed to provide heat dissipation for the APDs and electronics boards; they will have metal fingers in contact with a cooling pipe routed circularly below the bottom of the rack's connection mechanism to the disk.
- The cooling system will be connected to the same cooling circuit used by the tracking system



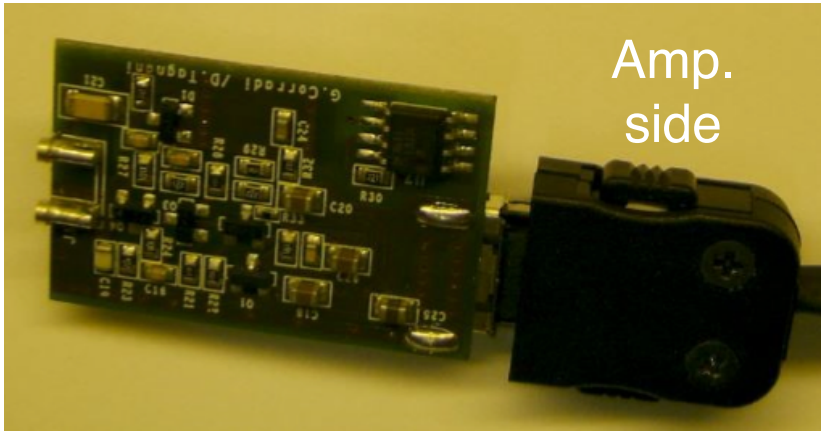
Requirements I – Calorimeter FEE

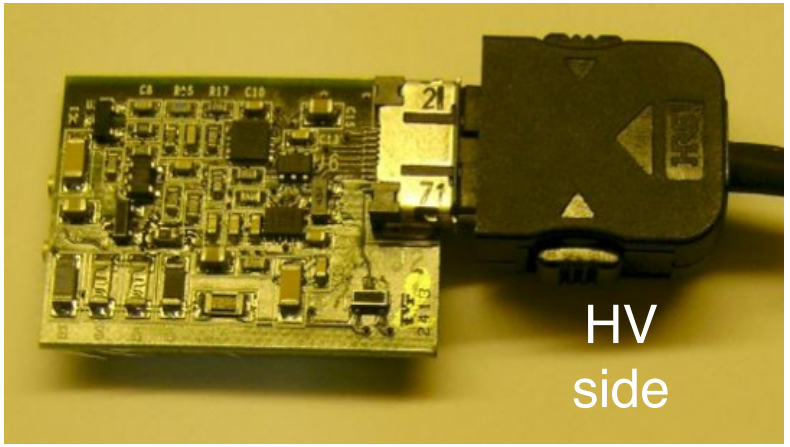
- Provide both the amplification stage and a local linear regulation for the photosensor bias voltage
  - High amplification with low noise
  - Fast signal rise and fall times for good time resolution and pileup rejection
  - Work in a rate environment of 200 kHz/channel
  - Have low power consumption
  - Provide an extremely precise voltage regulation with a long-term stability

Design – Calorimeter FEE

- The Amp-HV is a multi-layer double-sided discrete component board that carries out the two tasks of amplifying the signal and providing a locally regulated bias voltage, thus significantly reducing the noise loop-area.

- The two functions are independently done in a single layer of the chip, named the Amp and HV sides, respectively





Prototype characteristics – Calorimeter FEE

- The project and the development of the chip have been done at LNF by the SEA electronic department
- Characteristics of the Amp-HV chip:

Amp.

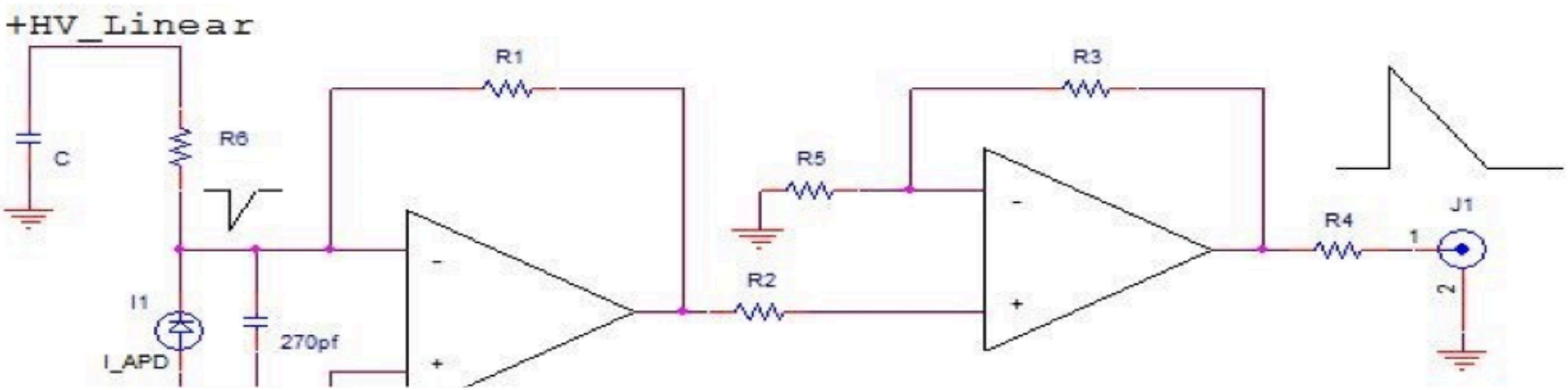
Dynamic		2.5V
Bandwidth		70Mhz
Rise time		6ns
Polarity		Reversed
Output impedance		50 Ω
Stability with source capacity	max	300pf
Coupling output end source		AC
Noise, with source capacity 1pf		1000 enc
Power dissipation		14mW
Power supply		6V
Input Protector over-Voltage		10mJ

HV

Adjustment range Vout	250V to 500V
Accuracy, reading and writing, Vout	16 bit
Current limiter can be adjusted	tpv. 300uA
Noise tot.	2mVpp
Long-term stability	100ppm
Settling Time	<500 us $\rho < 1$
Typical power dissipation	135mW
Double filter high Voltage, attenuation	56db

Amplification Layer – Calorimeter FEE

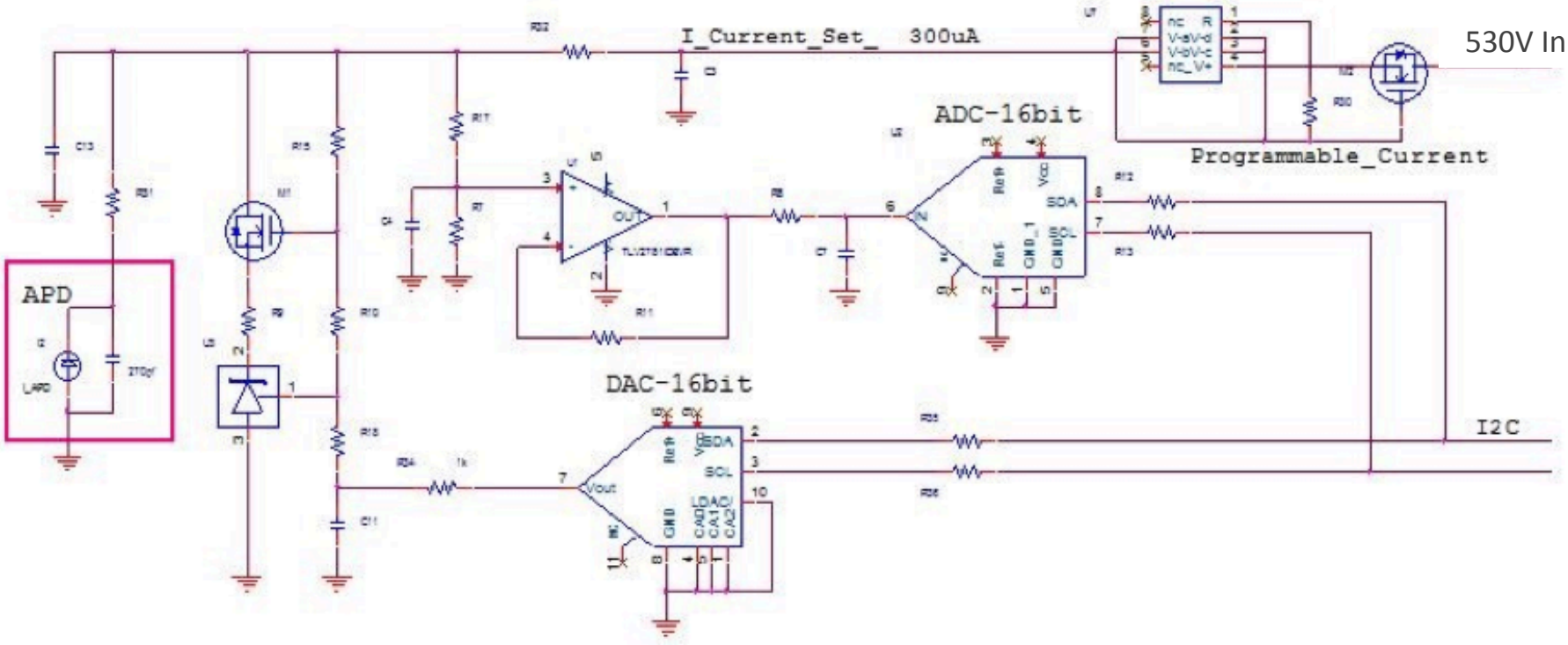
- The electronic scheme is that of a double stage trans-impedance preamplifier, with a final trans-impedance gain of 14kΩ
  (voltage equivalent, V_{out}/V_{in} of 300)



The equivalent noise charge (ENC) level is of about 1000 electrons, with no input capacitor source

Linear regulator layer – Calorimeter FEE

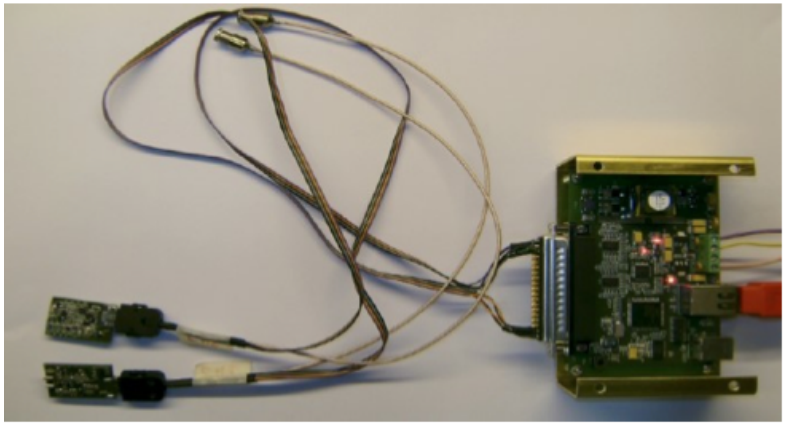
- The linear regulator are that it provide extremely precise 16-bit voltage regulation and long-term stability of better than 100 ppm

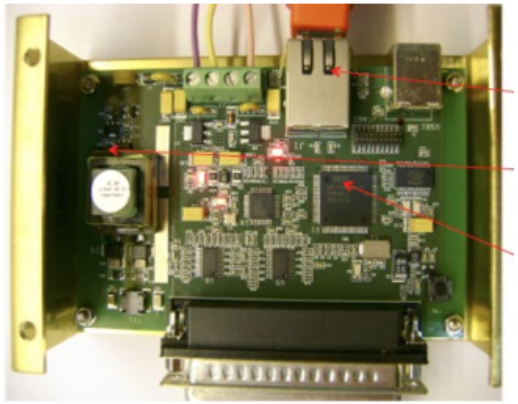


- The current limit of the APD is conservatively set to about 300 μA

ARM controller – Calorimeter FEE

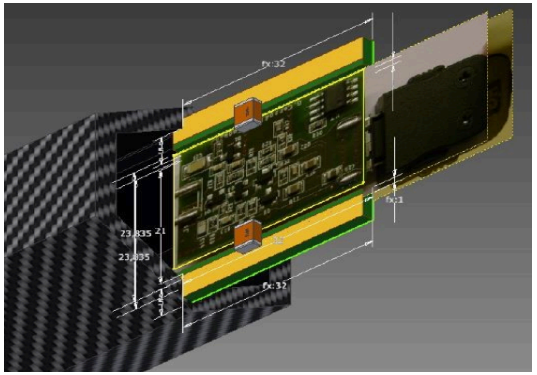
- The design of the CPU system architecture for the prototype, consisting of a series of Cortex M3-ARM processors
  - The high voltage required has been designed for the Hamamatsu APD and produced by a primary generator using switching technology, with very low noise, residing on the controller board. It generates a voltage of 530 V, and a current of 5.5 mA, sufficient to power 16 channels in parallel
  - The ON and OFF states of the channel are controlled by the ARM processor
  - The bias can be adjusted from 1600 to 1850 V, with a 16 bit regulation range. Similarly, the channel settings can be directly read out, using a 16-bit ADC.





Cooling – Calorimeter FEE

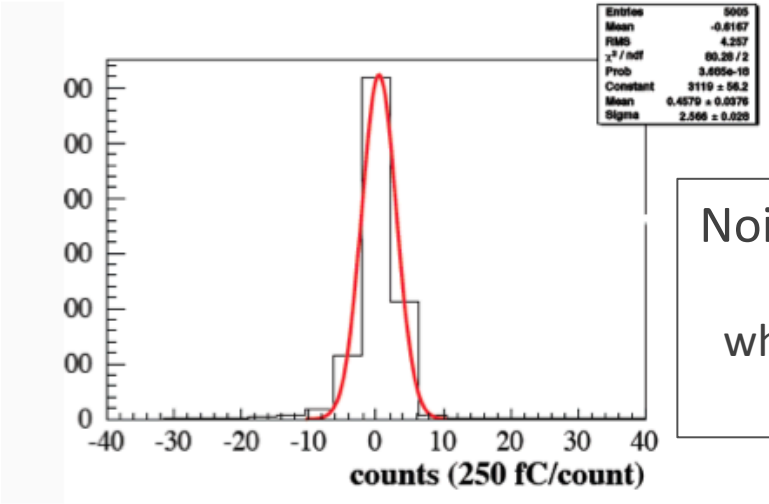
- The average power to be dissipated for the Amp/HV is ~150 mW per channel
  - The ground cannot be connected directly to the shielding surface
  - Therefore the use of a bulk bridge resistor, with a 1 pf capacitance, which is capable of transferring heat from the Amp-HV chip to the nearby mechanics, is foreseen



- The power dissipation of the controller board is about 5W, and requires two voltages: +8V/100 mA to power the Amp-HV cards and 12V/300 mA for the high-voltage primary generator.

Summary I – Calorimeter FEE

- ✓ 40 prototypes have been built during 2013 and have been used for the test of the LYSO matrix prototype.
- ✓ The requirements are successfully satisfied.
  - We have extracted the ENE from the noise term found using a ^{22}Na source with a LYSO crystal read out by an S8664-1010 APD, followed by the Amp-HV chip. The APD gain was set to 150 and a light yield of 2400 pe/MeV has been measured.



Noise distribution in counts:
the *rms* is 2.6 counts,
which corresponds to 36 keV
related to the ^{22}Na peak

Summary II – Calorimeter FEE

- ✓ For the BaF_2 calorimeter, the photosensor will be the 9x9mm RMD/JPL device that has two improved characteristics with respect to the Hamamatsu S8664:

  (i) a capacitance of ~ 60 pF, and

  (ii) an operational gain of 500.

- ❑ The electronic will be matched to the RMD/JPL device.
- ❑ In the final design the HV generator will be moved outside the DS and the HV signal will be brought on cables through the end-plate feedthroughs. In the latter case, each HV cable would serve 4 boards, i.e., 64 channels.

- ❑ The final design is being integrated with the digitizer one

Requirements II – Calorimeter Digitizer

- The exact shape of the signal is a function of the crystal material, the APD employed and the FEE parameters. We expect pulses of 50 ns width and maximum pulse height of 200 mV.
  - This requires very fast digitization and good resolution
  - The boards will be operated in vacuum, 10^{-4} Torr and access will be difficult
  - The expected radiation dose will be of the order of <12 krad/year and $\sim 10^{9}$ $n_{1MeVeq/year}$

Design – Calorimeter Digitizer

- The calorimeter is composed of 1860 crystals, each equipped with 2 APD photosensors, so in total 3720 fast analog signals will be digitized after being amplified and shaped by the FEE.
- We find that 200 Msps and 11 bits of resolution are a good compromise with power dissipation and cost
  - The Mu2e Calorimeter Waveform Digitizer subsystem (Cal_WFD) is an electronic printed circuit board that digitizes analog data, serializes and sends it upstream to the DAQ via a fiber optic transceiver
  - The Cal_WFD must also perform some minimum digital signal processing (DSP), removing data below threshold as well as providing mean charge and time for each channel by means of running averages

Modules – Calorimeter Digitizer

- The FPGA will be the core component of the WD board. It will have several functions:
  - Drive the ADCs control signals to synchronously get all the samples
  - Write the data to a DDR memory (a DDR hard controller is thus a requirement in the FPGA choice). Data will be sent to the DAQ in the inter-spill period
  - Read data from the DDR and serialize them (so fast internal serializers are another fundamental requirement for the FPGA)
  - To limit the number of fibers reaching the DAQ, the WD will be daisy-chained in rings. Each FPGA will thus receive data from the previous WD, add its own data and send them again to the next board
  - Slow control commands will be received and served by the FPGA through the same fibers used for data

Prototype – Calorimeter Digitizer

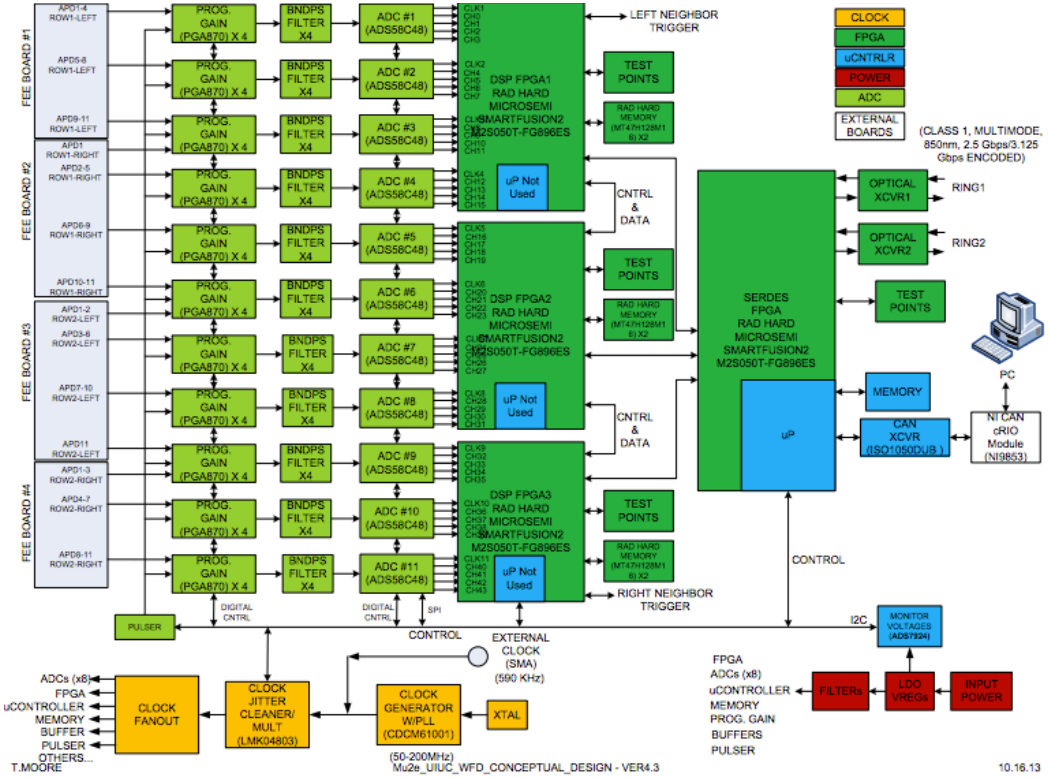
- A prototype board has been designed and is currently being tested. The experience gained with the prototype will be the base for the final Cal_WFD design. The requirements described are applied both to the prototype and the final board design.

- Block diagram digitizer board with SMARTFUSION FPGAs

Each 16 Channel,
WFD Board needs 23W

900 mW/ADC x 4 ADCs = 3.6W
680 mW/AMP x 16 AMPs = 10.9W
2.3W/FPGA x 3 FPGAs = 6.9W

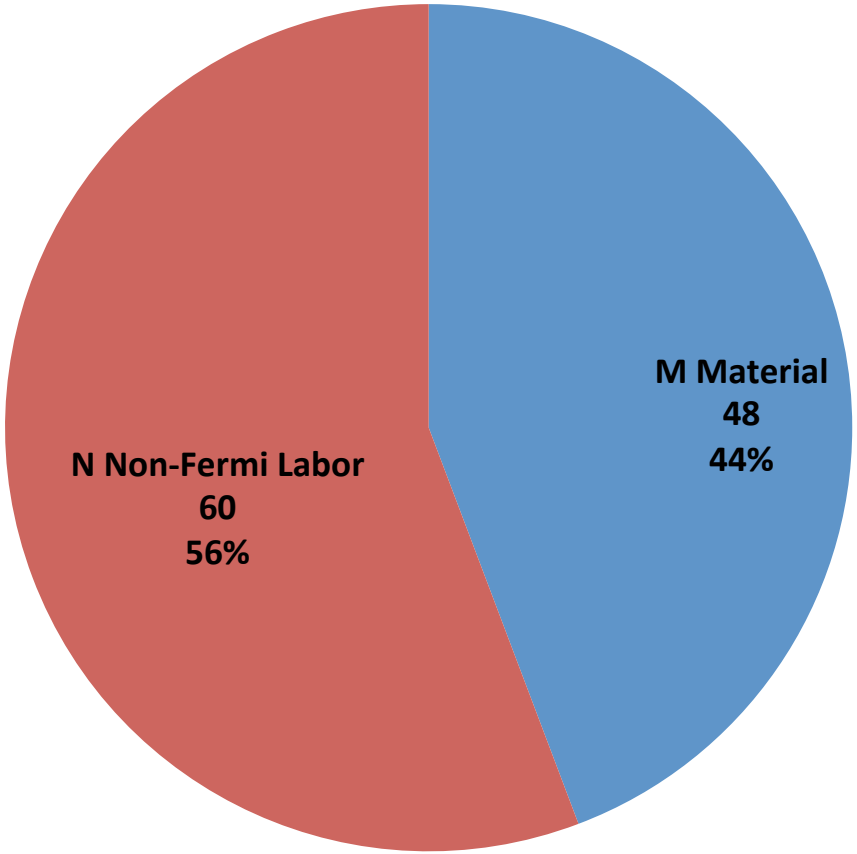
1.5W, Controls & Fiber Optics



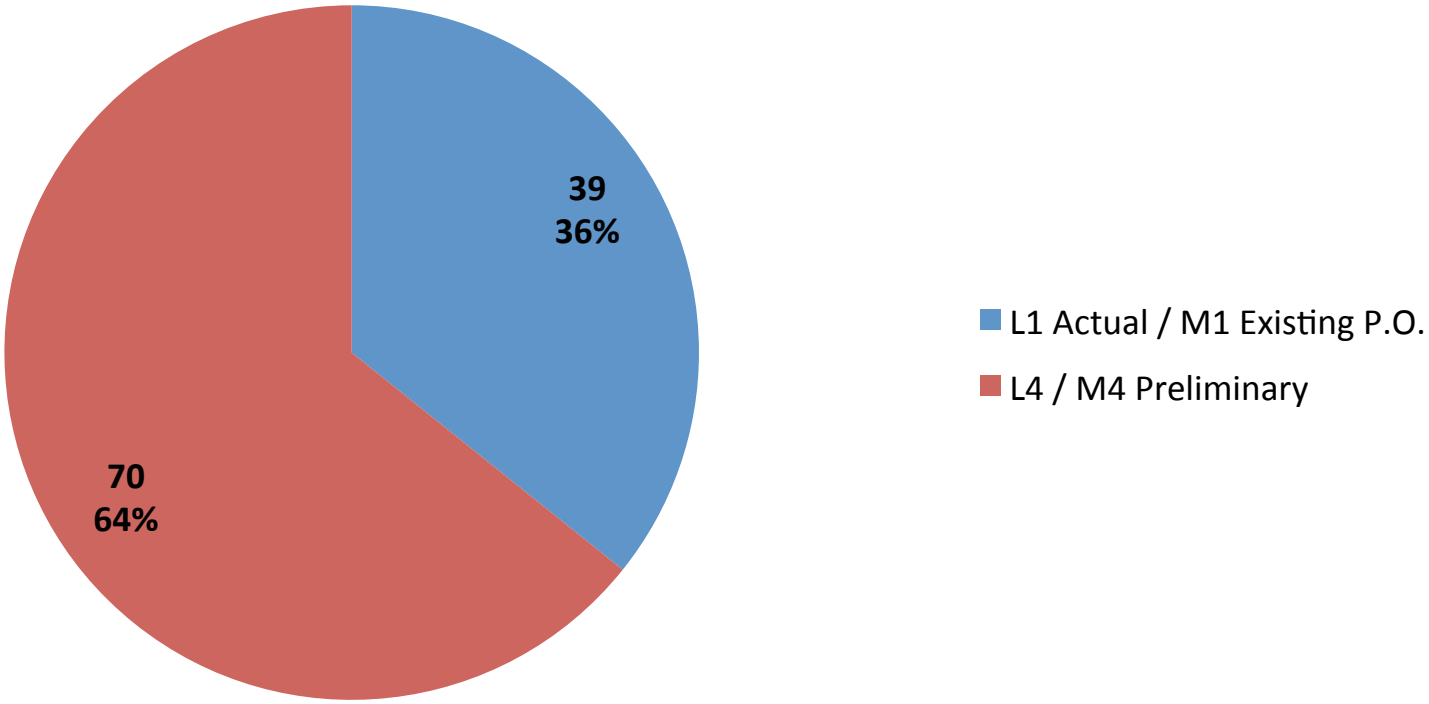
Technical design – Calorimeter Digitizer

- The WD follows the same block diagram of the prototype, but the boards will be operated in vacuum (10^{-4} Torr) and access will be difficult. This implies design rules quite similar to those used for space flight:
  - Highly reliable design (high MTBF). Some components will be of military grade
  - The thermal dissipation will be mainly removed by conduction, so the board mechanics (and of the supporting brackets or crates) and the PCB will have to be designed to take this into account
- Special care is needed for digital components and, in particular, the FPGA. Radiation-hard components, which are notoriously quite expensive, will be avoided, but at least for the FPGA a radiation tolerant device is selected:
  - It will be necessary to perform one or more irradiation tests before finalizing the design

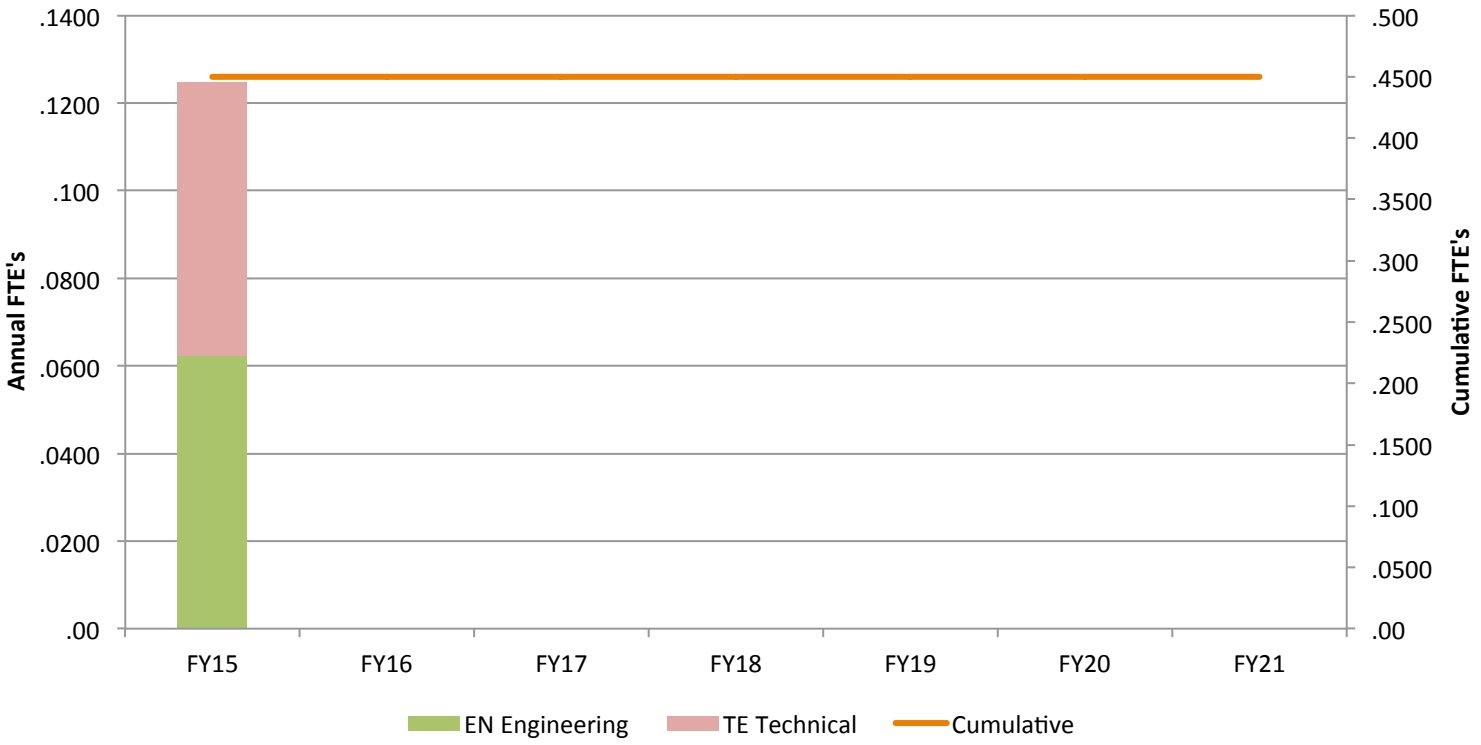
Digitizer: resource type



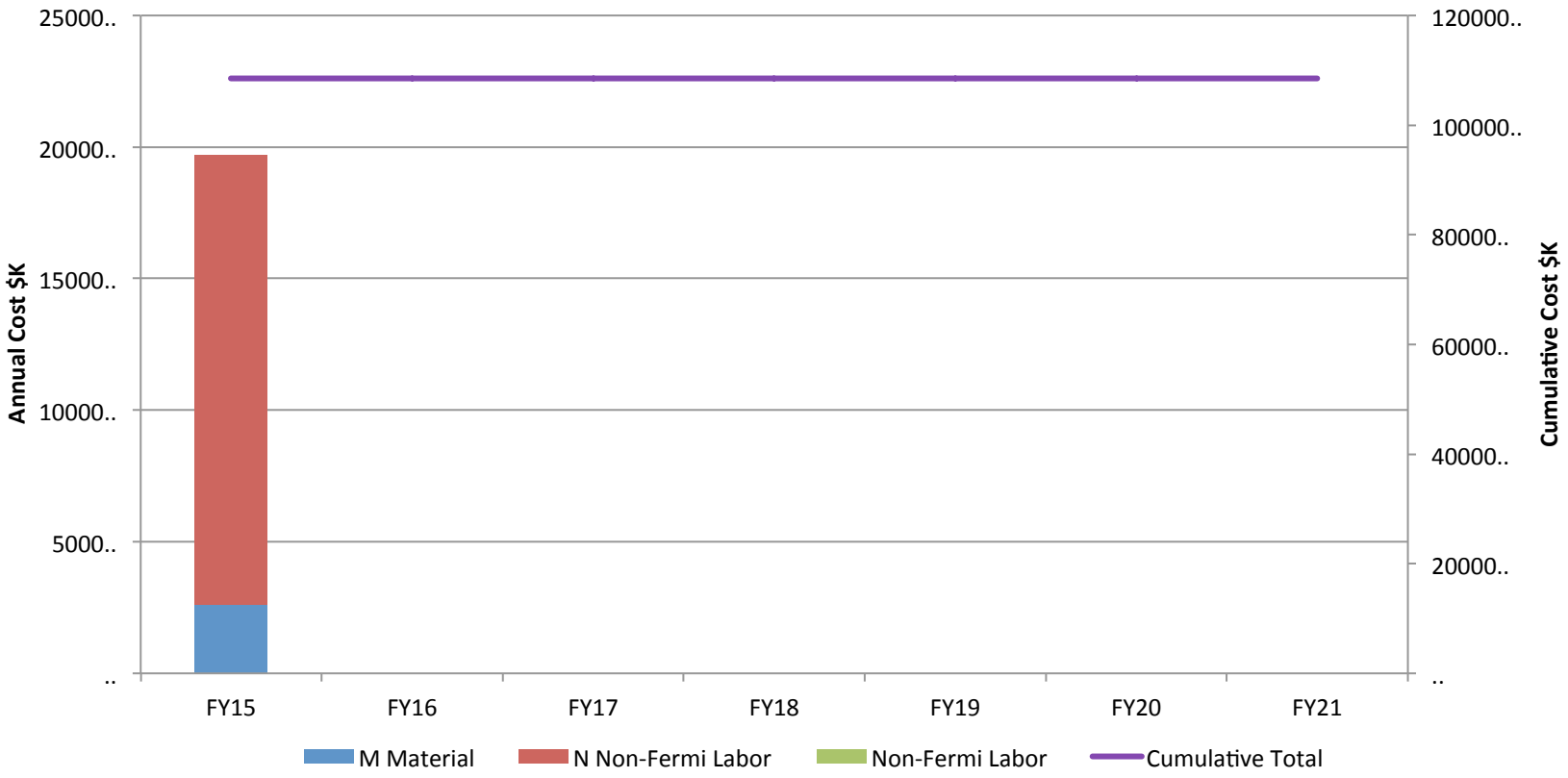
Digitizer: Quality of estimate



Digitizer: labor resources



Digitizer: labor/material profile



Summary – Calorimeter Digitizer

- ✓ ADC: the model used in the prototype appears to be adequate for the production board, both in terms of dynamics, sample rate and low power requirements. The cost is around $100 in quantity and supports 4 channels, bringing the cost to a reasonable $25 per channel.

- ❑ FPGA: we need a high speed FPGA, with an internal serializer and a DDR controller, low power and which is radiation resistant. Currently, the best choice seems to be the Microsemi SmartFusion2 M2S150T-1, which is SEU free, flash-based, and includes some mechanism for SRAM protection.

SPARES

Spare I

- The pre-amplifier has a bandwidth of 70 MHz, corresponding to a signal rise time of 14 ns:

  → To check this with the complete electronic chain, the photo-sensitive APD area was illuminated with a green laser having a narrow pulse of 2 ns width

- We determined the ENC to be ~1000 e^- with negligible input capacitance, growing nearly linearly up to 270 pF.

The measurement related to the amplifier itself has LV on and HV off, which corresponds to ~11500 e^- for a 500 ns integration window. To confirm this measurement, we have extracted the ENE from the noise term found using a ^{22}Na source with a LYSO crystal read out by an S8664-1010 APD, followed by the Amp-HV board. The APD gain was set to 150 and a light yield of 2400 photoelectrons/MeV has been measured. The *rms* is 2.6 counts, which corresponds to 36 keV after correcting for the ^{22}Na energy peaks. To extract the ENC(e-), the ENE(MeV) has to be multiplied for the light yield and APD gain, and an ENC of 13.000 e^- has been obtained.

Spare II

- For the BaF2 calorimeter, the photosensor will be the 9x9mm RMD/JPL device that has two improved characteristics with respect to the S8664:

(i) a capacitance of ~60 pF

(ii) an operational gain of 500.

The ENC(e^-) will be ~5000 e^-. Assuming a light yield of 30 pe/MeV, the expected noise level is ENE=ENC(e^-)/(G*LY) =5000/(30x500) = 0.33 MeV.

After receiving a dose of >10 krad, the LY will be reduced by 30-40%, so that the noise will increase to 0.55 MeV.

The signal peak in mV will be equivalent to 1/9 of that of LYSO, corresponding to a voltage output of 4 mV/MeV.

Spares III

- From beam flash simulation, we derive the expected data throughput when zero- uppressing the data below the 1 MeV threshold that corresponds to ~20 % channel occupancy, *i.e.*, an average of 40 kHz/ channel of random hits.

- A 50 ns signal width provides 10 samples after zero-suppression. In our estimate, we add a factor of two sample safety margin for the determination and monitoring of the signal baseline. In this case, the data throughput is 3720 (chan.) x 11 (bits) x 20 (samples) x 40.000 (hits/s), corresponding to 32.2 Gbits/sec (4 GBytes/sec), which matches the DAQ requirements. For a total number of 120 WFD boards reading out the full calorimeter, we expect 260 Mbits/sec (32 MBytes/sec) per board. Since the rings are limited by a 2.5 Gb/sec throughput, we organize the calorimeter into twelve sectors with 5 boards/ring per sector. A total of 24 rings are needed for the whole calorimeter.