Development of Application Specific Integrated Circuits at Fermilab

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Fermilab
DOE Detector R&D review
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Outline

- Introduction:
  - Mission and people
  - Recent major activities
  - Roadmap of technology processes in use
- R&D axes based on ASIC technology
  - 3D-IC
  - Intelligent pixels
  - SOI
- Resources
  - EDA/CAD tools
  - Instruments and tests
- Conclusion

Mission and Process

- Provide integrated circuits for detectors to build experiments
- Perform critical R&D on detectors for future energy and intensity frontiers experiments
- Activities:
  - Primarily: advanced instrumentation for HEP;
  - Secondarily: where synergies and where appropriate - leverage technologies for other fields and work through collaborations
- Projects usually brought from the community and the laboratory
- Initiation phases usually funded by KA15 – demonstration followed by support from projects

People

- ASIC Group part of PPD/EED
- 6 ASIC designers (3 PhDs)
  - 2 senior – project leader level
  - 1 pursuing PhD
  - 1 providing maintenance
    of tools, licenses, scripts, etc. *(essential!!!)*
- 1 engineering physicist (PhD)
- 1 test engineer *(need more)*
- 2 technicians

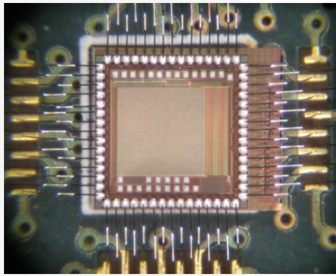
\+ depending on needs 1 PCB drafter

\+ occasional support from other resources within PPD/EED, CD and other departments at Fermilab

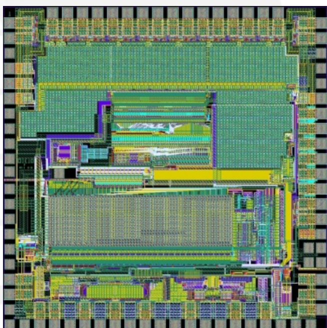
group depleted by 1 person (retirement) in 2011

Recent major activities

- Electronics and sensor technology is central to Particle Physics research – spinoffs in domains based on similar detection technique (ex. nuclear medicine),
- Microelectronics technology progression is rapid – science is a not a driver – leverage of emerging technologies for advancing instruments for HEP,
- Experiments need sensor arrays or grids of unheard-of sizes and in-situ processing and low mass


VIP2a 3D-IC

VIPIC1 3D-IC

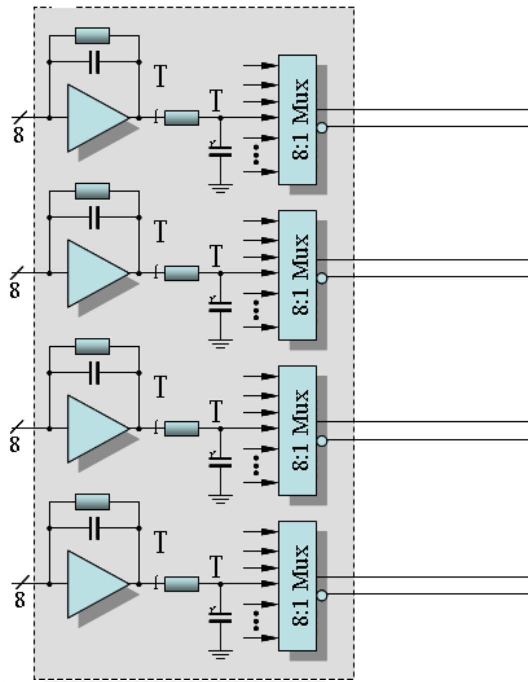

QIE10
tape out fall 2012

-- Complete list of projects --

- H-CAL ATLAS (ANL) and CMS (FNAL) QIE10 (2D)
- CMS p_T tracker-trigger VICTR (3D-IC)
- CMS phase 2 pixels upgrade CMSPIXELS (2D)
- HL-LHC hardware tracker VIPRAM (2D/3D-IC) → (content addressable / associative memories)
- photon science instrumentation VIPIC (3D-IC) → (X-ray Photon Correlation Spectroscopy – with BNL)
- monolithic pixel detectors in SOI process MAMBO (2D-SOI)
- highly granular pixels for lepton collider VIP (3D-IC)
- cold electronics: lAr TPC for LBNE (showed lifetime of transistors in .1μm scale adequate for integrated electronics for operation in Cryogenic)
- solid state PM *G-APD, SiPM* (implementation in 3D-IC)
- others, like: design of sensors, qualification of systems

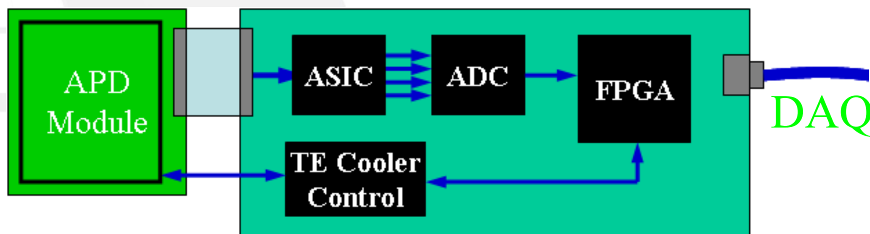
Projects transitioning from KA15

Front End Electronics for the NOvA Neutrino Detector *(completed 2010)*



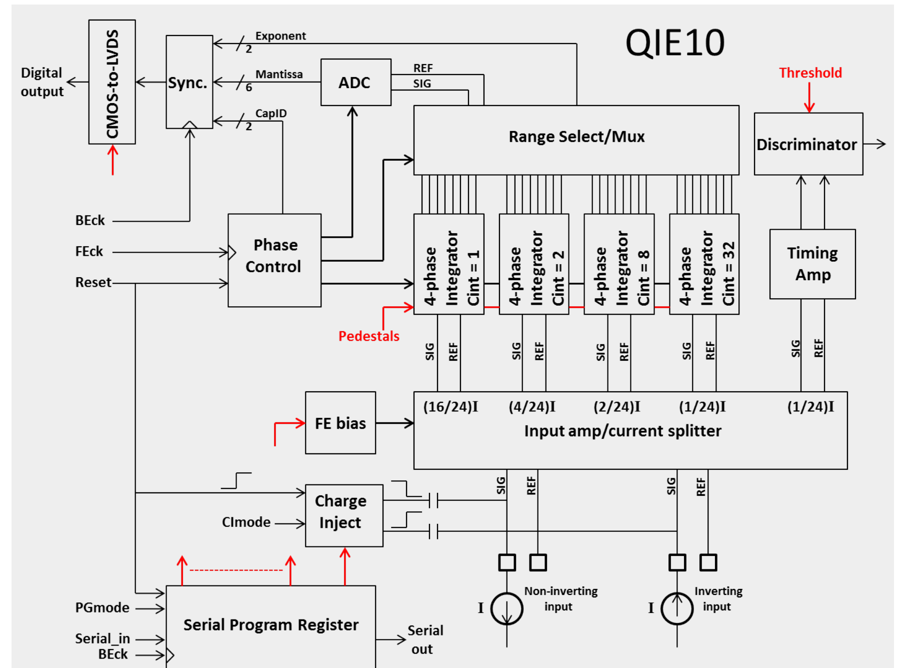
- 8:1 multiplexers run @ 16 MHz to sample each channel at 500ns
- 2 Msps per channel
- Adjustable rise-time & fall-time

completed



Charge (Q) Integrator and Encoder QIE10 *(transitioning KA15 ➔ project funds in 2012)*

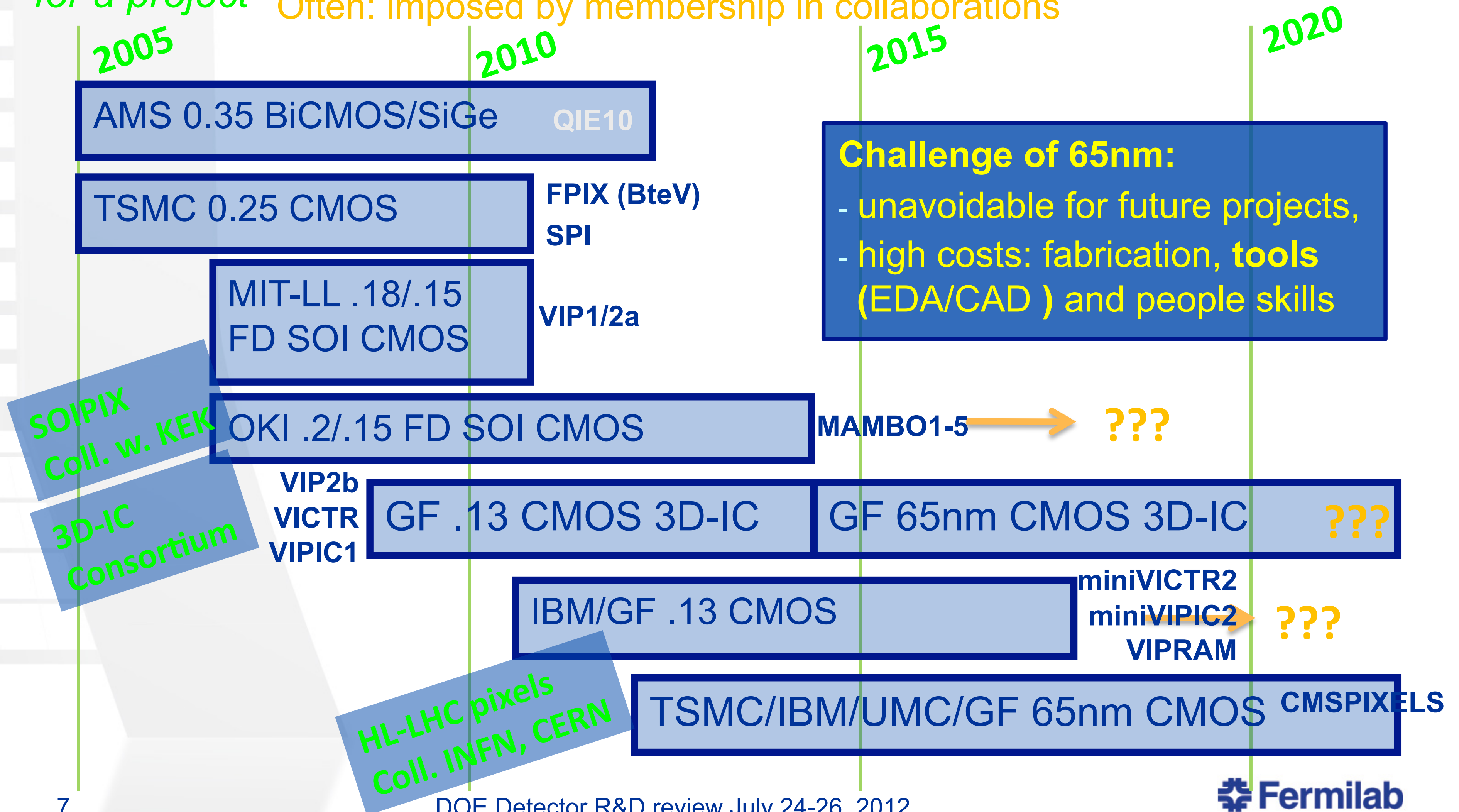
- QIE10: 0 – 330 pC range (10×higher wrt QIE8),
- 3 fC/LSB at the low end (nearly 17-bit DR),
- Resolution = 1.4%,
- 16 bits out every 25ns (6b-2b-2b-6b mantissa, exponent, CapID, timing discriminator ADC)
- Timing discriminator σ_t=~500ps



Fermilab

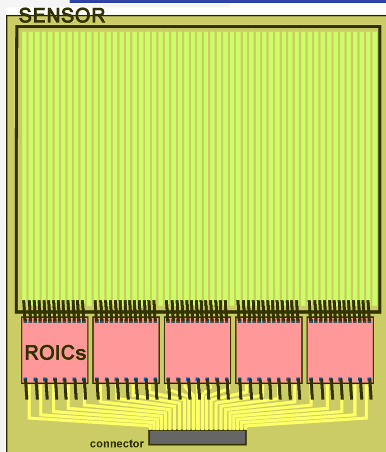
Roadmap of technology processes

Ideally: by understanding of needs of various projects, analysis of market and seek for best compromise: performance-cost-experience;
Often: imposed by membership in collaborations

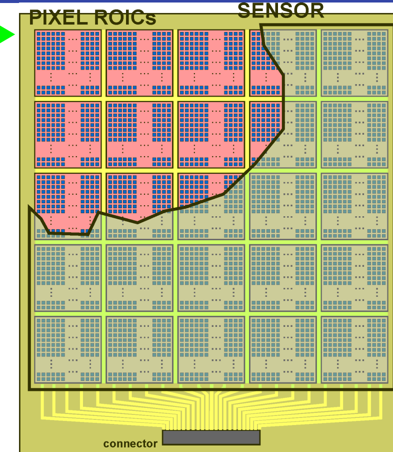


R&D towards integrated pixel systems

Trend observed is the migration of most systems, even those that until recently were offering only one dimensional information e.g. strip detectors (where a sensor is not covered by electronics) towards generalized pixels



real pixels of small both geometrical dimensions and quasi-pixels where one dimension maybe 10×larger than other



R&D in solid-state pixel detectors
(from tracking to calorimetry)

Hybrid:

2D + bump bonding
CMSPIXELS

3D-IC + fusion bonding / HDI
VIP, VICTR, VIPIC

High risk = High reward

Monolithic:

Quadruple well MAPS processes
Fermilab is not involved ex.LePix CERN

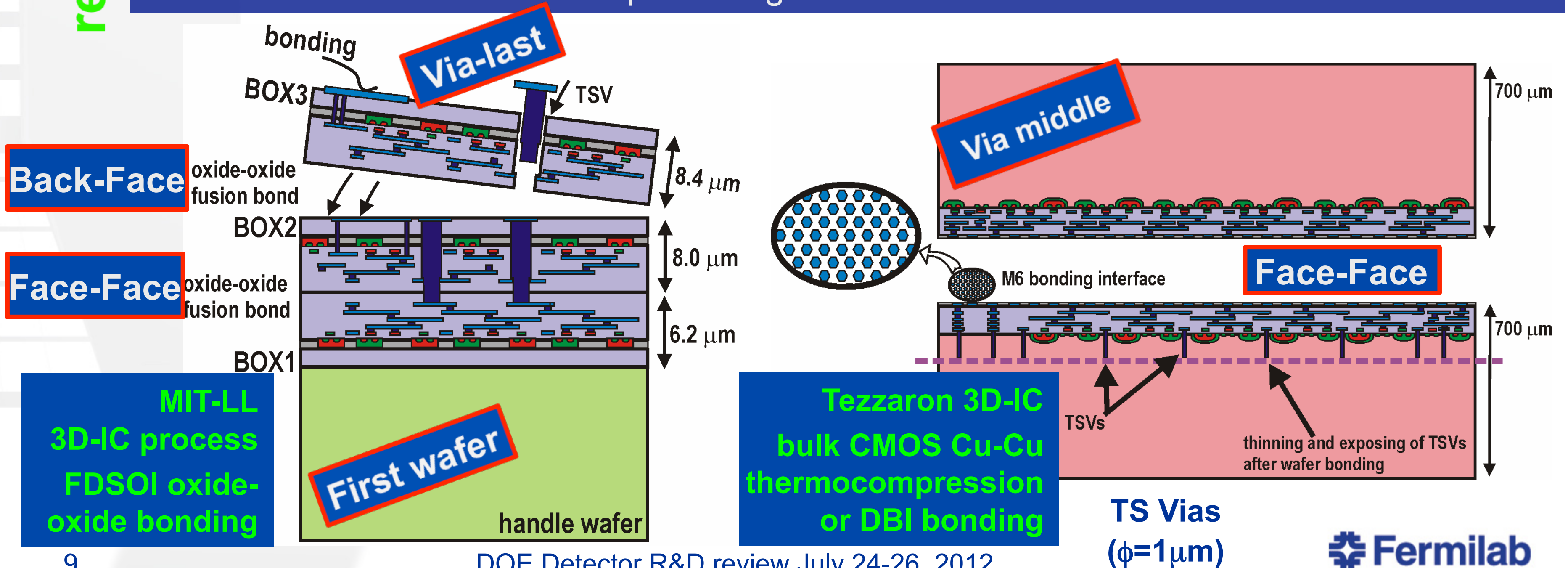
SOI processes
MAMBO with KEK and ASI

3D-IC revolution definition

3D-IC: definition

A chip in three-dimensional integrated circuit (3D-IC) technology is composed of two or more layers of active electronic components, integrated both vertically and horizontally

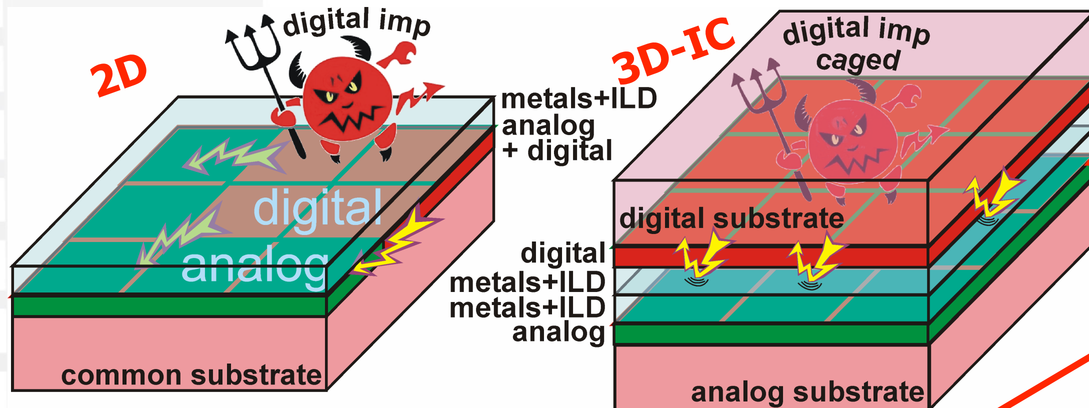
- Through Silicon Vias (TSV) for vertical wafer/chip connectivity not only electronic chips but also for attaching detectors to readouts
- Bonding: Oxide, polymer, metal, or adhesive strengthened (W-W, C-W, C-C)
- Wafer thinning: aggressive and precise
- Back-side metallization and patterning



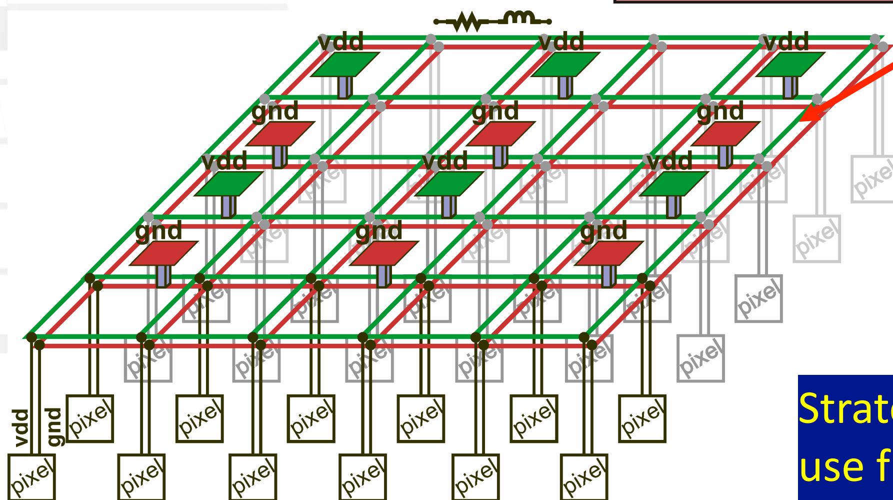
3D-IC: benefits

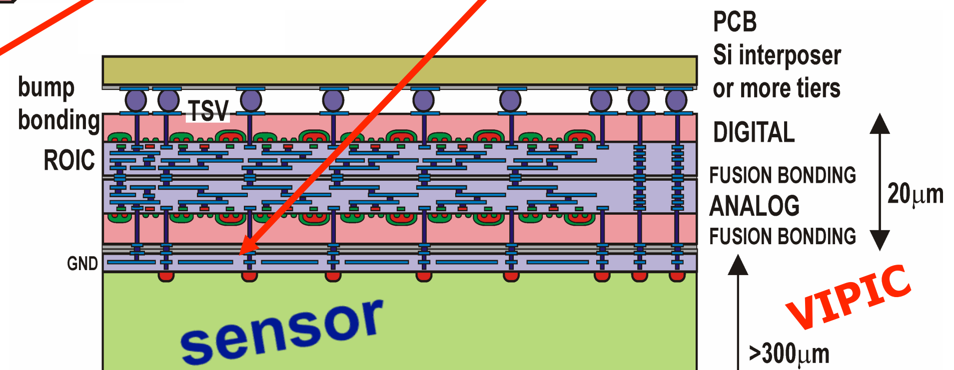
Why?

- Current fine-grained detector technologies face serious limitations; incremental improvements have proved inadequate
- 3D integration offers a transformational change to address current roadblocks to advance detectors in these areas



- 3D ROICs - complete separation of digital activity from low-noise analog parts
- 3D ROICs - uniform distribution of power supply and I/O pads on the back side
- ROICs can be integrated with sensors without bump-bonds

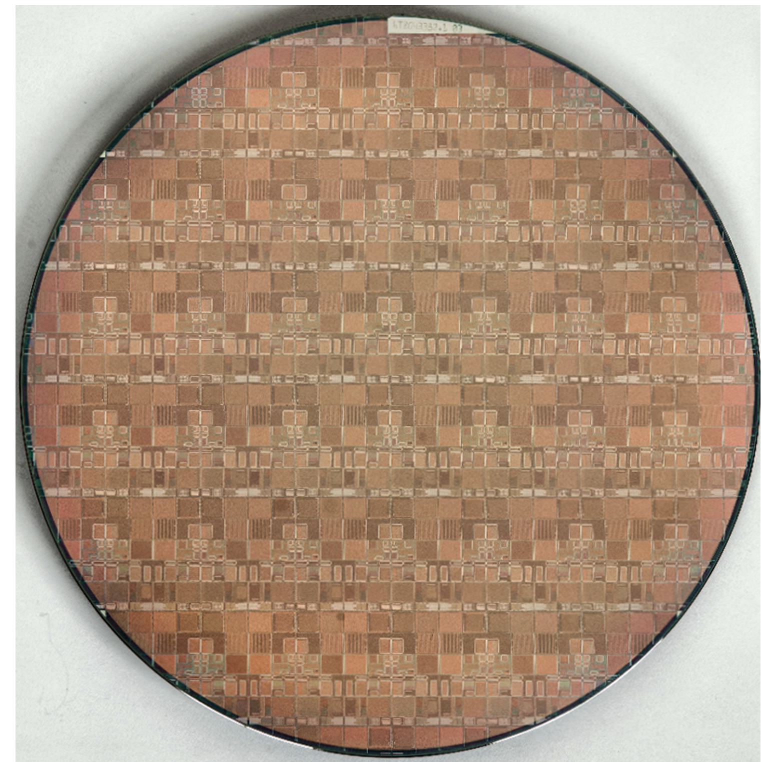




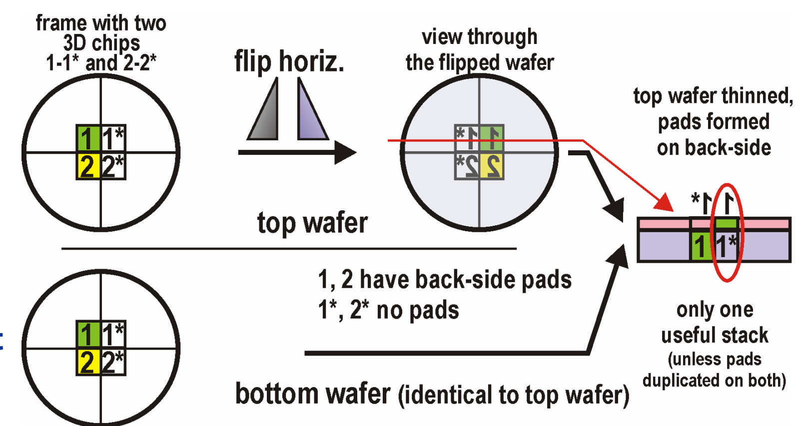
Strategic : 4 side buttable, dead-area-free detectors for use from X-ray, visible, IR imaging to classical tracking

3D-IC: realization

- **Initially small efforts started at Fermilab:**
  - **brought an expert and internationally regarded position to Fermilab in 3D-IC (leadership role within an international HEP community)**
  - **stimulated great interest among the detector community worldwide and eventually materialized in the 3D-IC consortium formed and led by Fermilab**
- **3D-IC Consortium established in late 2008, now 17 members; 6 countries: USA, Italy, France, Germany, Poland, Canada) + Tezzaron** ***– activity needs to be revitalized***
- **Fermilab organized first 3D-IC MPW run for HEP**
- **Designs in: 05/2009; Chartered (GF) 130nm**
  - **Many challenges in working with cutting edge technology; like: design mistakes, incompatibility of software tools at Tezzaron (not Cadence), handling of gigantic (>10GB) databases, shifting Chartered (GF) requirement, etc.**
- **MPW frame accepted by Chartered in 03/2010**
- **3D bonding did not yield for initial lot of wafer, until June 2012 when successful chips were obtained from 2 bonded pairs of wafers**
  - **Some combination of bad luck and human carelessness: initial lot fabricated with reticle shift to optimize yield of full reticles but inhibiting 3D bonding (whole lot refabricated = 1st lot),**
  - **3D bonding not successful on almost all wafer pairs from 1st lot**
- **Fermilab run in fab in parallel with 2 other runs**
  - **(DARPA and SNL) – they were successful**



GF/Tezzaron wafer for 3D chips from Fermilab MPW run



3D-IC: impact

- MOSIS/CMP/CMC assumed taking over responsibility for future submissions
- Fermilab has helped in the process of opening access to 3D-IC services by MOSIS
- Fermilab developed various ingredients:
  - Wafer-to-wafer bonding interface template
  - Reticle division template
  - Library of minimum set of standard digital cells
  - Library of 3D pads
  - Some 3D oriented design verification
- Fermilab put a 2x6mm^2 test chip on the MOSIS 3D MPW run free of charge. It contains blocks of NMOS devices with layouts for characterization of HCE degradation (lAr TPC @ LBNE)

-- transfer --

ANNOUNCEMENT

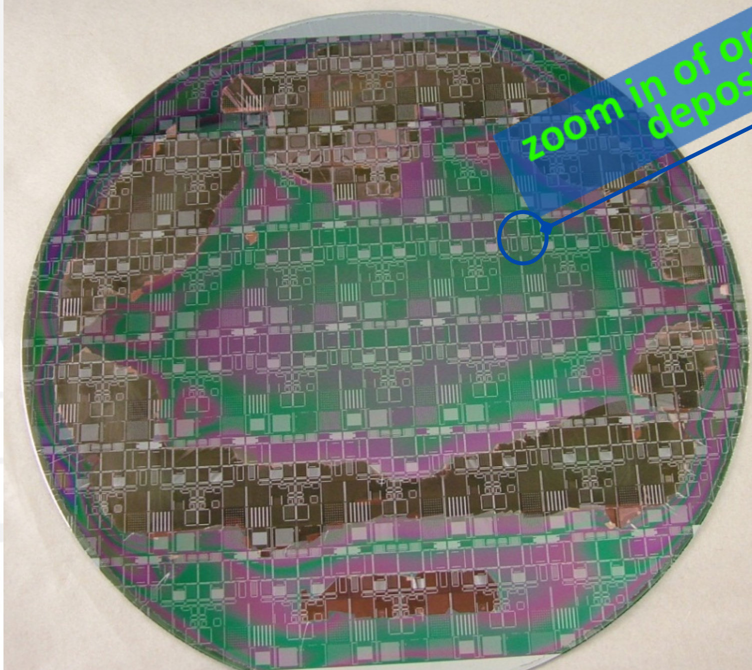
CMP/CMC/MOSIS partner to introduce a 3D-IC process

Grenoble, France, 22 June 2010, CMP/CMC/MOSIS are partnering to offer a 3D-IC MPW service based on Tezzaron's SuperContact technology and GLOBALFOUNDRIES 130nm CMOS.

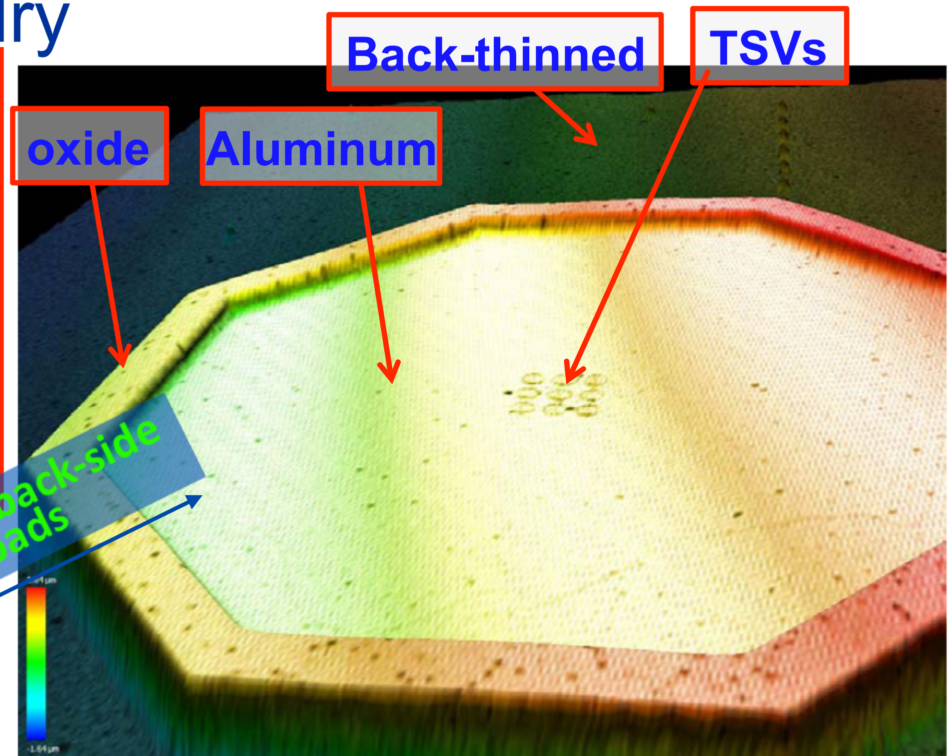
- 3D design kit built by CMP based on GF 130nm using data from Tezzaron, NCSU, Fermilab and others
- MOSIS concluded on positive outcome of the DARPA run and decided to carry out the submission for customers
- First MOSIS run taped out 11/2011 (CMP/CMC/MOSIS partnership) – still in fabrication, 3D bonding scheduled for fall 2012

3D-IC: post foundry

- Location of 3D bonding changed a few times IEM Singapore→ EVG Tempe, AZ→EVG Austria
- Back-side processing to Ziptronix, NC,
  – 1st time questionable
- Dies from bonded wafers delivered in 09/2012 showed shorts due to misalignment
- Recently 06/2012 received 2 bonded pairs
  - diced chips are operational, parts distributed
- lot of 18 extra wafers in bonding now



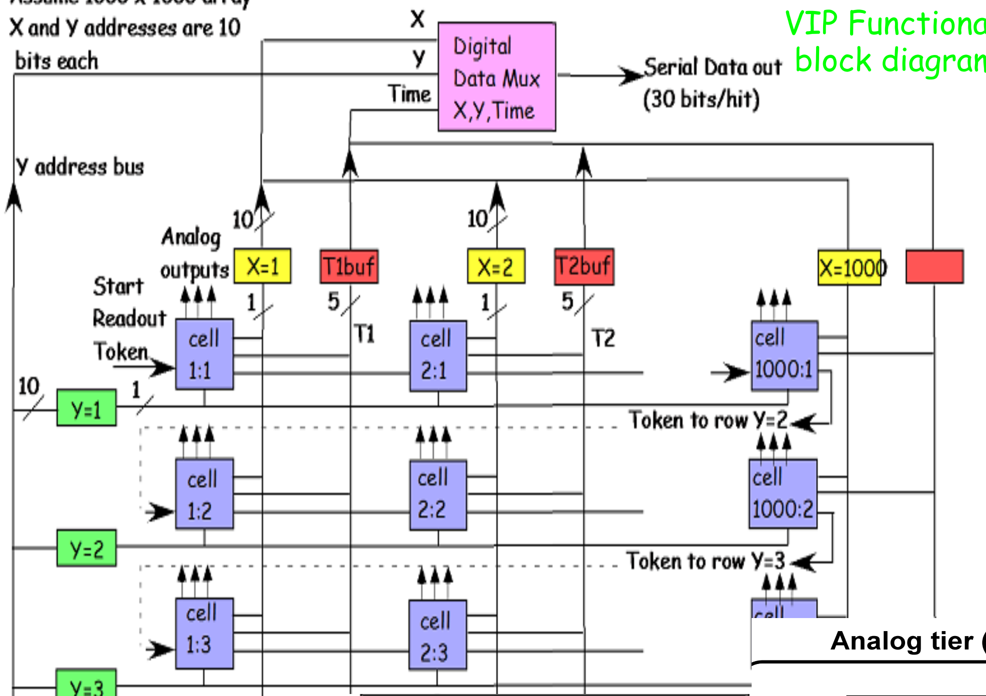
Cu TC Bond at EVG with 1st good 3D chips!



- **Main objectives of demonstration of 3D program has been achieved**
  (Cu-Cu TC and Cu-Cu DBI bonding), but:
  - limited number of available 3D dies
  - need to make a connection to sensors
- **Important**
  - Back-grinding down to TSVs' tips and full back side processing to create Al pads!

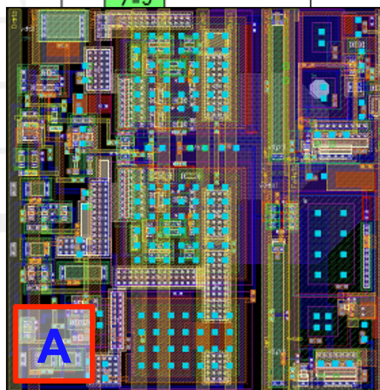
3D-IC: Fermilab designs – VIP2b

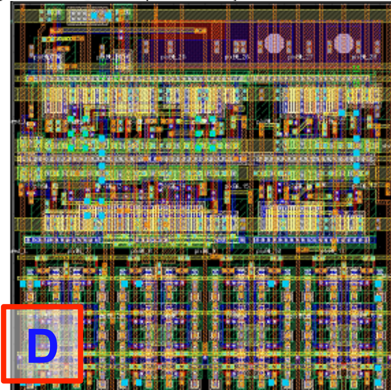
Low-power, low-mass, highly granular, sparsified readout pixel detector

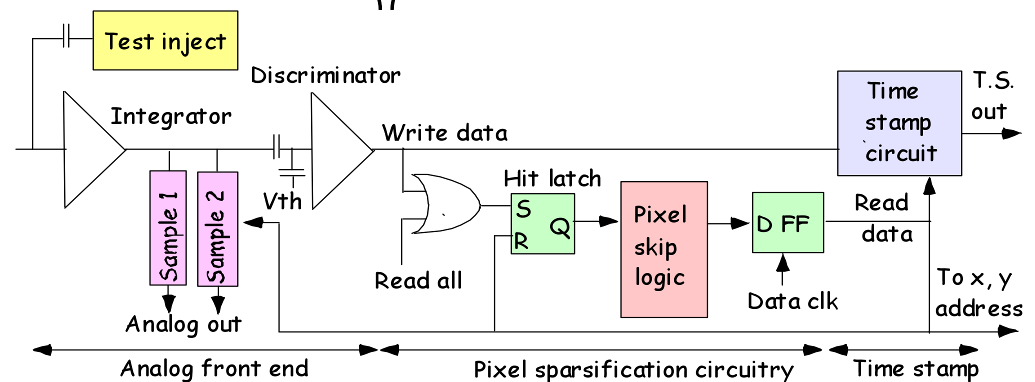


VIP Functional block diagram

- **How it works:**
  - 192 × 192 array of 24x24 μm^2 pixels
  - 8 bit digital time stamp (Δt=3.9 μs)
  - Readout between ILC bunch trains of sparsified data
  - Sparsification - token passing scheme
  - Single stage signal integrating front-end with 2 S/H circuits for analog signal output with CDS
  - Analog information available for improved resolution
  - Serial output bus
  - Polarity switch for collection of e^- or h^+

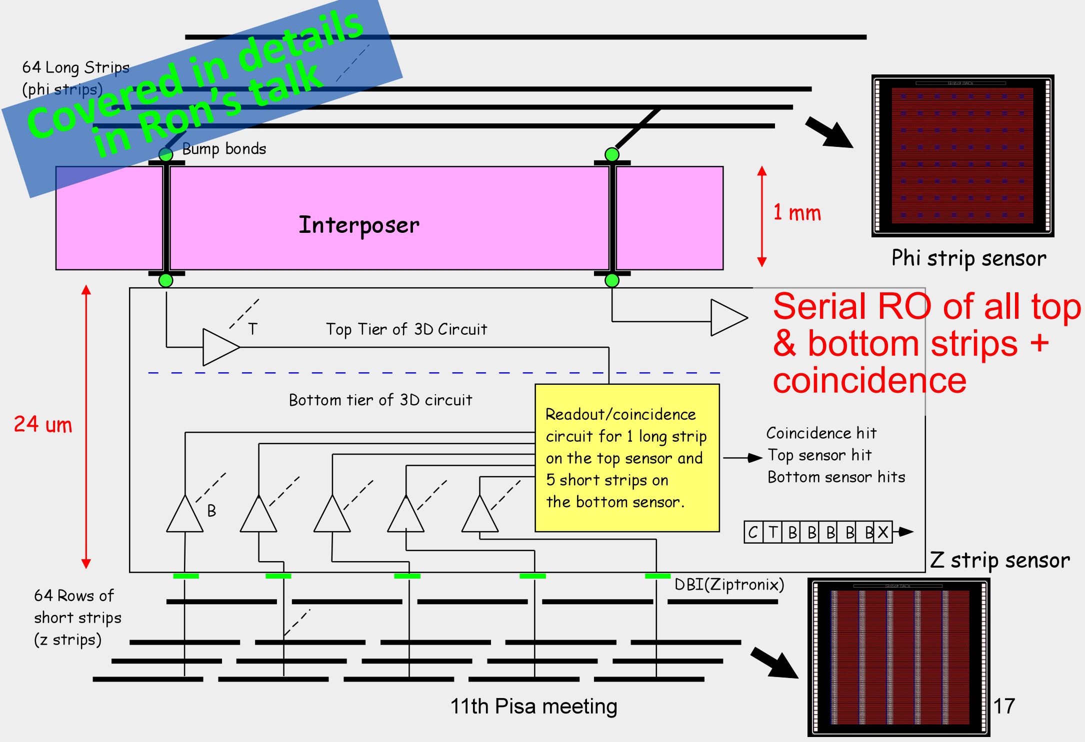






3D-IC: Fermilab designs – VICTR

Low-power, with in-situ processing, double layer of quasi pixel detector



Serial RO of all top & bottom strips + coincidence

COLLABORATIONS

- Long Strip Sensors / Interposer / Short Strip Sensors
- **Bump-bonding, UC Davis**
- **Interposer: Cornell, AllVia, Tezzaron**
- **Sensors/edgeless sensors: BNL, VTT**
- **IC design: LBNL**
- **3D ASICs with TSVs: Tezzaron**
- **DBI/fusion bonding: Ziptronix, T-micro, RTI**

- **uses slightly modified front-end from FEI4 (ATLAS) with a custom serial RO architecture**
- **Track-Trigger definitively needs 3D-IC technology – but may not need 3D ASICs**

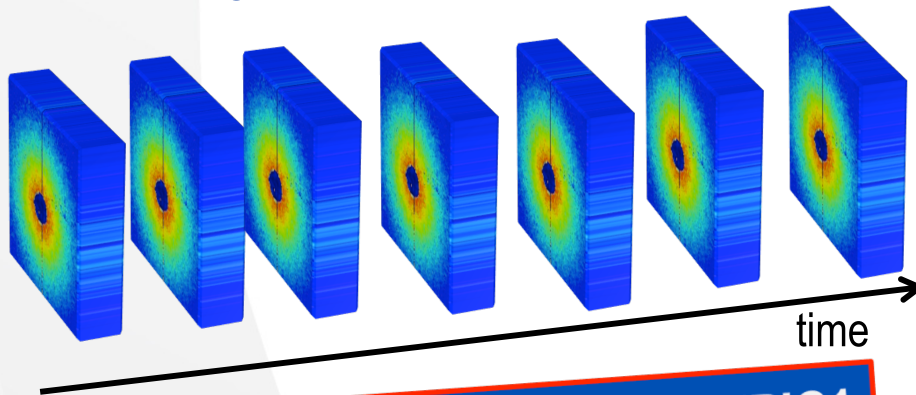
3D-IC: Fermilab designs – VIPIC

Low-power, time-of arrival and charge sharing corrected intelligent pixel detector

Vertically Integrated Photon Imaging Chip

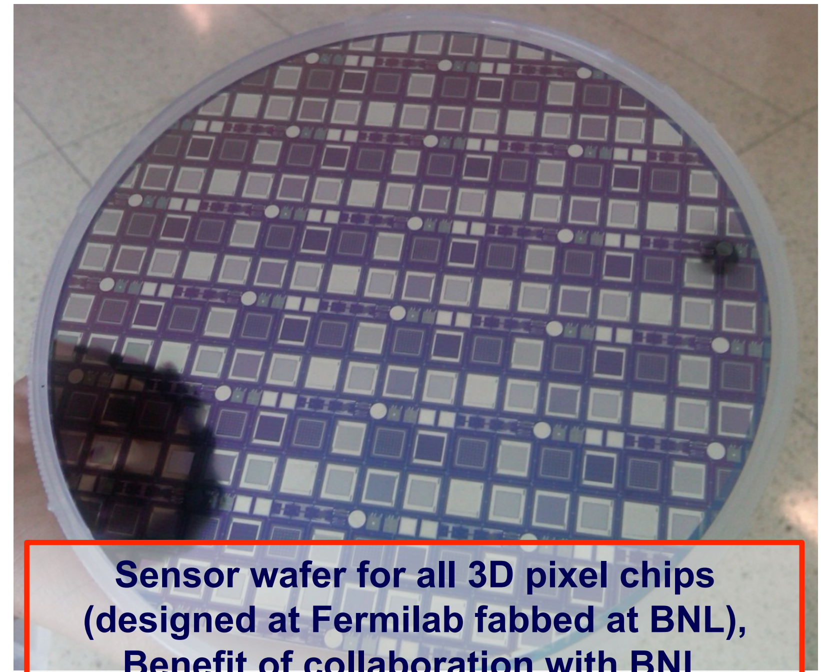
Detector: Si 500 μm thick sensors soft X-rays

Why?
- Immediate application in producing science with light source
- no comparable device available (2D autocorrelation @ ~10μs or better)
- Develop practices and techniques applicable later in devices for HEP
- Intelligent pixels (raw data not output, processing incl. inter-pixel communication)



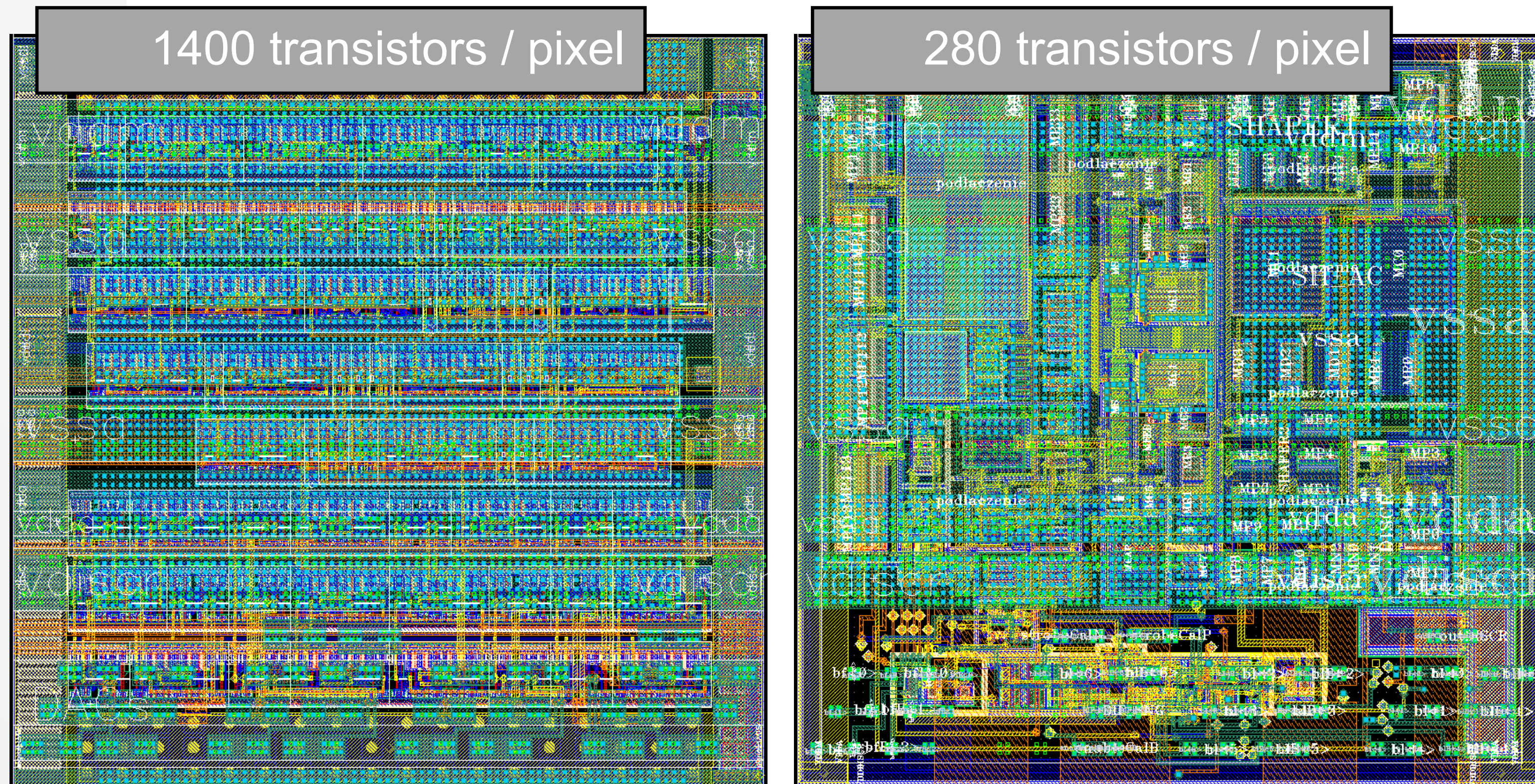
Beam and DAQ are ready for VIPIC1

Standard XPCS analysis: multi-tau correlator
Probes correlations between intensity fluctuations at times 0 and 0+t



Sensor wafer for all 3D pixel chips (designed at Fermilab fabbed at BNL), Benefit of collaboration with BNL

3D-IC: Fermilab designs – VIPIC



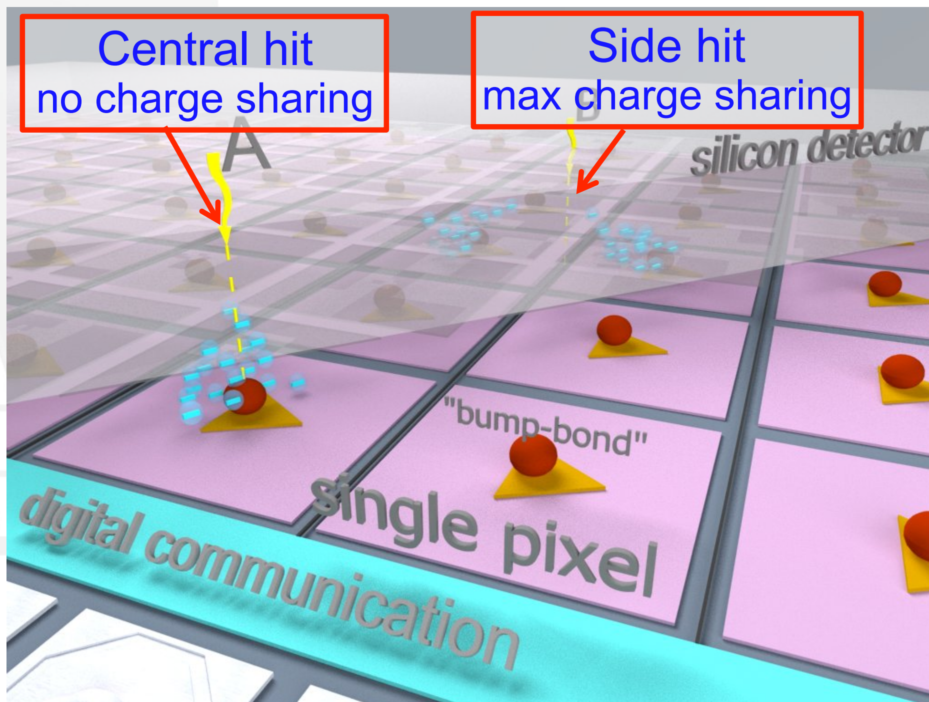
Digital part of pixel | **Pixel 80x80 μm^2** | **Analog part of pixel**

- **64 × 64 array of 80 mm²; shaping time τ_p=250 ns, power ~25 μW / analog pixel, noise <150 e^- ENC**
- **Two dead-time-less modes of operation (64 × 64 matrix / in 16 sub-matrices of 4 × 64 pixels):**
  1) timed readout of hits acquired at low occupancy (address and hit count) σ_t=10μs
  2) imaging – counting of events
- **Sparsified readout with priority encoder circuit (hit pixel address readout only)**

Intelligent pixels (VIPIC 1 / 2)

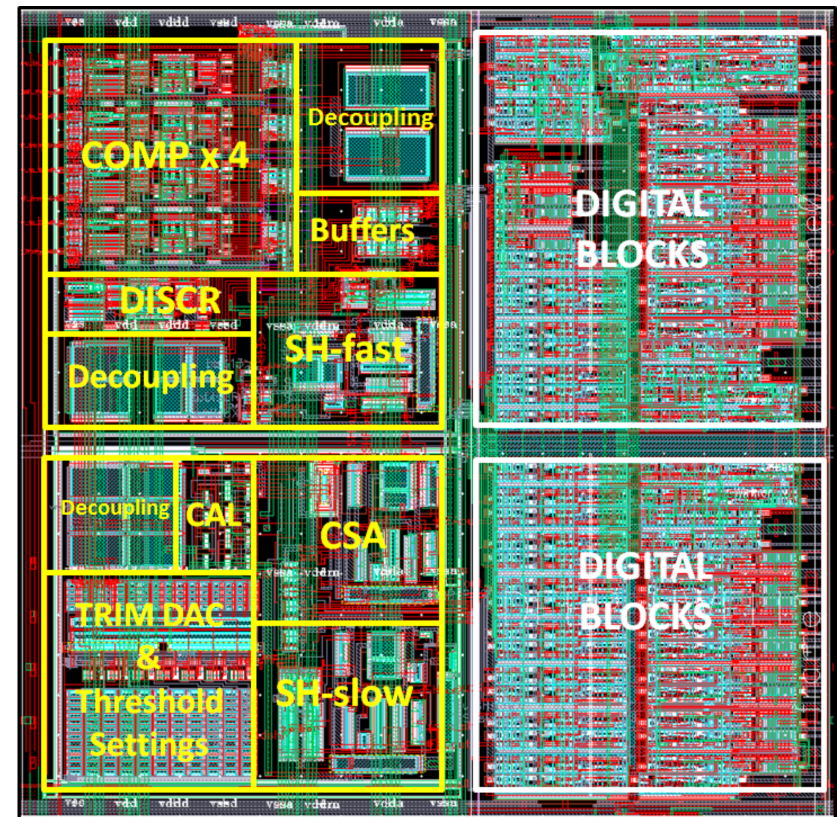
Pixel exchange data and detector processes information in situ outputting smaller quantity of ‘digested’ results

Ex. defeat charge sharing *(degrades DQE, amplitude and timing spectroscopic performances)* in X-ray detectors ➔ dynamic cluster reconstruction in tracking detectors



Development of new algorithm for reconstitution of full event charge

- Each pixel is an asynchronous processor (machinery), exchanging data with neighbors
- Applied directly in X-ray science,
- hardware cluster reconstruction

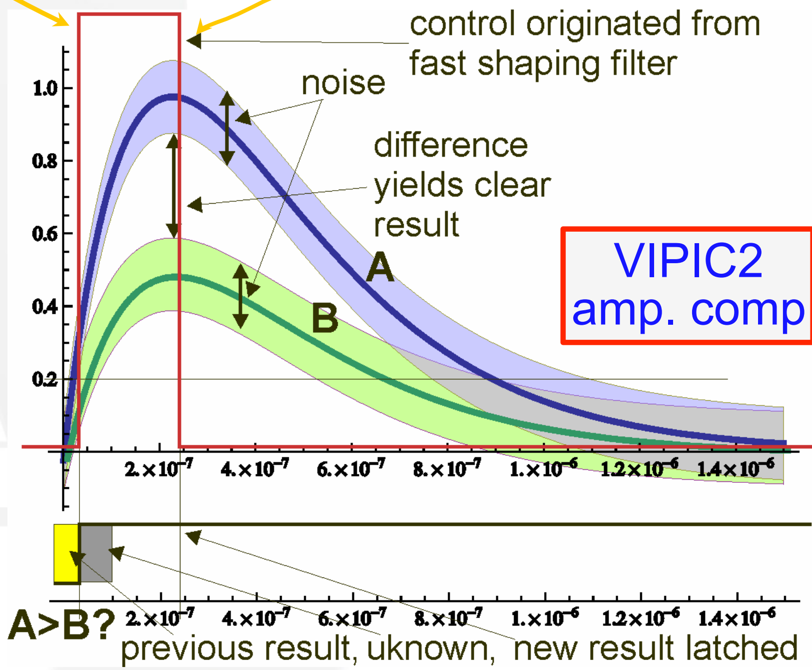


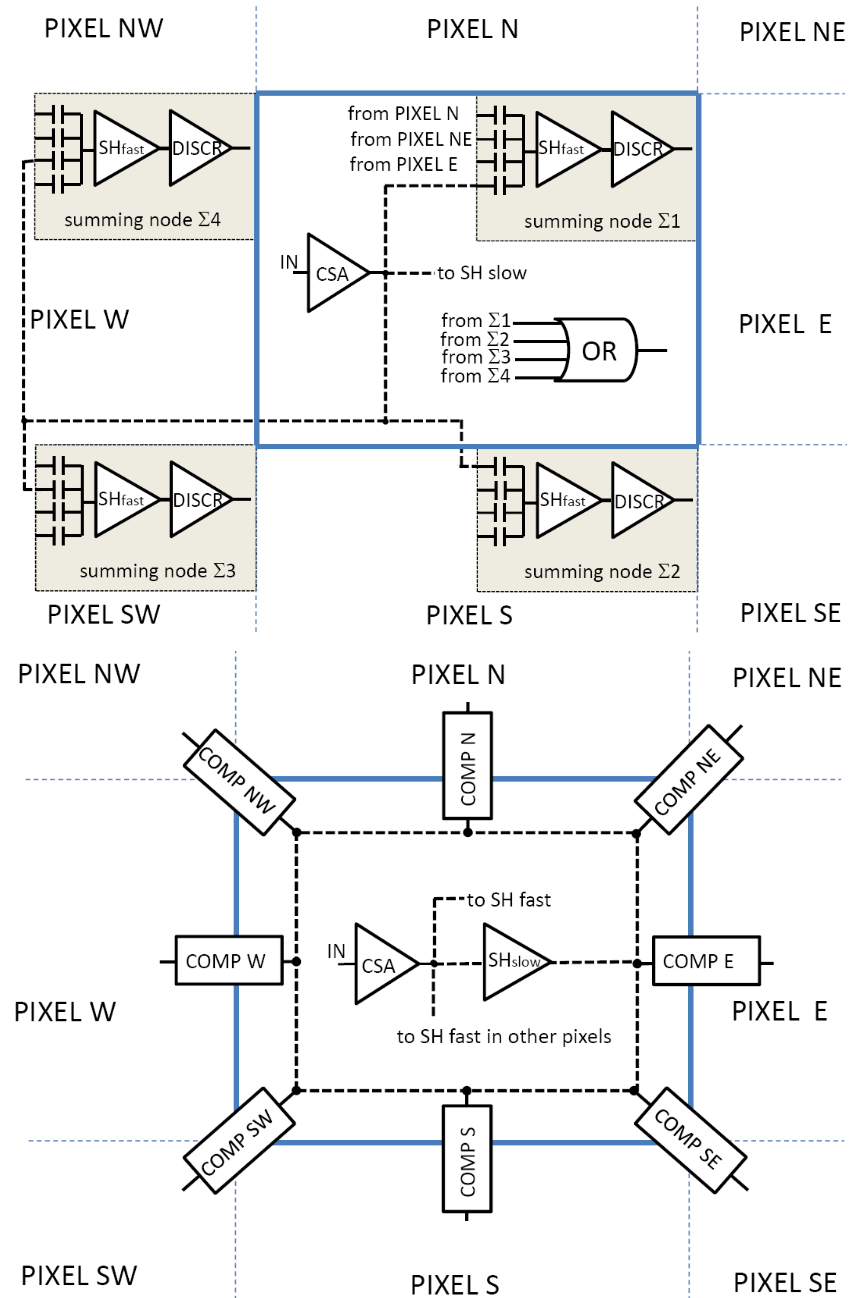
100×100μm^2, 130nm GF, 2k transistors / pixel

Intelligent pixels

C8P1 algorithm:

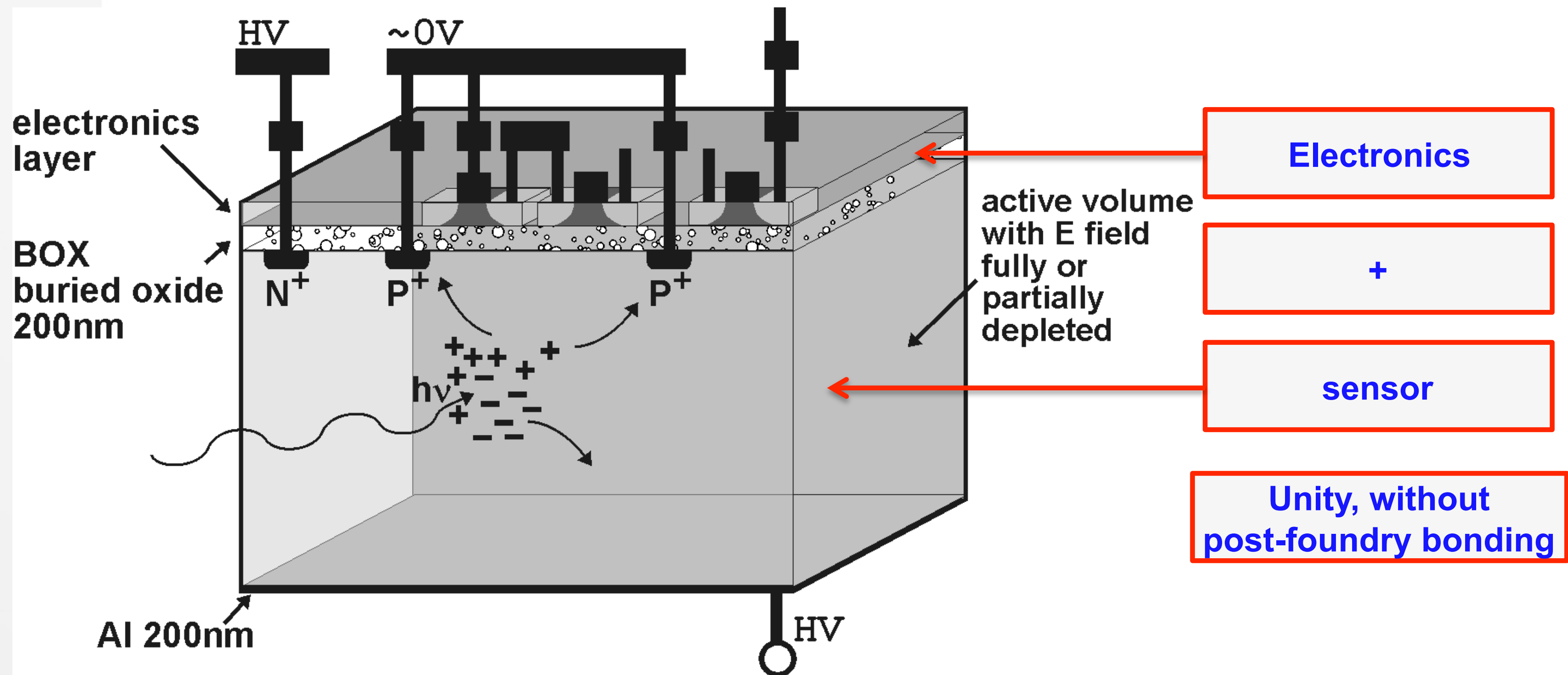
- Continuous summing of signals from neighbors in every pixel,
- Triggering on Σ>threshold performing all way comparators and latching one winning pixel (seed of cluster)
- miniVIPIC2 is 2D in preparation for 3D





Silicon On Insulator (SOI) pixels

- Collaboration established with KEK and under a Japan-US agreement (MoU 2007) on monolithic SOI devices + OKI/LAPIS (industrial partner).
- also domestically with ASI through SBIR



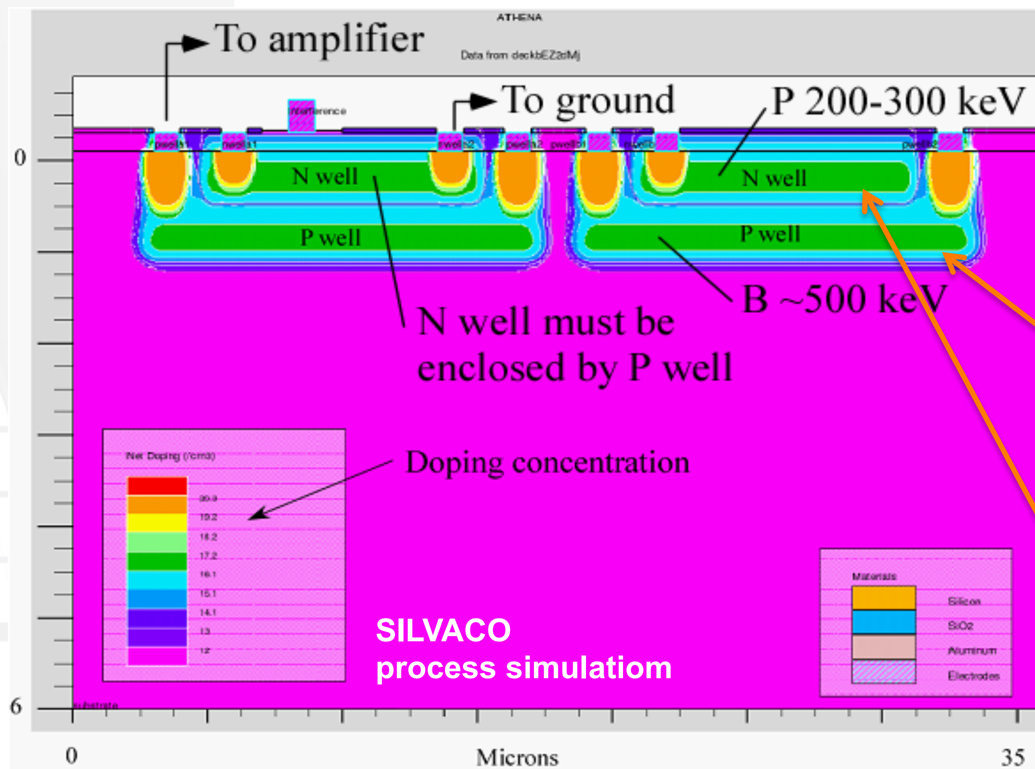
process was a slightly modified version of a commercial FD SOI process at the beginning

Suffering from strong back-gating and generally coupling between sensor and electronics

SOI pixels: Fermilab process improvement

– Triple role of shielding between the SOI electronics and detector layer:
- **to avoid back-gating in transistors** (DC potential underneath the BOX shifts threshold of transistors),
- **to avoid injection of parasitic charges** (from the SOI electronics to detector),
- **to avoid strong electric field in BOX** (that results in accelerated radiation damage).

improvement proposed by Fermilab



- Simulation with Silvaco
- Feature introduced in the design kit together with scientist from KEK and engineers from OKI/LAPIS

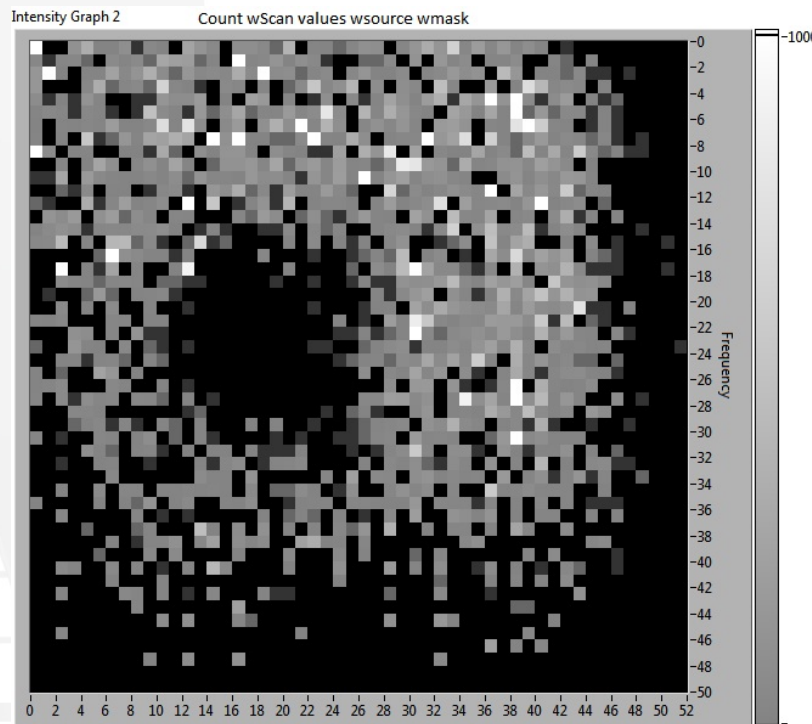
This well collects the charge carriers

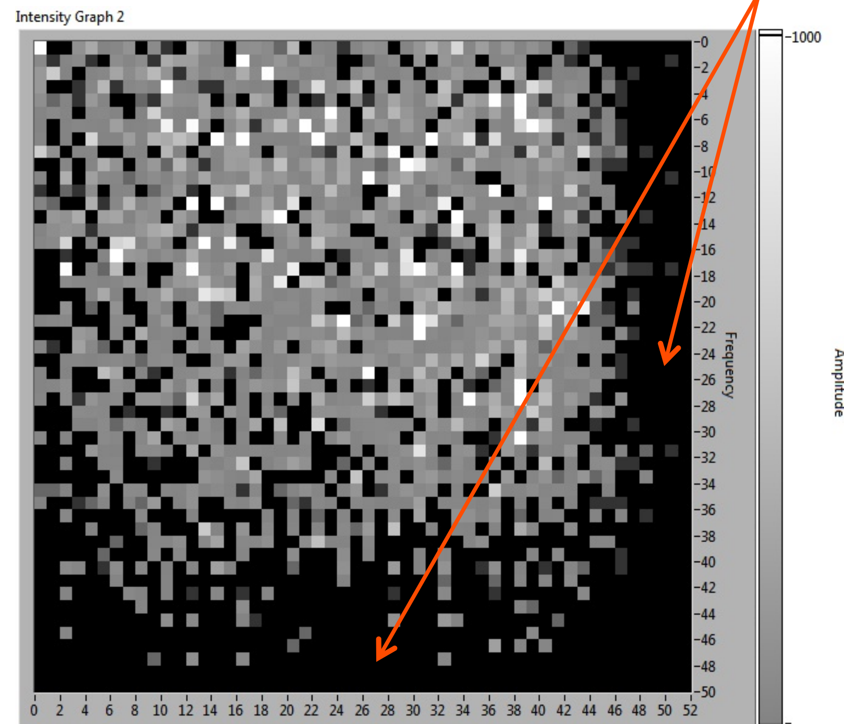
This well separates digital circuits from sensor substrate and prevents back gating effects

SOI pixels: Results

– **Started in 2006, a sequence of counting MAMBO chips developed:**
- gradually improve circuitry and understand better the technology
- dedicated resources are limited and risk to abandon this direction
- technology applicable for example in pixel upgrades for STAR at RHIC

First images obtained with counting (150ns) SOI pixel detector





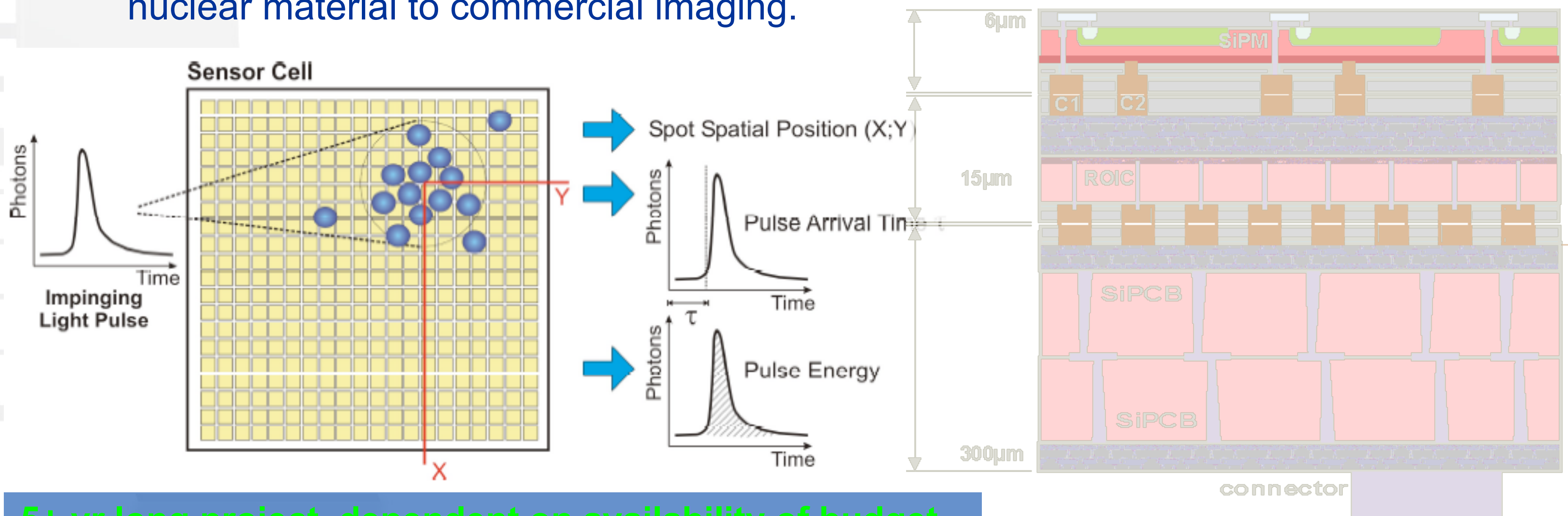
($1.9\times1.9mm^2$) square W mask **^{109}Cd source (22keV X-rays) with MAMBO 5 – submission cost covered by US-Japan funds** **flat field**

R&D on pixels: HL-LHC CMS upgrade

- Implementation target: 65nm CMOS process in collaboration with Italian INFN and CERN
- 2GHz/cm^2 hit rate at HL-CMS translates to event rate per pixel (50×100^{mm}m^2) >150kHz (approaching limits of nowadays direct detection X-ray systems!)
- Speed and maintaining low power are directions of R&D (to maintain <1% of pile-up durations of analog signals must be less than 100ns)
- Current benchmark in HEP pixels is FEI4 for ATLAS (LBL, UBonn, CPPM) – but its architecture has limits – thus decided to explore:
  - Fast higher order filtering (to avoid pile-up, out of time hits and lower threshold)
  - Offset auto-zeroing comparators (to avoid real estate hungry trimming DACs and to simplify)
  - Per pixel clock-less ADC (to convert to digital in situ at low power and allow further digital processing)
  - Explore architecture with arbitrary form hardware cluster recognition
  - Study pixel size that would explore different experimental conditions CMS vs. ATLAS (mag. field)
- Exploring common design element between ATLAS team to:
  - Exchange experience, evaluate synergies
  - Conclude on merging developments into one ROC or maintain two concepts if reasonable and advantages are clearly identified
- Target prototype submissions in 2013 (shared among participants)

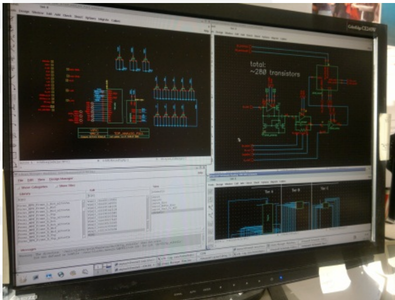
R&D: 3DDigSiPM if funds for new strategic R&D

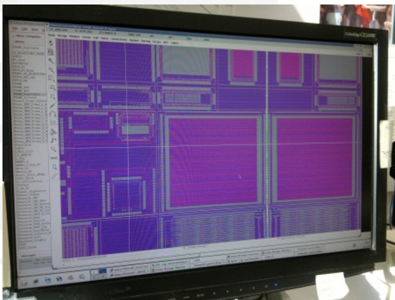
- Develop a novel type of fully digital, scalable photonic component capable of detecting single and multi-photon bursts, their time-of-arrival, intensity and position with high efficiency and purity (single photon detector)
  - optimized sensors and electronics (large area using advanced techniques developed for 3D-IC),
  - digital per pixel electronics (masking noisy pixel and obtain best timing),
  - Leverage experience and privileged access to 3D-Ic techniques working with companies (Tezzaron, Ziptronix, ASI, SVTC, and other).
- Establish technological procedures, as a toolbox for advanced detectors whose use may range from HEP, medical imaging, material science, detection of special nuclear material to commercial imaging.



5+ yr long project, dependent on availability of budget

Resources: EDA/CAD tools





- **Cadence – main frame**
  + Mentor Graphics – Silvaco (and Magma + Tanner)
  - tools selected from various vendors to ensure only strictly necessary functions, no advanced analyses and facilitations in design process available; guidelines:
    - common environment frame and affordability
  - adv. technology nodes <100nm are strongly tools linked,

strategic moves:
adaptation to 65nm needs included

- Shifting from Cadence IC5.1X to IC6.1X *(all new designs under IC6.1X OA) – (underway),*
- Optimization of access to XL (VSE and ADE) and GXL (VLE – VCAR but not VSR) features through license tokens in Cadence IC6.1X - *(2010)*,
- Migration from Eldo (Mentor Graphics) to Analog-Mixed-Mode Simulation (AMS) with Spectre (Cadence) – *(2011),*
- Solicitation for: ASSURA PVS, VSR and VDI (budget dependent) – to be capable of 65nm flow - *(2012)*,

Resources: instruments

- **ASIC test lab spaces**

  + "clean room" (probe stations /one capable 8"/ and measurement instruments)

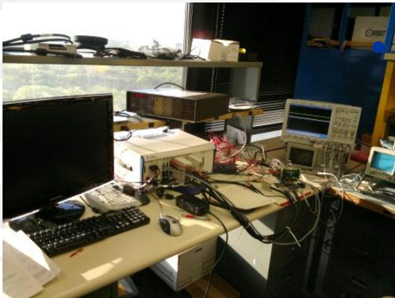
  + 2 labs (FlexRIO National Instruments systems and test equipment + lab. radioactive sources)

  + robotic chip testing station (upgrade)

  + manual bonding station

  + PCB components mounting lab

ASIC test la



bench NI test setu

strategic moves:

- Requisition of two PXI/PXIe FlexRIO National Instruments digital and analog (ADC,LVDS,CMOS,DAC,DMM,power, etc.) systems based on LabView – to fulfill hardware needs for testing of chips
- DC-3GHz spectrum analyzer – intended for noise measurement bench – crucial but needs development!
- Other instruments: static parameter / LCR / Logic / network analyzers/ V / I source, pA, digital oscilloscopes, etc.

comment:

- Instruments are becoming outdated; some are not up to current measurement standard and procedures – needs addressing

Conclusions

- Solid-state detector instrumentation ⇔ ASIC + sensors → physics data,
- Valuable resources are: people' skills, science environment and collaboration
- Interesting R&D projects with the challenges were found allowing becoming leaders in new areas like 3D circuits,
- Working in R&D collaborations, like SOIPIX, opens access to technologies and to groups of targeted interests; contribution of Fermilab is visible, however continuations are uncertain depending of resources and funding,
- Intelligent pixels direction for much higher level of in-situ processing
- Intensive work on strategic directions, ex.:
  - 3D-IC technology in a wide spectrum of scientific uses
  - HL-CMS pixels upgrade and tracking-triggering
  - Technology development like 3D Dig SiPMs
- Challenge is to keep up (education) with progression of μelectronics in industry
  - Desirable to establish PhD in EE/Device Physics following the CERN model of 'CERN PhD" and/or other schemes for students
- Investment unavoidable in CAD/EDA
  - Challenging to maintain collaborations in areas : digital design / automated chip floor-planning / mixed mode automation, and challenging to maintain leadership position while certain tasks are out of reach, like tasks in nodes <100nm