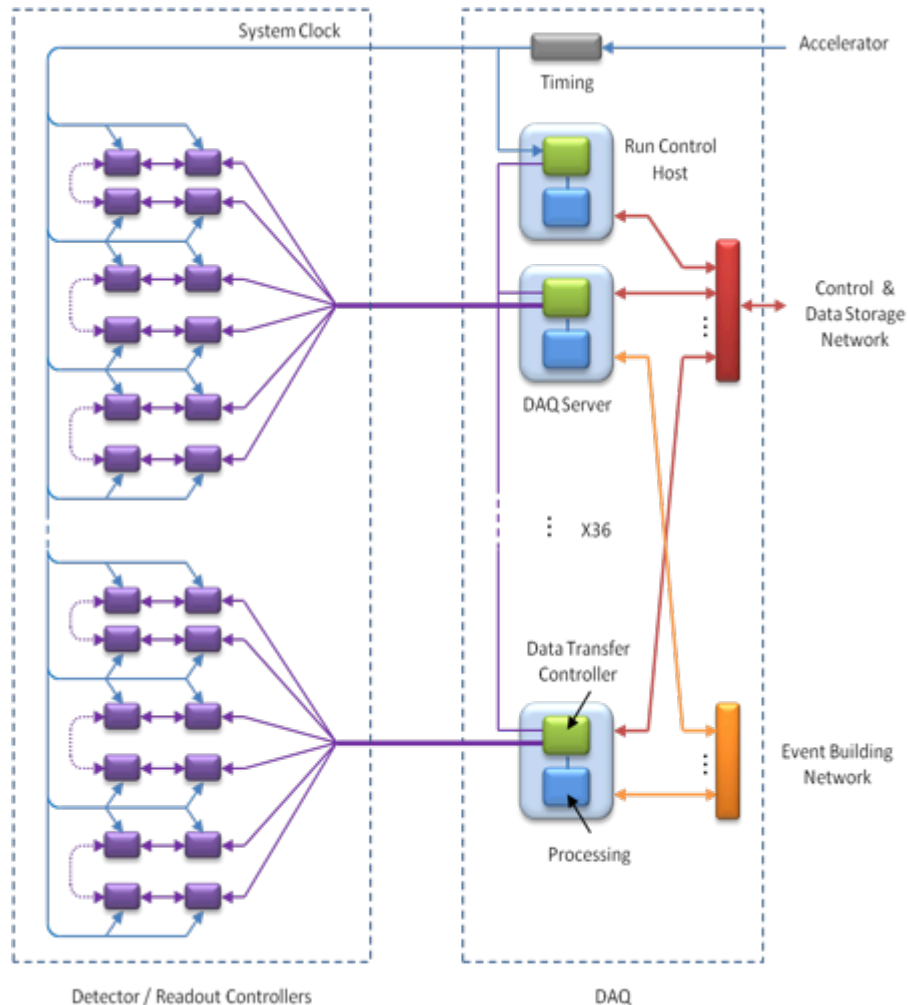# Mu2e CD-2 Calorimeter Waveform Digitizer

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October 23, 2014
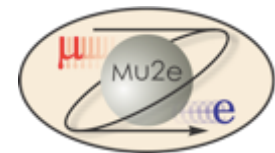
Mu2e DAQ system

- DAQ architecture supports both streaming (Tracker, Calorimeter) and triggered (CRV) readout

- DAQ Servers handle data readout, event building and processing

- Bidirectional front-end interface for fast control and readout

- Large front-end buffers for uniform data transfer
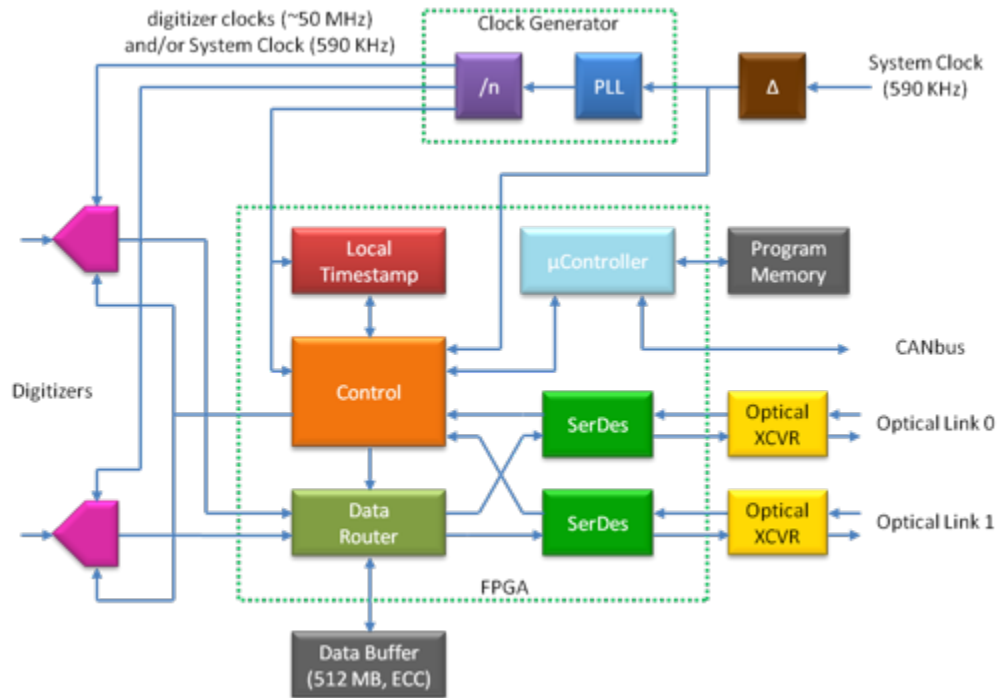
Mu2e DAQ system (Tracker example)
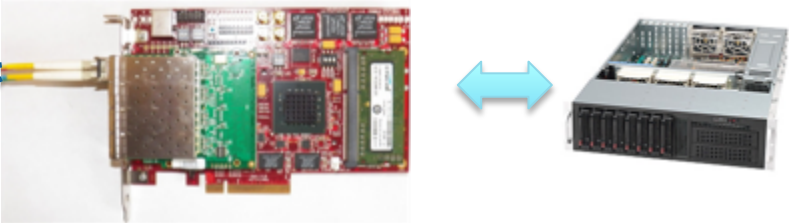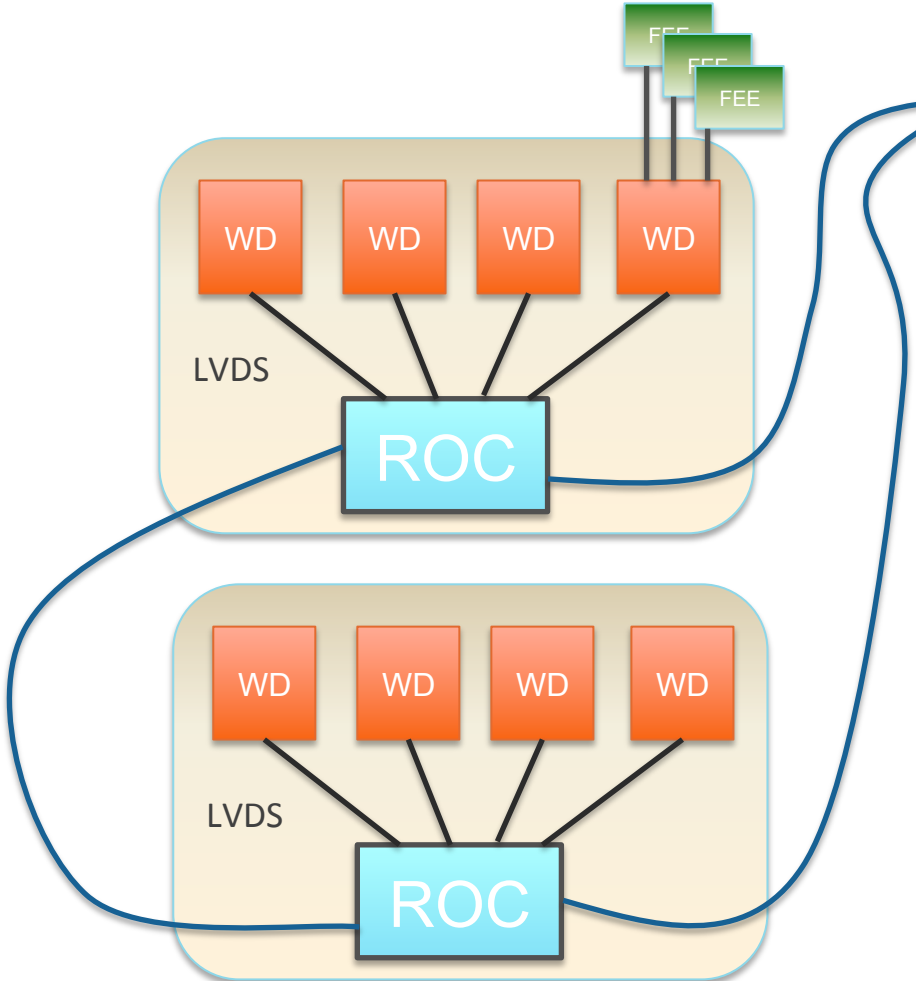
- FEE amplify and generates the signals
- Waveform Digitizer (WD) performs: digitalization, pedestal suppression, sparsification and compression
- ReadOut Controller (RoC) receives data from WD and write them in a huge buffer (~ 1 s od data)
- Data are transferred to the DAQ during the supercyccle period (500 ms beam-on, 830 ms beam off)
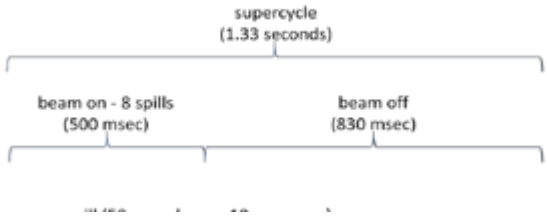
Roc

- Readout Controller:
  - WD interface
  - Optical redundant connection throw DAQ servers (2.5 Gbit, 8b/10b)
    - Slow control
    - Timestamp
  - Can be linked in daisy chains (rings)
  - Project and specifics (hardware + firmware) under study @ FNAL for the tracker
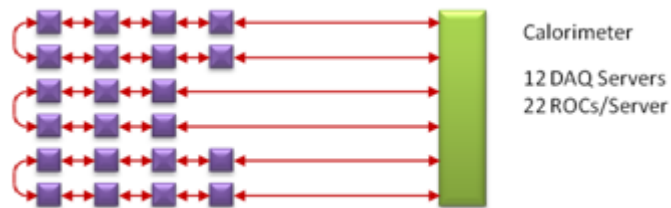
- Calorimeter will use 22 links (22 rings)

Calo WFD bandwidth and specifications

- 1860 crystals, 3720 channels (APD, SiPM, …)
- BaF_2 : signal width ~ 50 ns , 200 mV → ADC sampling 200 MHz 12 bit.
  - 10 samples per signal, 20 con safety margin 2 after zero-suppression
  - Mean occupancy after zero-suppression 20% → 40 kHz rate
- 3720 (chan.) x 12 (bits) x 20 (samples) x 40,000 (hits/s), corresponding to 35.7 Gbps + header + slow control (10 %) → 40 Gbps
- 22 links @ 2.5 Gbips (3.125 encoded) → 55 Gbps → bandwidth is OK

- The FPGA will be the core component of the WD board. It will:
  - Drive the ADCs control signals to synchronously get all the samples
  - Write the data to a DDR memory. Data will be sent to the DAQ in the inter-spill period. Read data from the DDR and serialize them
  - The WFD will be daisy-chained in rings. Each FPGA will thus receive data from the previous WD, add its own data and send them again to the next board
  - Slow control commands will be received and served by the FPGA through the same fibers used for data

Calorimeter DAQ

- Tracker needs lots of logic on the digitizers, because it implements TDC on FPGA => backplane + ROC + 6 WD (7 FPGA "microsemi" / 96 channel)
- Two options under study for the calorimeter:
  - ~ tracker
  - ROC logic +analog + ADC on the same board/FPGA

🎔 **Fermilab**
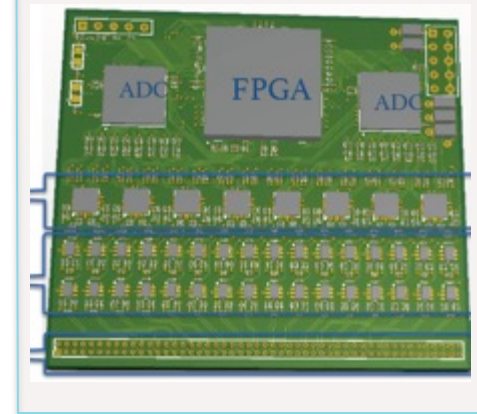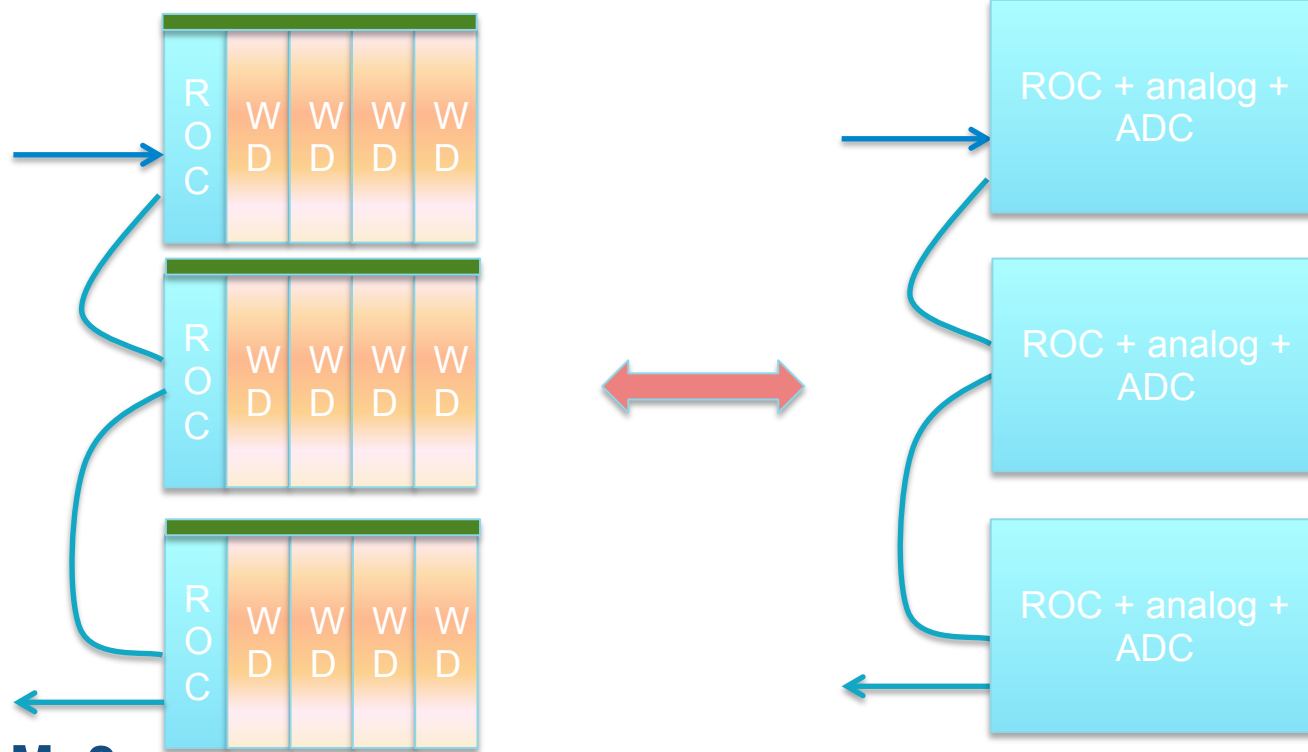
Calorimeter DAQ 2

- "SuperRoC" option is preferable (one project, no links needed between boards…)
  - Studies underway for taking the final choice:
    - No options for Soc: **Microsemi SmartFusion2 M2S150T**
    - Board dimensions constrained by the distance between the two calorimeter disks (max allowed 15 x 15 cm^2)
    - Max number of boards imposed by the adopted mechanics
- Single board option OK if:
  - Board dimensions fit in the mechanics
  - FPGA logic sufficient
- Number of boards depend on the final # of channels choice:
  - 16 ch → 232 boards (our baseline goal)
  - 32 ch → 116 boards (if achievable)

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Mechanics

- Electronics housed in crates (custom or standard) behind the disks
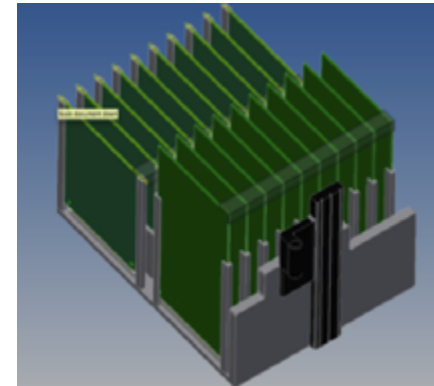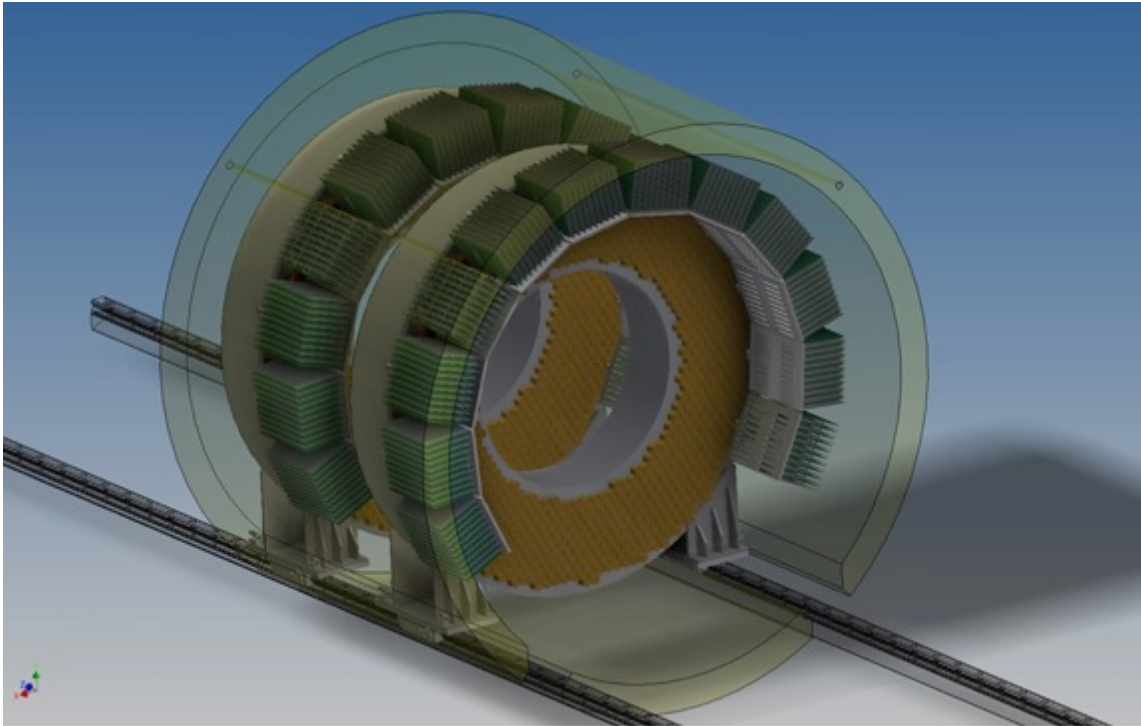
Mu2e environment

- High magnetic field (1T) → problems for magnetic nuclei of DC-DC converters

- Radiation (not too high but present) 100-1000 rad/y and high neutron flux (~1000 cm^2/sec) → select rad-hard components
  - FPGA (Soc) SmartFusion2 M2S150T is flash based, so no SEU
  - ADC used in the prototype ADS58C48 must by qualified

- All the electronics is in vacuum → degassing problems and need to use only conductive thermal dissipation.

- Maintenance complicated → cryostat will not be opened more often than once per year

Project must be realized in "high reliability mode",
like an experiment in the space

DC/DC

- High efficiency needed, but high magnetic field present. It is not so easy to implement it.

- FNAL technical devision is developing a DC/DC converter in B field (air inductor in air). Work is in progress. It will be used also by the tracker system.

- INFN R&D (CSN-5) dedicated program has selected a commercial DC/DC converter which works on B-field and seems to satisfy the Mu2e requirements. Validation of this new DC-DC converter underway.

Prototype Digitizer PCB (1)

Prototype Digitizer PCB Block Diagram
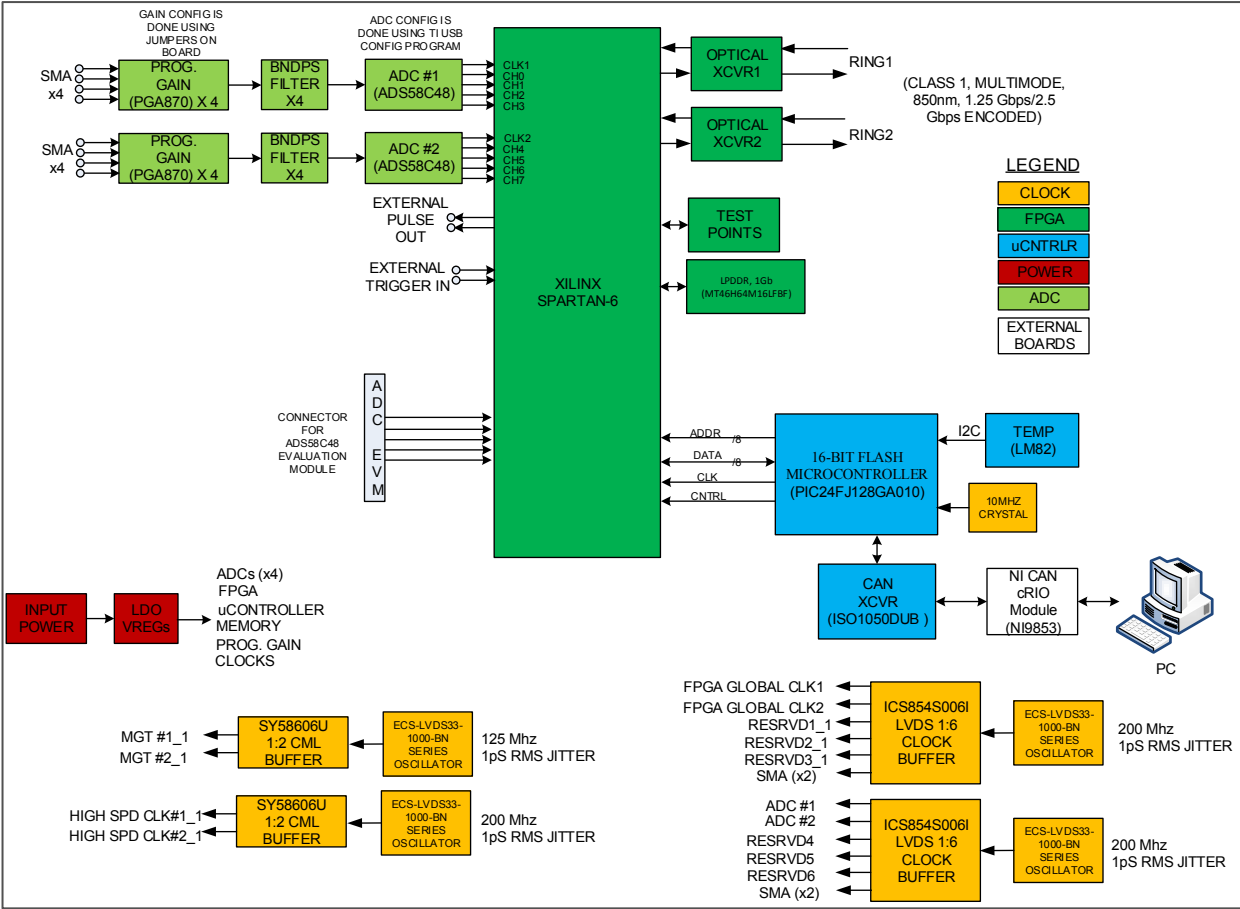
5 boards of 8 channels/each with 200 msps and 12 bit ADC resolution constructed at University of Illinois. SOC: Xilink Spartan 6

Prototype Digitizer PCB(2)
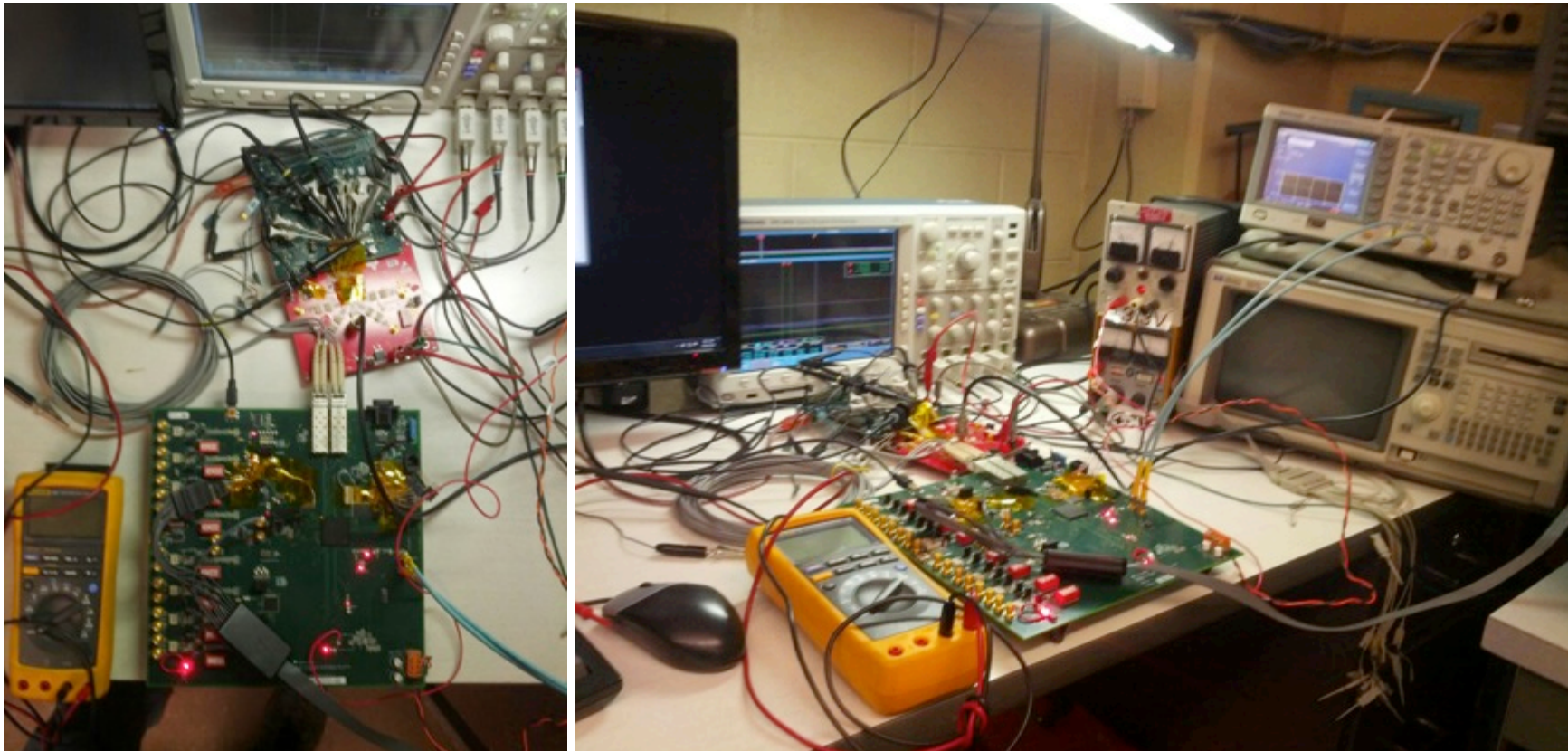

Pictures of the test setup for the digitizer at the University of Illinois

Prototype Digitizer PCB (3)

- **Testing and FPGA firmware development is ongoing.**
  - Hardware Subsystems Testing:
    - Hardware subsystems on the board are being tested for functionality.
  - Rate Testing:
    - **Firmware being written to perform a rate test to verify digitizer can handle data rates needed for project.**
    - **Firmware will:**
      - Upon receipt of a "Start Trigger" signal, capture 10 samples of 11-bit, digitized data from 8 TI ADS58C48 ADCs.
      - Convert the 11-bit data into 16 bit data.
      - Combine & serialize data from all 8 channels
      - Attach start of frame character and end of frame character to serialized data.
      - Send frame data out Fiber Optic Transceiver, transmitters.
      - Loopback optical frame data into Fiber Optic Transceivers, receiver.
      - Compare frame data sent with frame data received, & assert error (light on-board led) if communication errors exist.
      - Count errors occurring during transmission of frame data.

Mu2e

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INFN short term Milestones

- 2014: in progress now .. usage of 2 demo boards smartFusion2 for doing preliminary transmission test via optical fiber

- 2015: realize a digitizer prototype and define the final factorization of the system, number and type of boards, number of channels, form factor.

- 2015: test all components @ high B field and high radiation environment

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475.07.05 Digitizer cost breakdown & estimate

Sum of Value	
Resource Type	Total
M Material	12
N Non-Fermi Labor	96
Grand Total	**108**
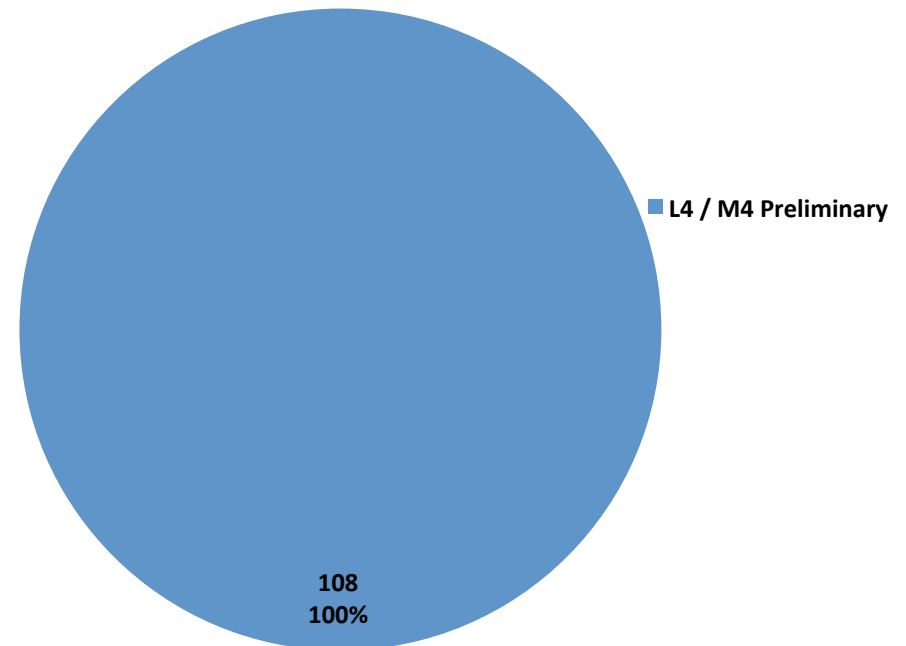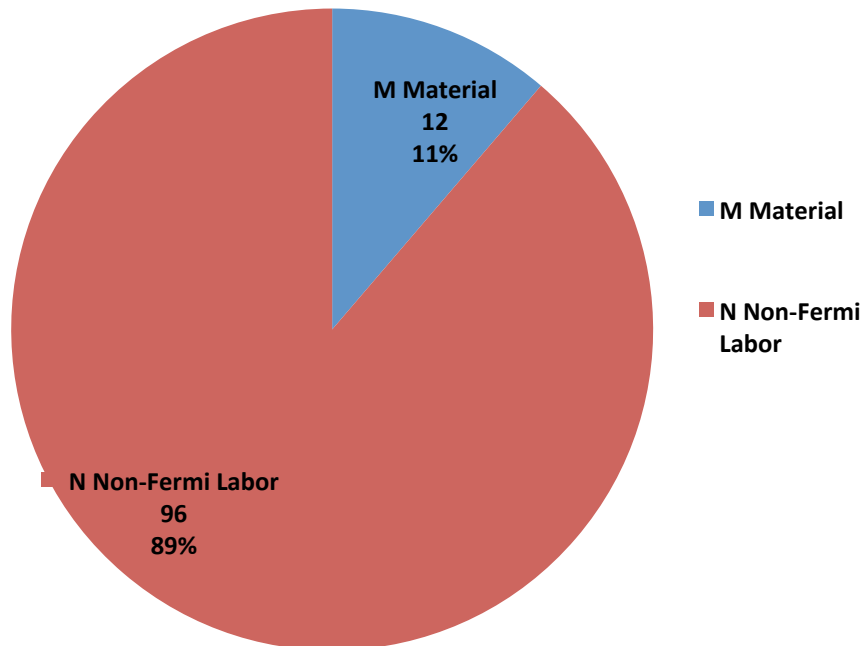
475.07.05 Fee & Digi Labour and Material

Sum of Value	
Resource Type	Total
M Material	12
N Non-Fermi Labor	96
Grand Total	108

G. Pezzullo – Mu2e CD-2 Calorimeter   7/8/2014

Mu2e   🔶 **Fermilab**
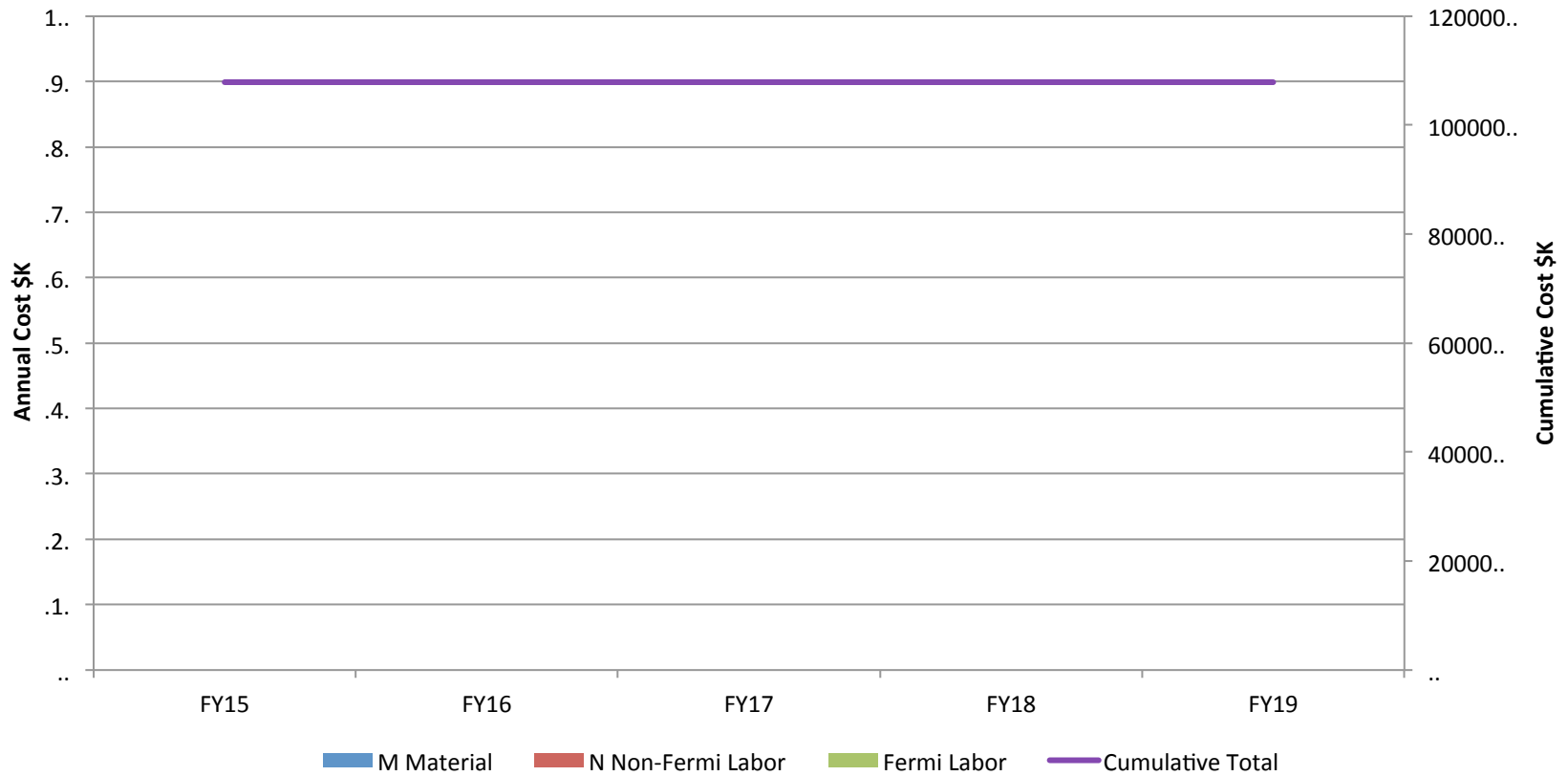
475.07.05 Fee & Digi FTE resources

Sum of Value

Resource Type	Total
M Material	12
N Non-Fermi Labor	96
Grand Total	**108**

AD Administrative — EN Engineering — ES Environmental, Safety & Health — FM Facilities Management — IT Information Technology — SC Scientific — TE Technical — Cumulative

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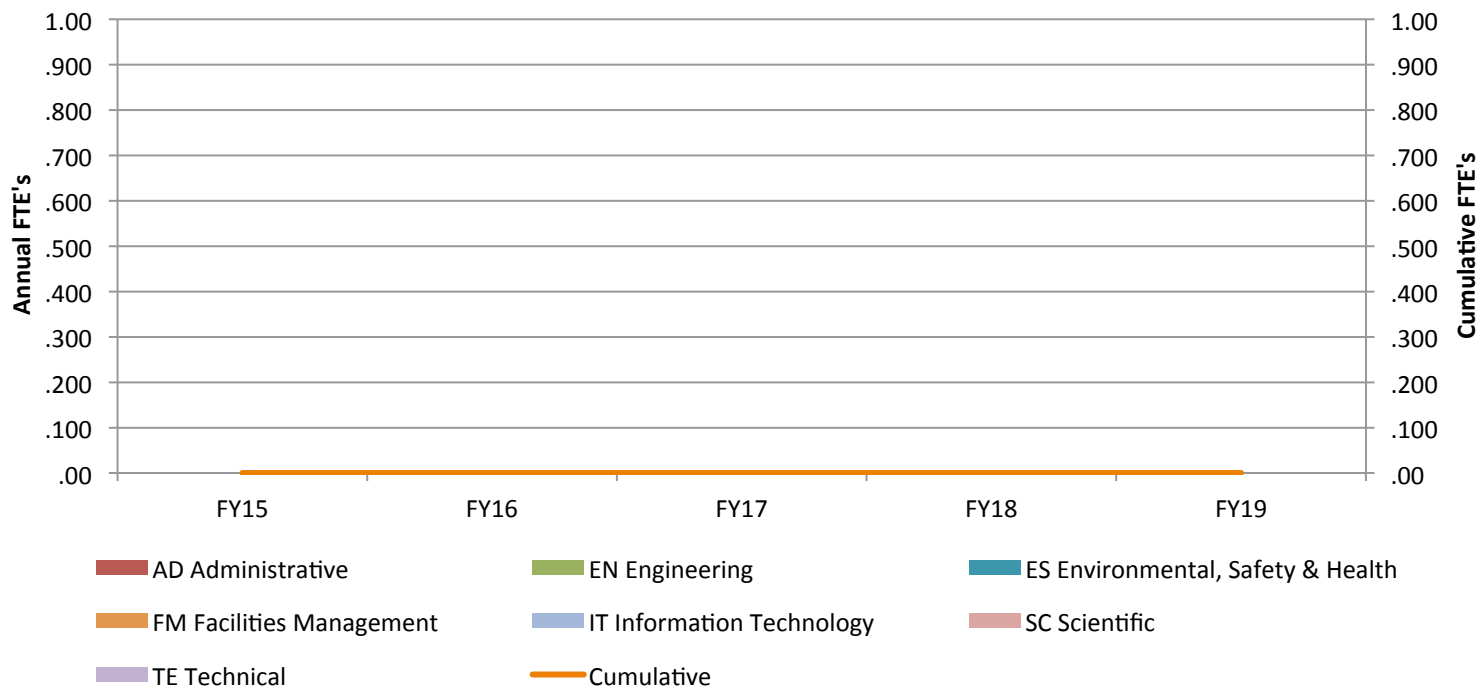
ADDITIONAL MATERIAL

Extra Slides…

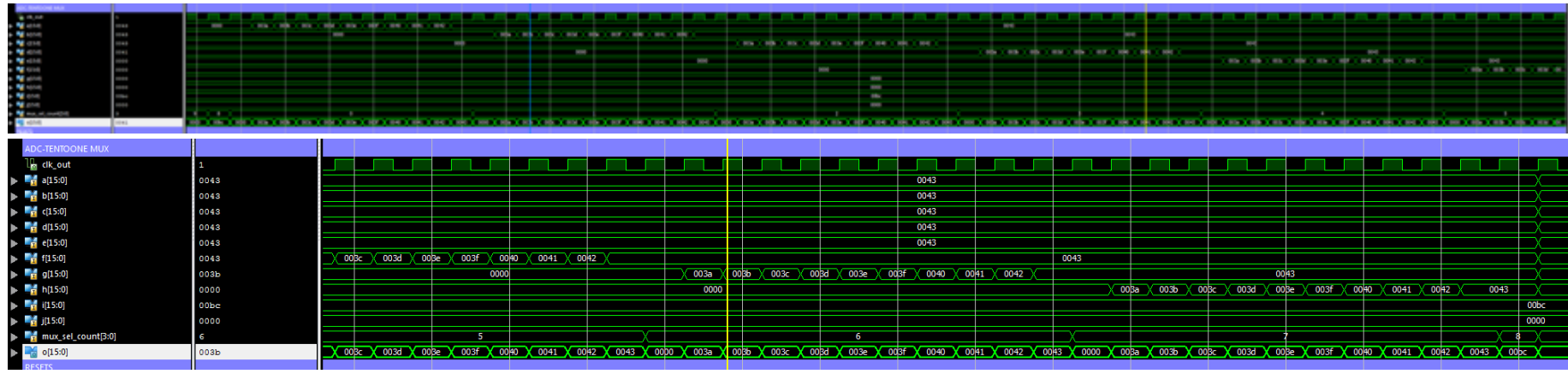Behavioral Simulation screen captures of data going into & out of ten_to_one_mux module

Post-Route Simulation screen captures of data going into & out of ten_to_one_mux module
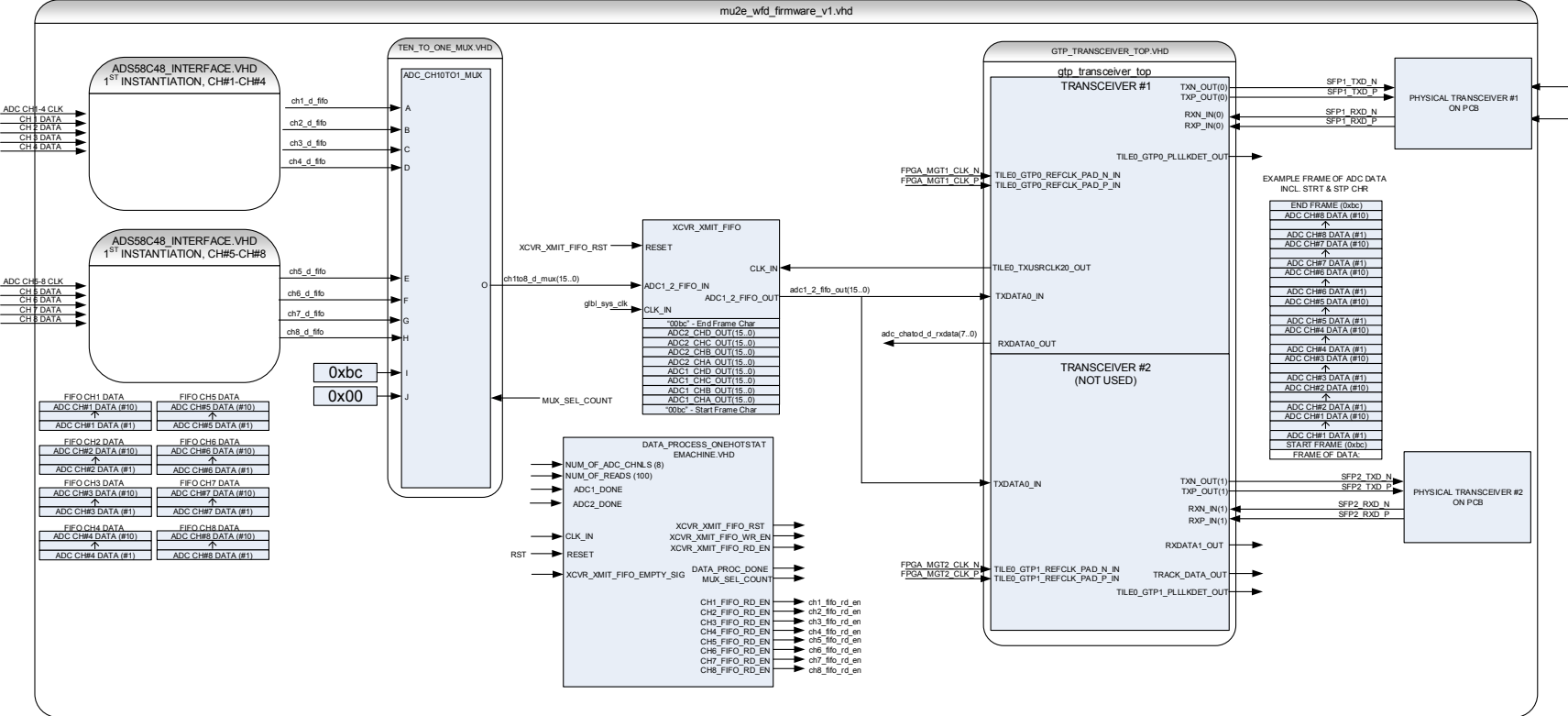
Mu2e

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Extra Slides…

Logic Analyzer Screen Capture Showing All 'Ones' being outputted from ADC
(0b 111 1111 1111 => 0x3e, 0x3f)
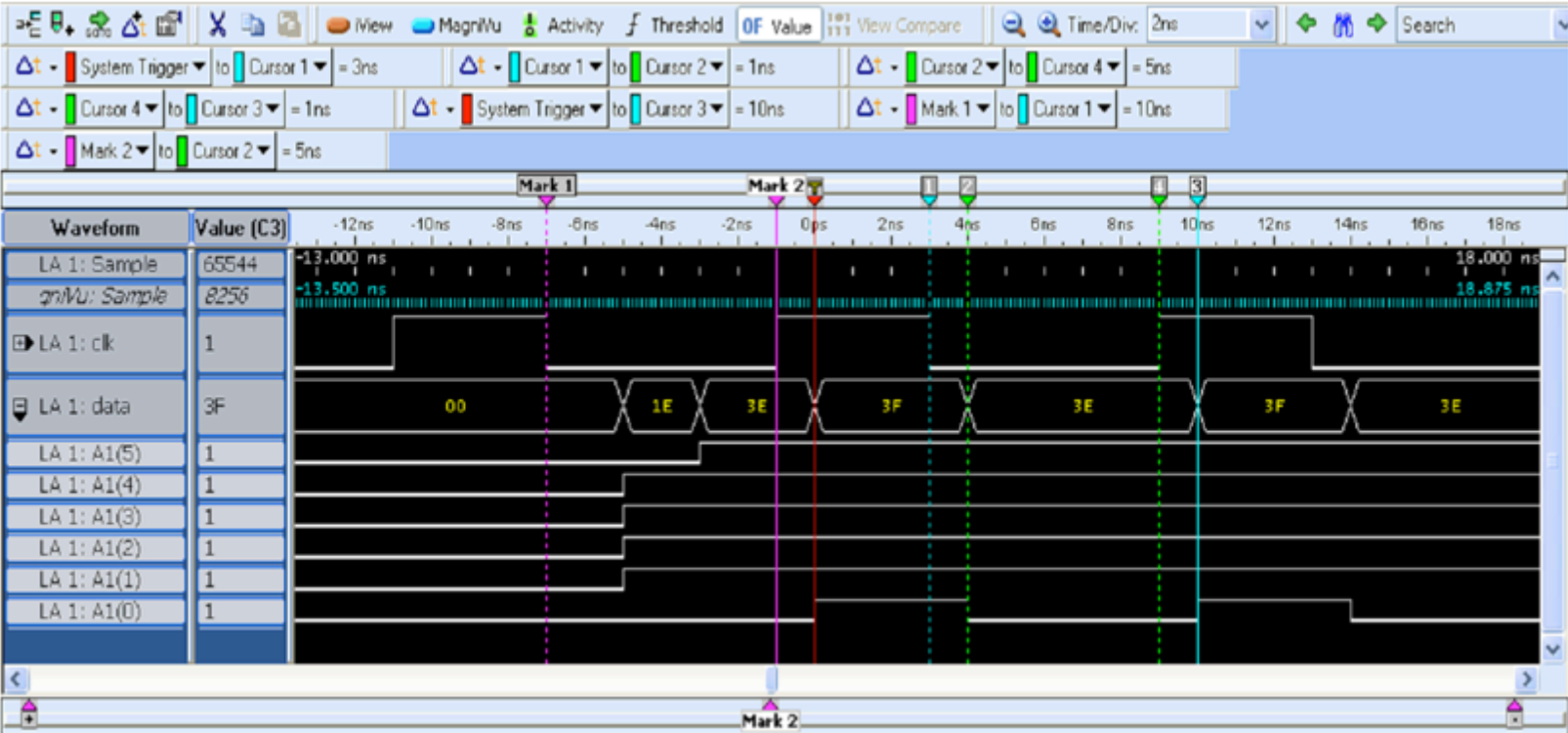
Preliminary studies: Prototype Digitizer PCB

Block Diagram of Rate Test Firmware, Version 1
(Written in VHDL)

Prototype Digitizer PCB (4)

- Rate Tests:
  - First, write VHDL firmware to perform rate test @ 1.25 Gbips.
    - Firmware is currently being written & tested.
      - Firmware has passed functional simulation.
      - Firmware has not yet passed post-route simulation and is under development.
        - Post-route simulation has passed sending correct data through ten_to_one_mux module(see picture on previous slide).
        - Post-route simulation for FIFO & Transceiver is currently under development.
      - Firmware won't be programmed into FPGA and tested, until it passes post-route simulation.
  - Second, write VHDL firmware to perform rate test @ 2.5 Gbips.
    - Test has not been started yet.
    - Use the code from 1.25 Gbips test.
    - Increase the clocks to capture data at a faster rate.
    - Change transceiver clock & settings to increase output to 2.5 Gbips.

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Preliminary studies: Prototype Digitizer PCB

- Hardware Tests:
  - First, write firmware (VHDL or ANSI C/C++) to test each subsystem.
    - Optical Transceiver, ADCs, Clocks have been tested and are functional.
    - Microcontroller, & CAN Interface are under development.
    - Memory has some code written, but not complete or have been tested yet.

  - Second, verify ADC data output format is well understood.
    - Use Texas Instruments ADS58C48EVM, evaluation module & Prototype Digitizer PCB to understand ADC data output format.
    - ADC data output format is understood and can be applied to rate test firmware.

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Preliminary studies: Prototype Digitizer PCB

- Rate Testing (Cont.):
  - Firmware Development Workflow:
    - Write code.
      - Fix syntax errors.
    - Perform Behavioral Simulation.
      - Fix logic errors.
      - Iterate, until it passes Behavioral Simulation
    - Perform Post-Route Simulation
      - Fix Timing Errors.
      - Re-write code.
      - Iterate, until it passes Post-Route Simulation
    - Program FPGA & confirm code works in hardware.

    Ie. Upon receipt of "Start Trigger" signal, will board capture data from 8 ADCs, digitize, serialize, and be outputted correctly @ 1.25 Gbips & 2.5 Gbips?

Preliminary studies: Prototype Digitizer PCB

- Hardware Subsystem Testing:
  - Tests are done to verify that each subsystem is working properly.
  - Firmware either has been or has to be written to correctly perform the hardware tests.
  - Subsystems being tested are:
    - FPGA programmability
    - ADCs
    - Clocks
    - Optical Transceivers
    - Microcontroller
    - CAN Interface
    - Memory