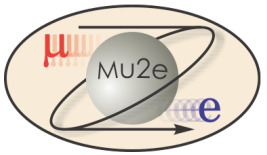
Fermilab

Mu2e CD-2/3b CRV Electronics



Sten Hansen

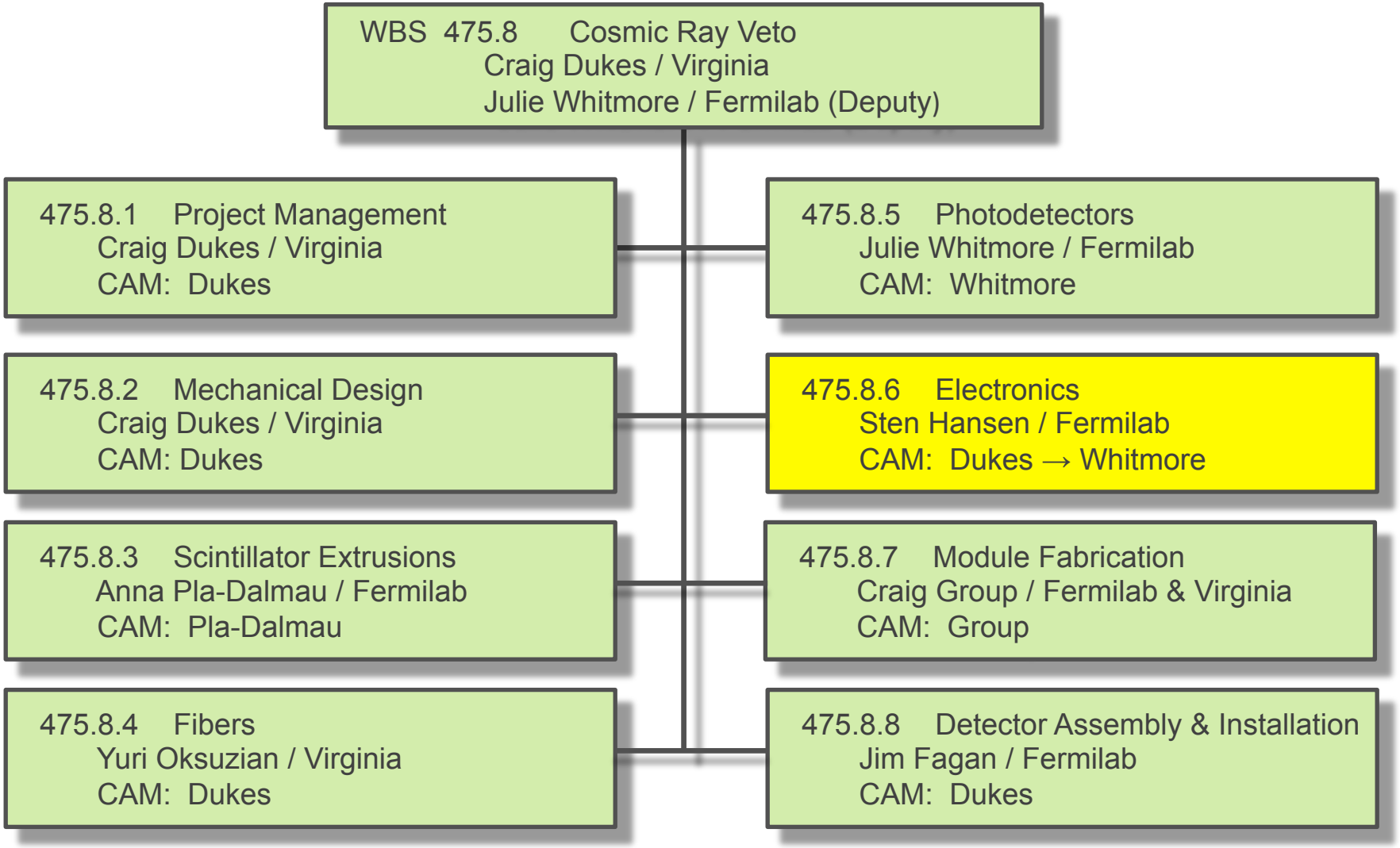
CRV FE Electronics Level 3

10/21/2014

Experience

- 36 years at Fermilab
- In the last couple of years:
  - Warm side electronics for CDMS
  - Beam position monitor system for the Linac
  - Beam Intensity monitor for the SeaQuest experiment
  - Wire chamber TDC system for test beam facility

Organization



Requirements

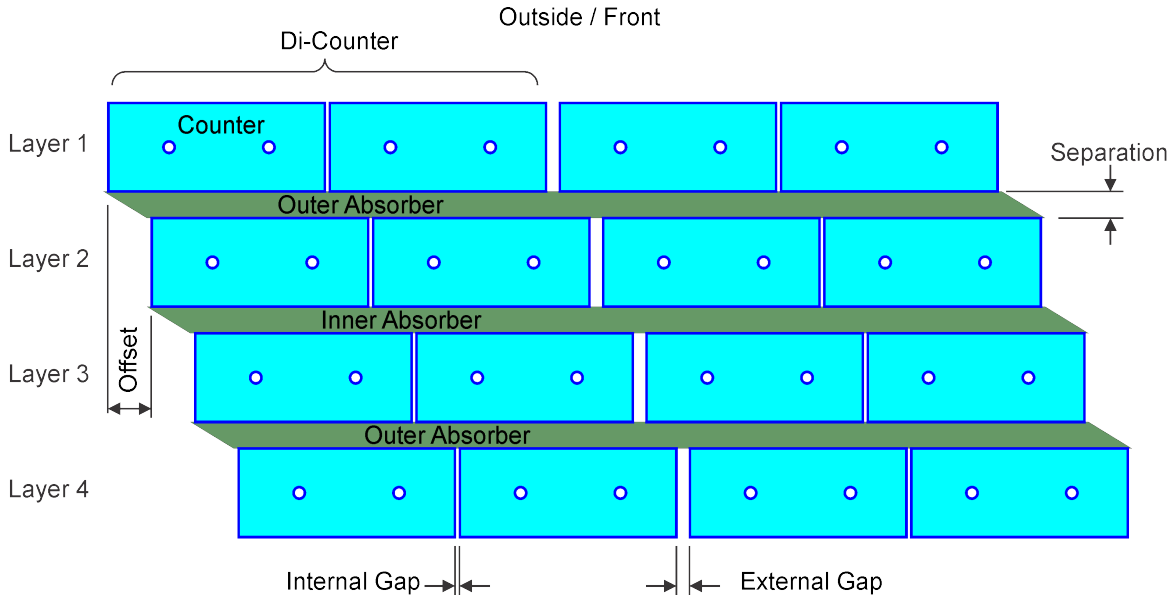
- The requirements for the Cosmic Ray Veto are described in detail in Mu2e-doc-944.
- Fundamental (detector independent) requirements:
  - To reduce the conversion-like background from cosmic rays to less than 0.1 events over the course of the run
  - To provide a cosmic-ray trigger primitive to the DAQ
  - Not to contribute more than 10% experiment dead time → accurate timing
  - Not to use more than 20% of the DAQ bandwidth

Design

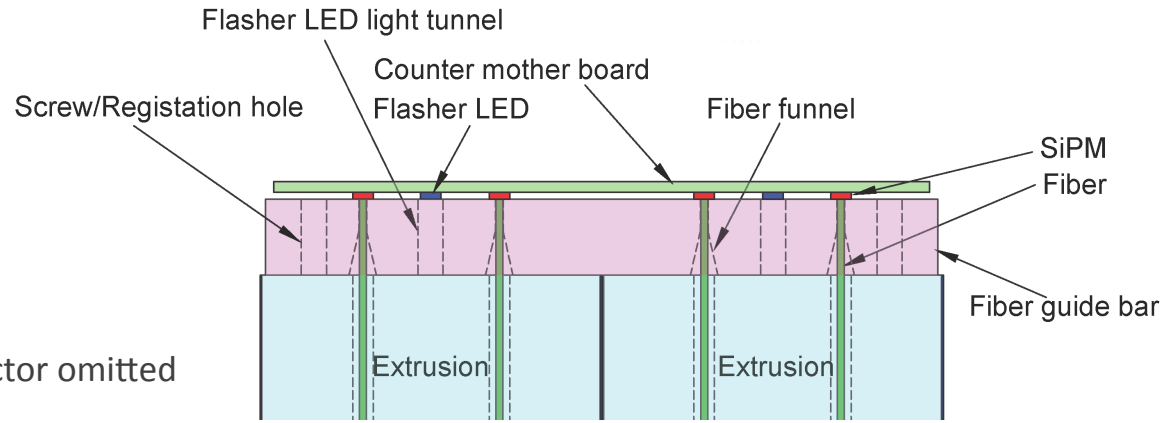
- There are three board types in the system:
- A counter mother board (CMB) which holds four SiPMs, two flasher LEDs, flash gate switches and a temperature sensor.
- A front-end board (FEB) which digitizes the signals from 64 SiPMs.
- A readout Controller (ROC) which gathers data from and supplies power to 24 front-end boards over Cat-5 cables. Interfaces to the DAQ/timing/control system.

Design

Extrusion Arrangement :



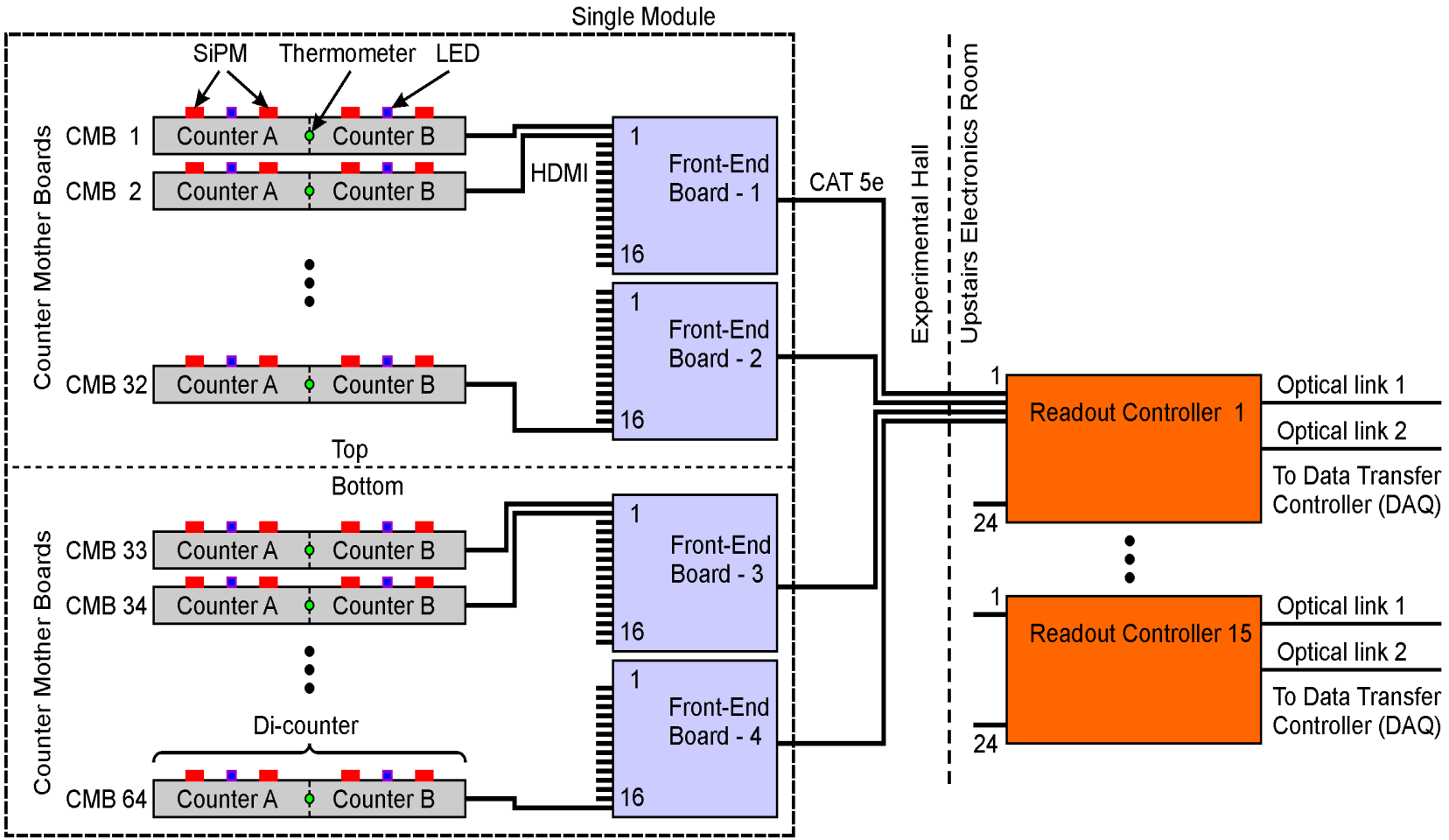
Counter motherboard:



HDMI connector omitted

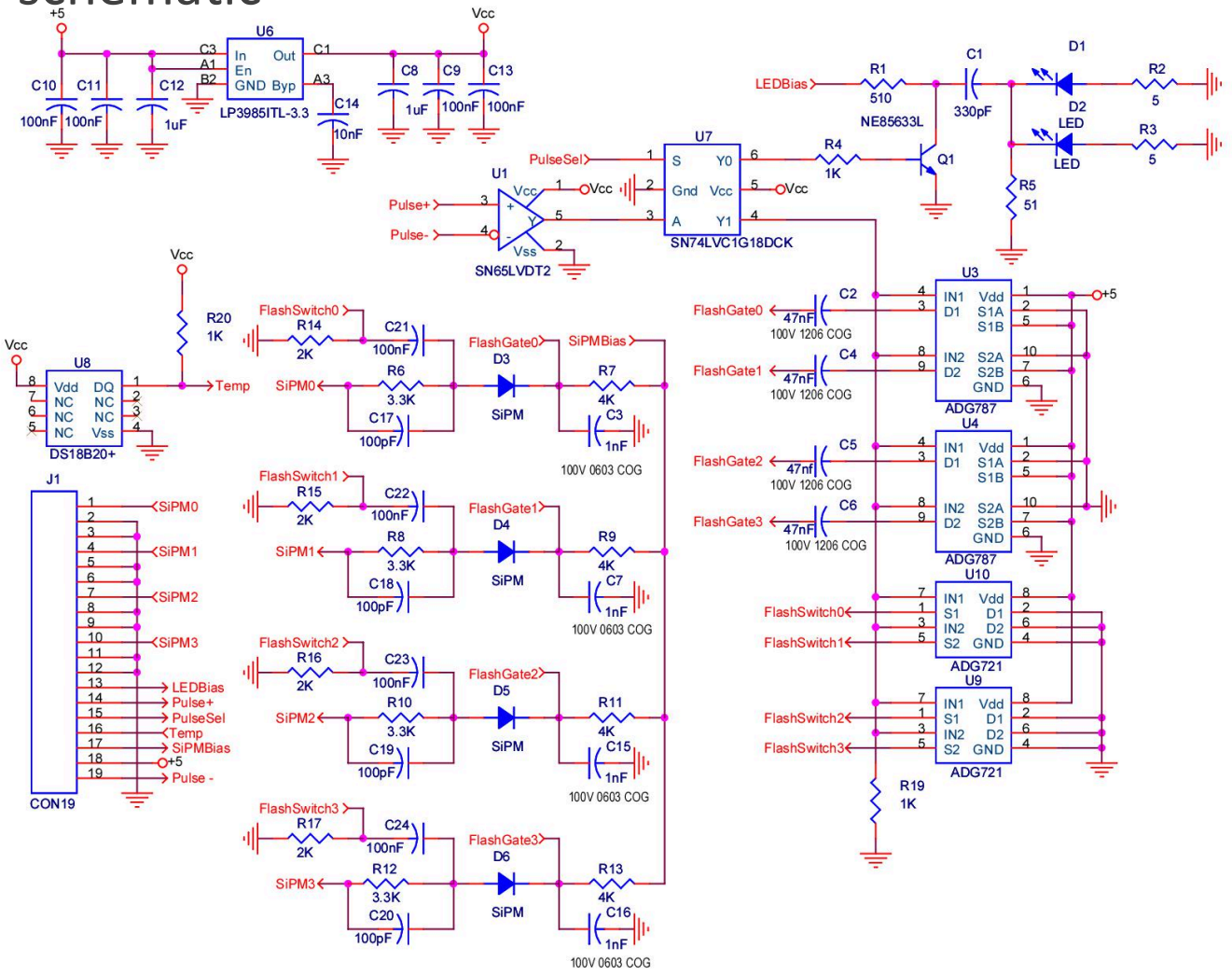
Design

Diagram showing interconnection of all three board types:



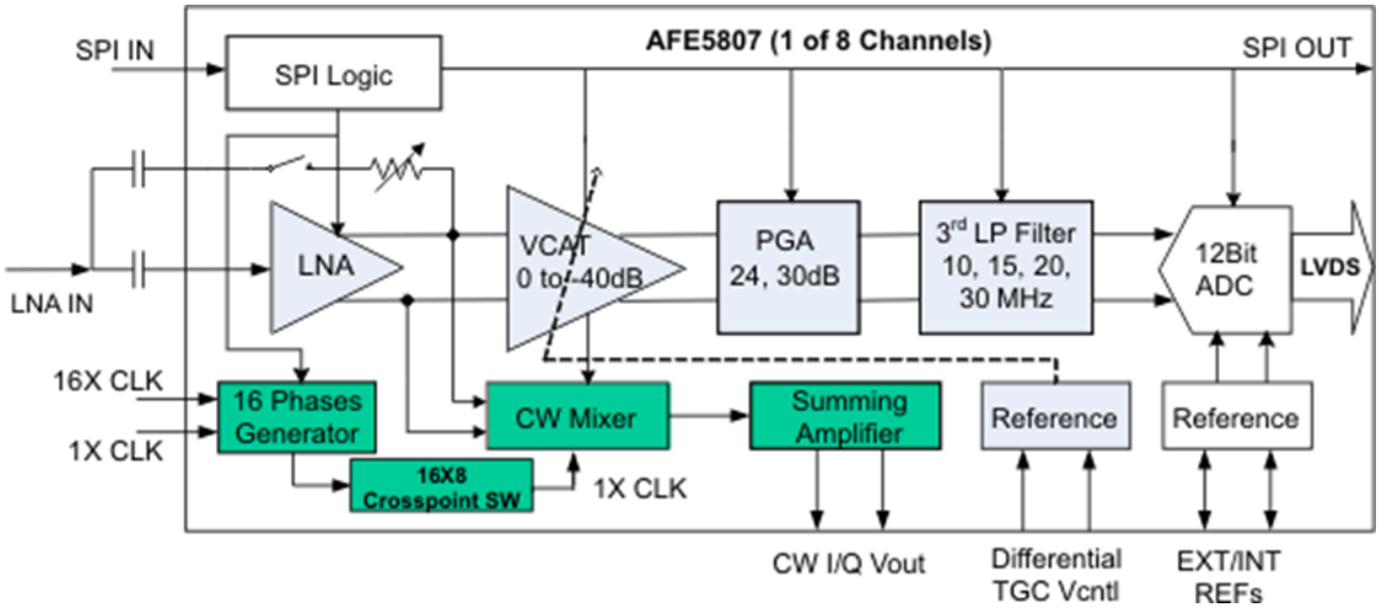
Design

The CMB schematic



Design

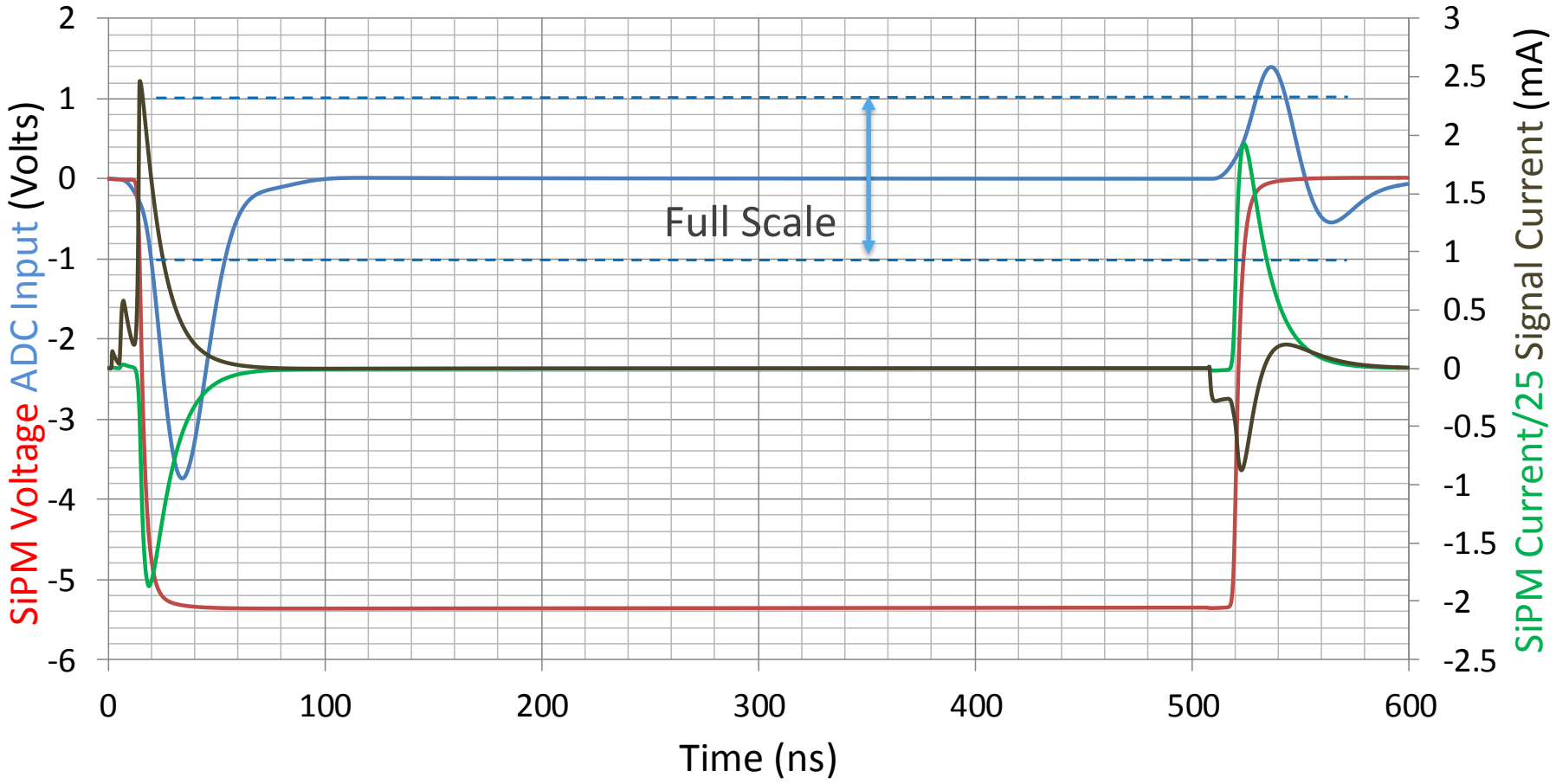
The core of the readout is a commercial ultrasound imaging chip:



Eight channels of: low noise preamp, variable gain amp, programmable gain amp, programmable low pass filter, 80msps 12 bit ADC. $8 per channel, 120mW per channel. Adjust gain such that 1p.e. = 10 ADC counts.

Design

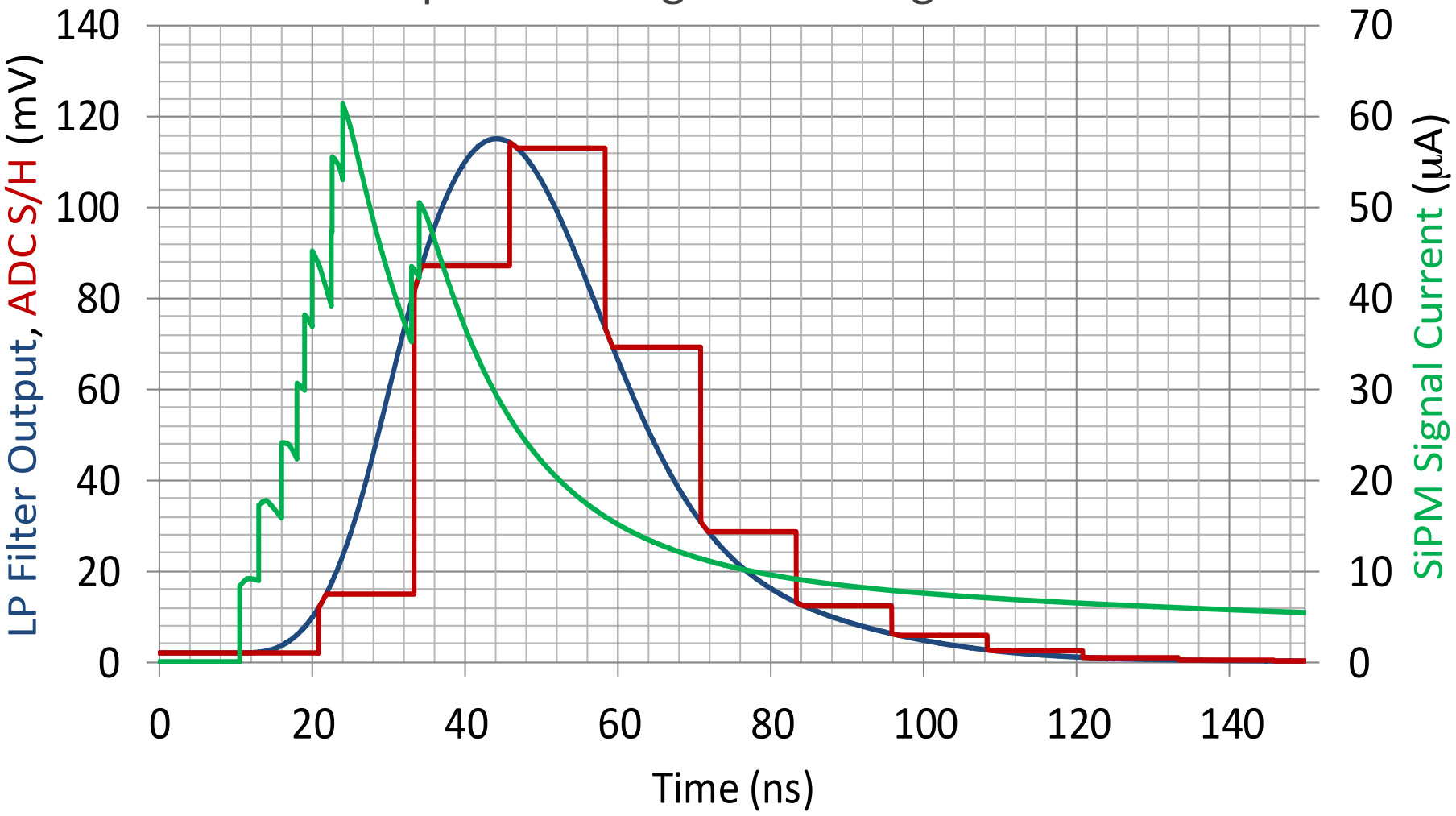
Flash gate simulation



LNA Voltage Clamp not simulated, ultrasound imaging requires fast over range recovery

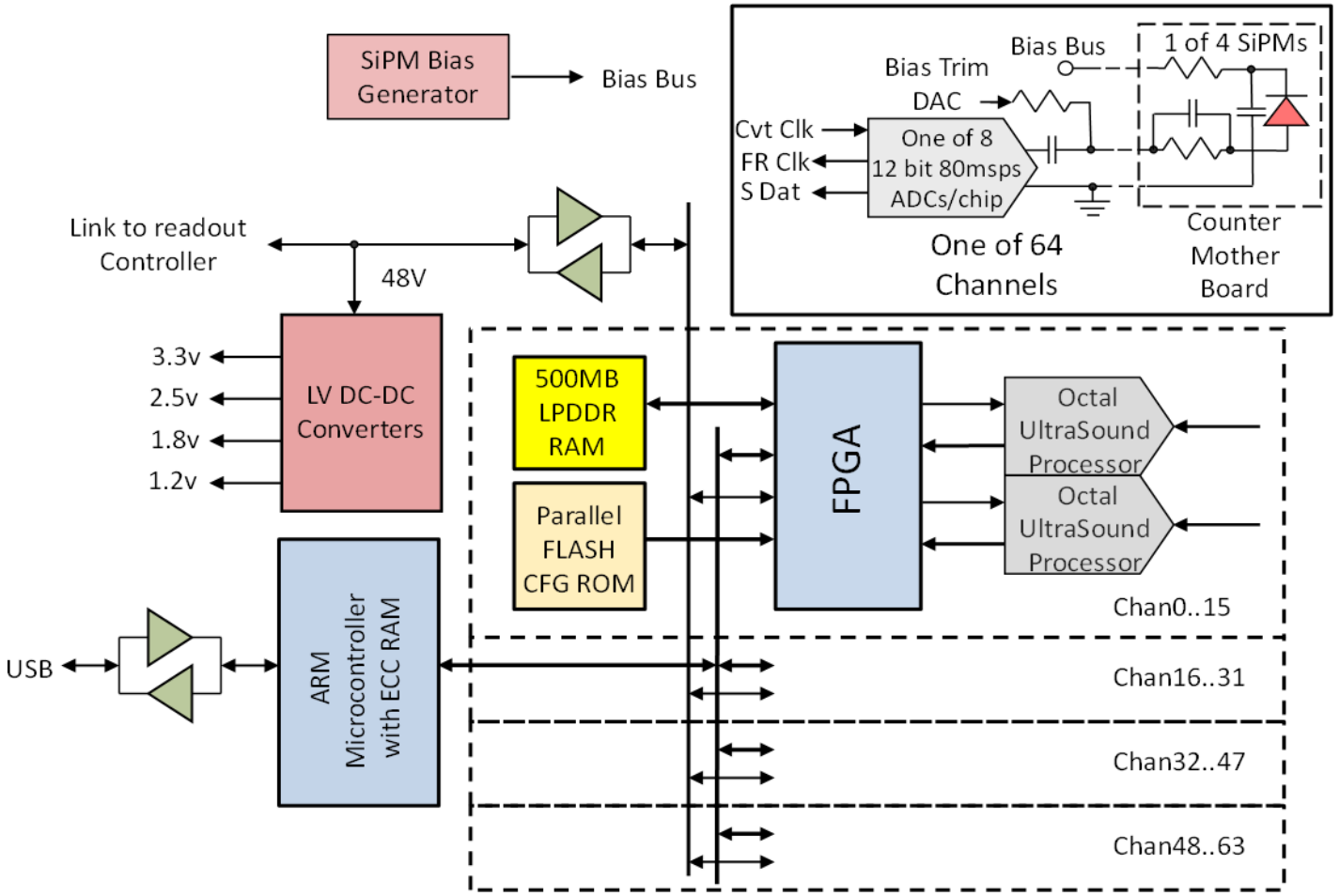
Design

Simulation of an 11 p.e. SiPM signal showing tail cancellation:



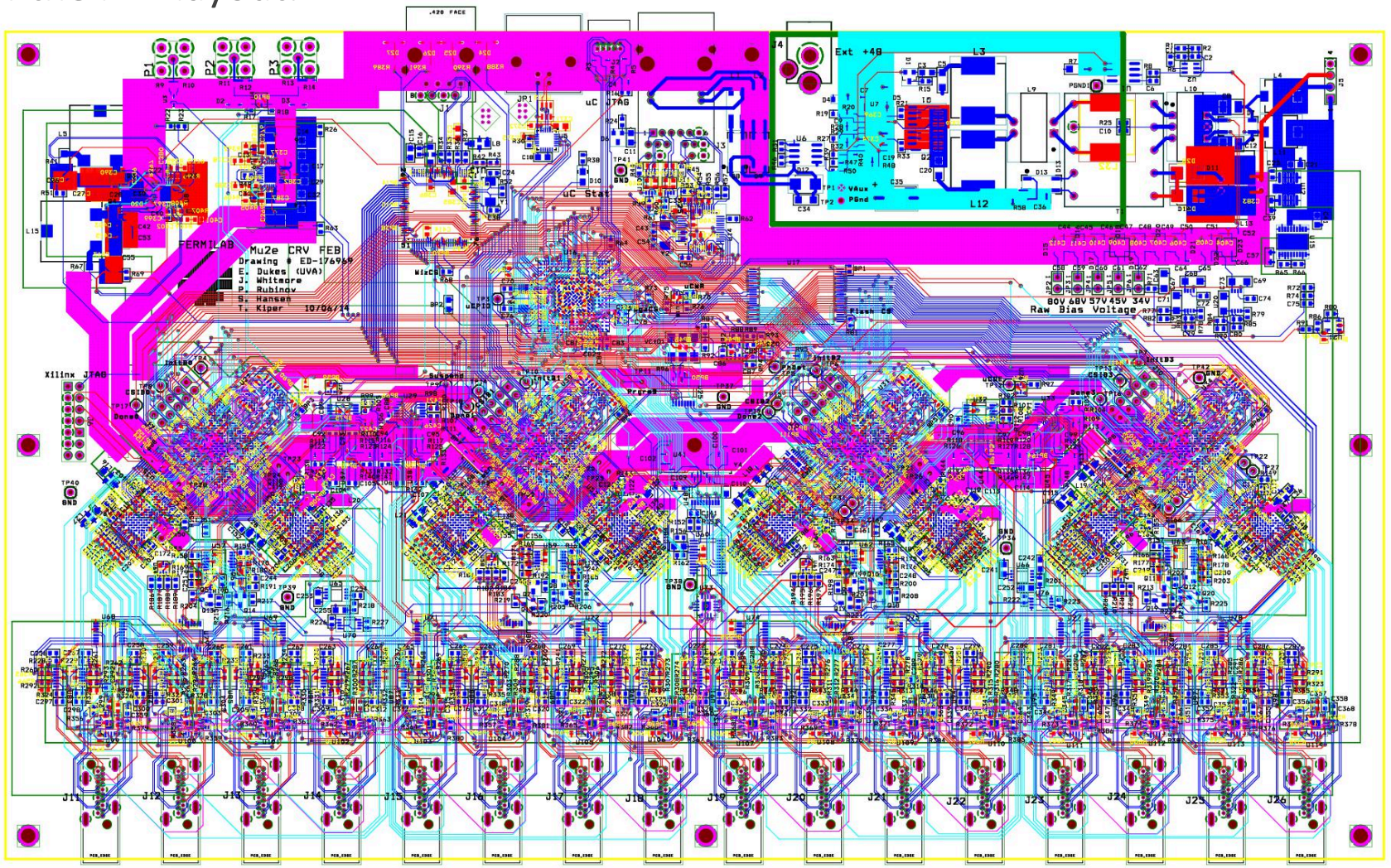
Design

Front end board block diagram:



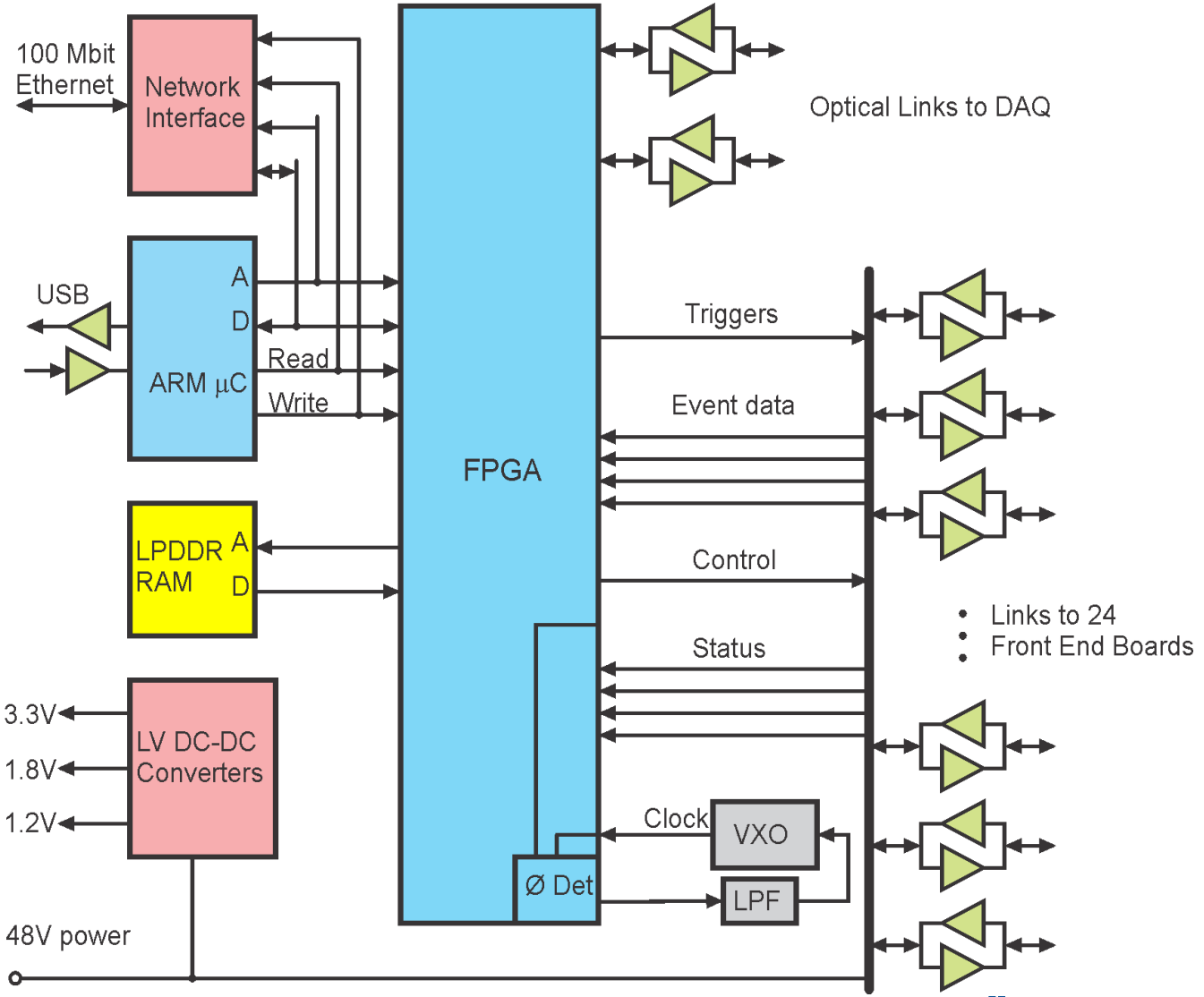
Design

Plot of the FEB layout:



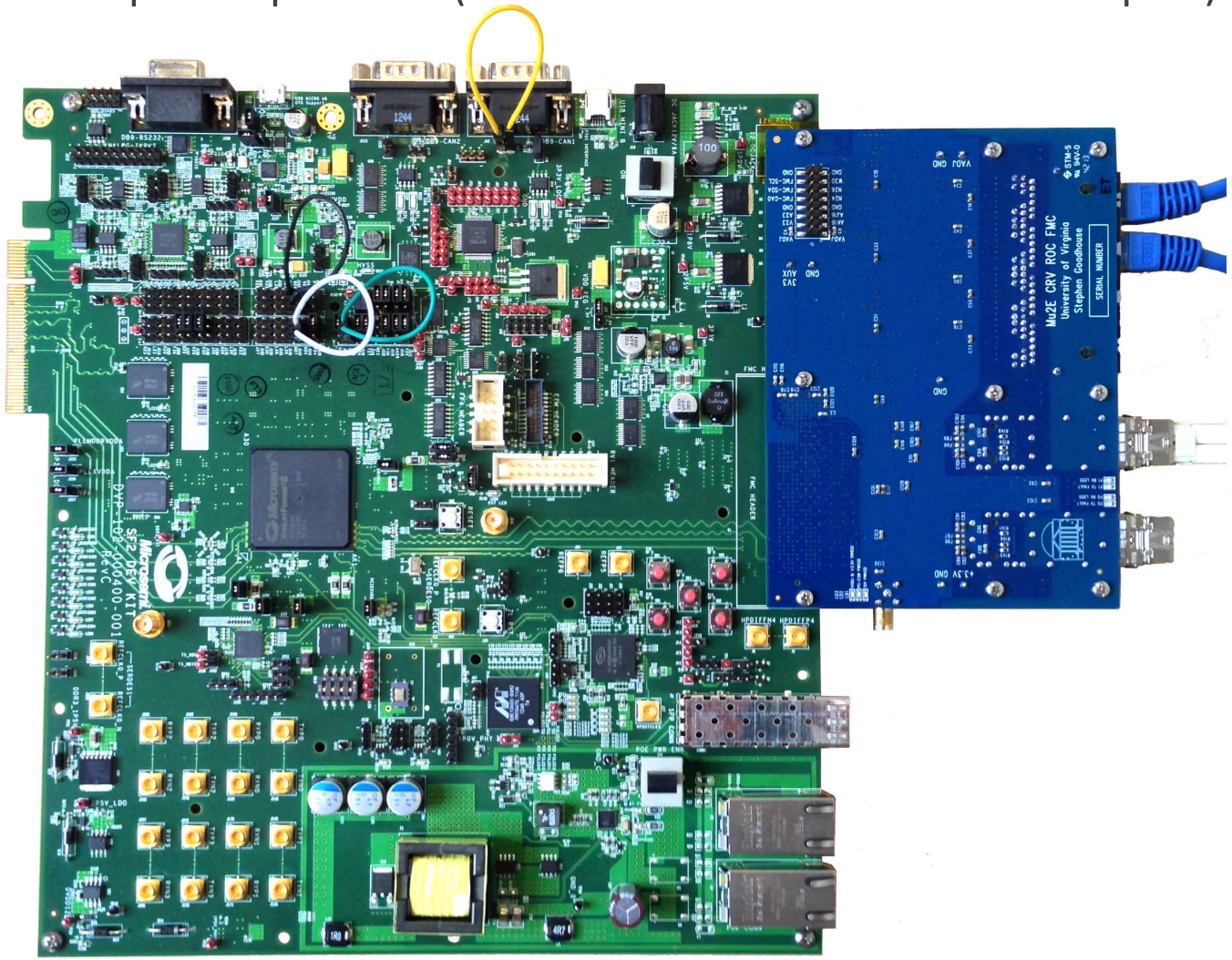
Design

Controller block diagram:



Design

Controller development platform (FPGA evaluation board + FEB adapter):



Design

Rate Estimates:

	Item	Average	Design
Live Spill Period	Instantaneous hit rate/counter (channel)	127.0 kHz	1000.0 kHz
	Hit event size	12 bytes	
	Instantaneous data rate/channel	1.5 MB/s	12.0 MB/s
	Spill length (s)	0.497	
	Spill duty factor	0.528	
	Average data rate/FEB	51.5 MB/s	405.7 MB/s
	Total data per FEB per live spill	25.6 MB	201.6 MB
Interspill Period	Instantaneous hit rate/counter (channel)	10.0 kHz	100.0 kHz
	Instantaneous data rate/channel	0.1 MB/s	1.2 MB/s
	Interspill length (s)	0.836	
	Interspill duty factor	1.000	
	Average data rate/FEB	7.7 MB/s	76.8 MB/s
	Total data per FEB per interspill	6.4 MB	64.2 MB
Total	Average data rate/FEB	24.0 MB/s	199.4 MB/s
	Average data rate/CRV	7.1 GB/s	59.0 GB/s
	Total data per FEB per cycle	32.0 MB	265.9 MB
	Total data CRV per cycle	9.5 GB	78.7 GB
FEB to DAQ	Trigger rejection	100	
	Data rate out per FEB	0.2 MB/s	2.0 MB/s
	Average data rate to a ROC	5.8 MB/s	47.9 MB/s
	Total CRV data rate to DAQ	71.1 MB/s	590.2 MB/s
	Total CRV data for run	1.0 PB	8.0 PB

10 MB/s Links
FEB to Controller

200 MB/s Links
Controller to DAQ

Integration and Interfaces

- Internal
  - Schematics, documents posted on UVA server
  - Weekly CRV meetings
- External
  - Drawings, documents specifying system interfaces posted on Docdb
  - DAQ meetings
  - Electrical integration meetings

Changes Since CD-1

- Background rates have gone up >10x
- Signal tail cancellation implemented to improve double pulse resolution
- Flash gate implemented
- Channel count has increased 33%
- 1E10 Neutrons/cm2 total dose. Damage is not an issue, SEUs are.
- Single event upset mitigation required
- 100mT ambient field
- Magnetic field tolerance required
- Controllers are to be placed in the electronics room to avoid magnetic field and radiation dose

Value Engineering since CD-1

- Change from self triggering to externally triggered. All data analysis beyond zero-suppression and trigger primitive is done offline. Reduces FPGA programming labor, reduces data rate

Performance

- We will use the ADC data to track SiPM gain variations based on single p.e. signals during the interspill in order to apply a known energy threshold during the spill.
- An 80 msps ADC can resolve adjacent pulses down to ~40ns. There is no efficiency loss if two pulses are counted as one, but the time accuracy suffers. Time resolution degrades as pulse separation goes below 60ns.

Performance

- We will use the ADC data to track SiPM gain variations based on single p.e. signals during the interspill in order to apply a known energy threshold during the spill.
- For a typical muon track we expect timing accuracy of 5ns.
- An 80 msps ADC can resolve adjacent pulses down to ~40ns. There is no efficiency loss if two pulses are counted as one, but the time accuracy suffers. Time resolution degrades as pulse separation goes below 60ns.

Quality Assurance

- Extensive testing regime
- Prototype FEB
  - Test for single event upsets
  - Test magnetic field tolerance
  - Rate testing in a beam
  - Stability testing with cosmic rays.
  - Test link to DAQ
- Pre-production prototype FEB
  - Incorporate changes based on results from above
  - Build test fixture, write test software

Risks

There are no major risks.

Risk of increased channel count has been actualized.

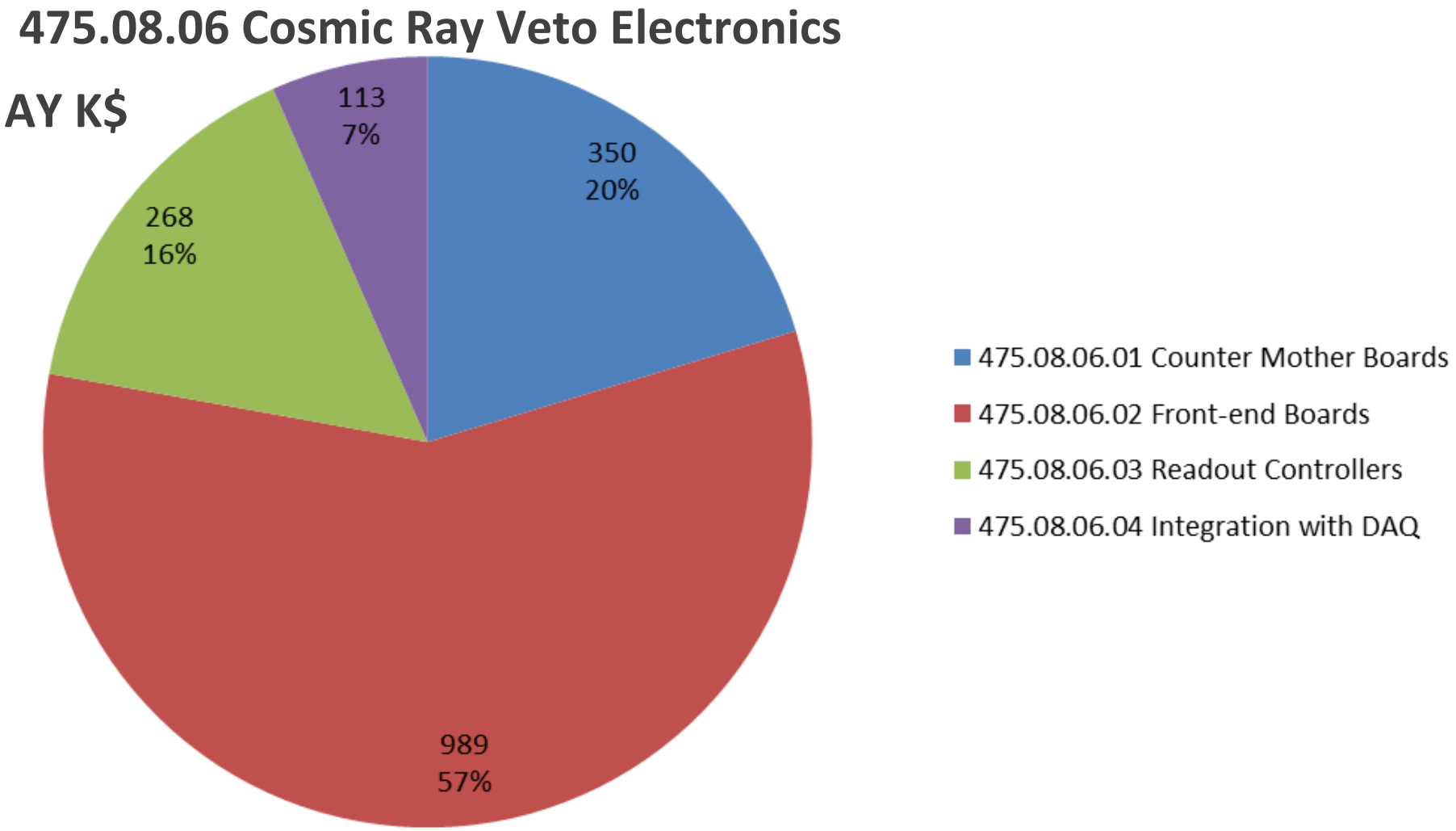
ES&H

- There are no special concerns with the CRV electronics
- There will be moderate voltages (<100V) present for biasing the photo detectors. Stored energy values are in the milli-Joule range. Moderate power levels (700W) in the controllers.

Cost Table

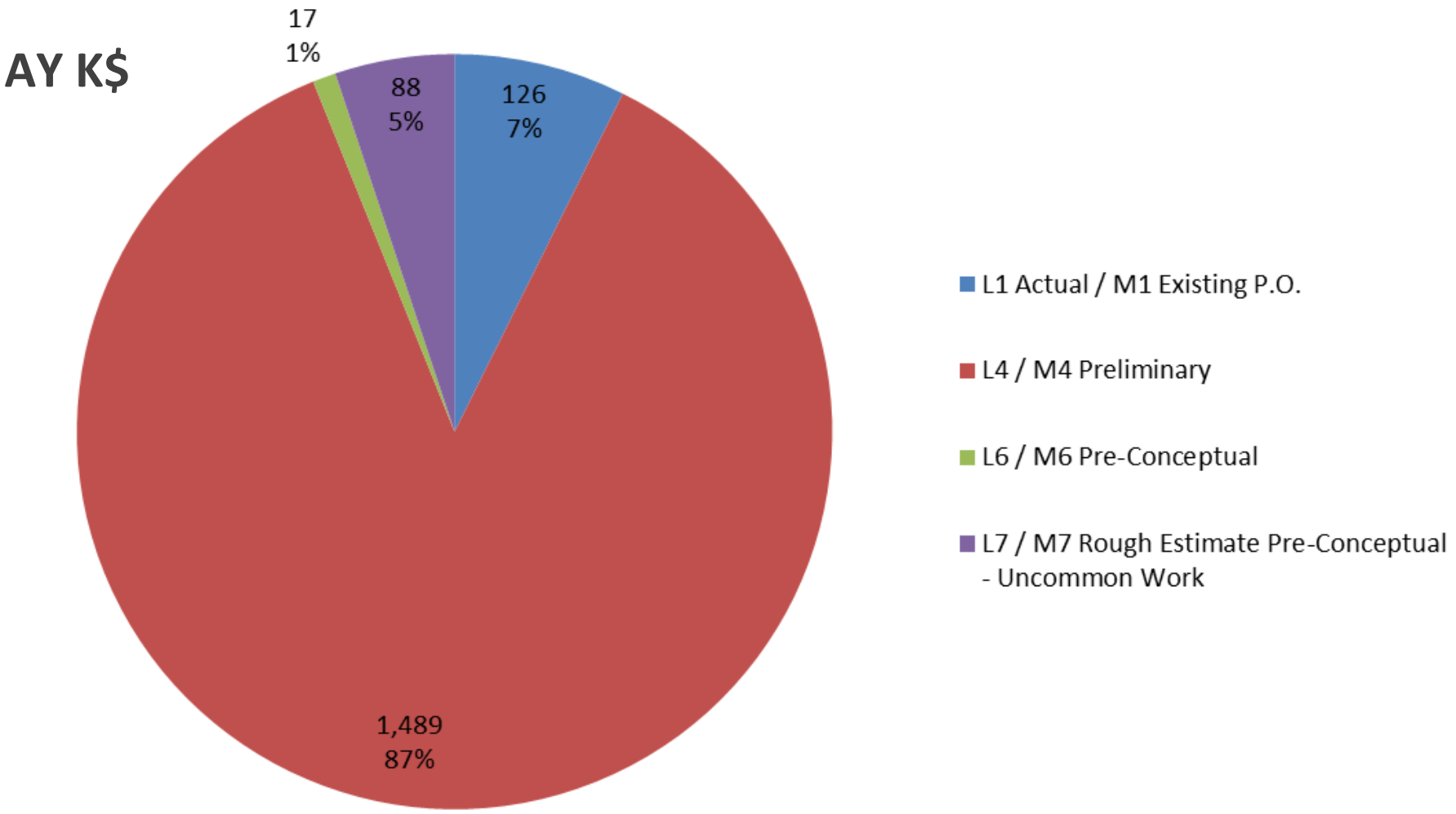
	Base Cost (AY K$)					
	M&S	Labor	Total	Uncertainty (on remaining budget)	% Contingency (on remaining budget)	Total Cost
475.8.1 Project Management	267	178	445	75	21%	520
475.8.2 Mechanical Design	135	3	138	24	38%	162
475.8.3 Scintillator extrusions	567	462	1,029	209	25%	1,238
475.8.4 Fibers	462		462	106	24%	568
475.8.5 Photodetectors (SiPMs)	464	305	769	190	41%	959
475.8.6 Electronics	1,314	407	1,720	511	33%	2,231
475.8.7 Module Fabrication	1,482	8	1,490	466	35%	1,956
475.8.8 Detector assembly and installation	127	81	208	64	35%	273
475.8.9 Conceptual Design/R&D	258	252	511		0%	511
475.8.99 Risk Based Contingency				318	-	318
Grand Total	5,077	1,696	6,773	1,963	38%	8,735

Cost Breakdown

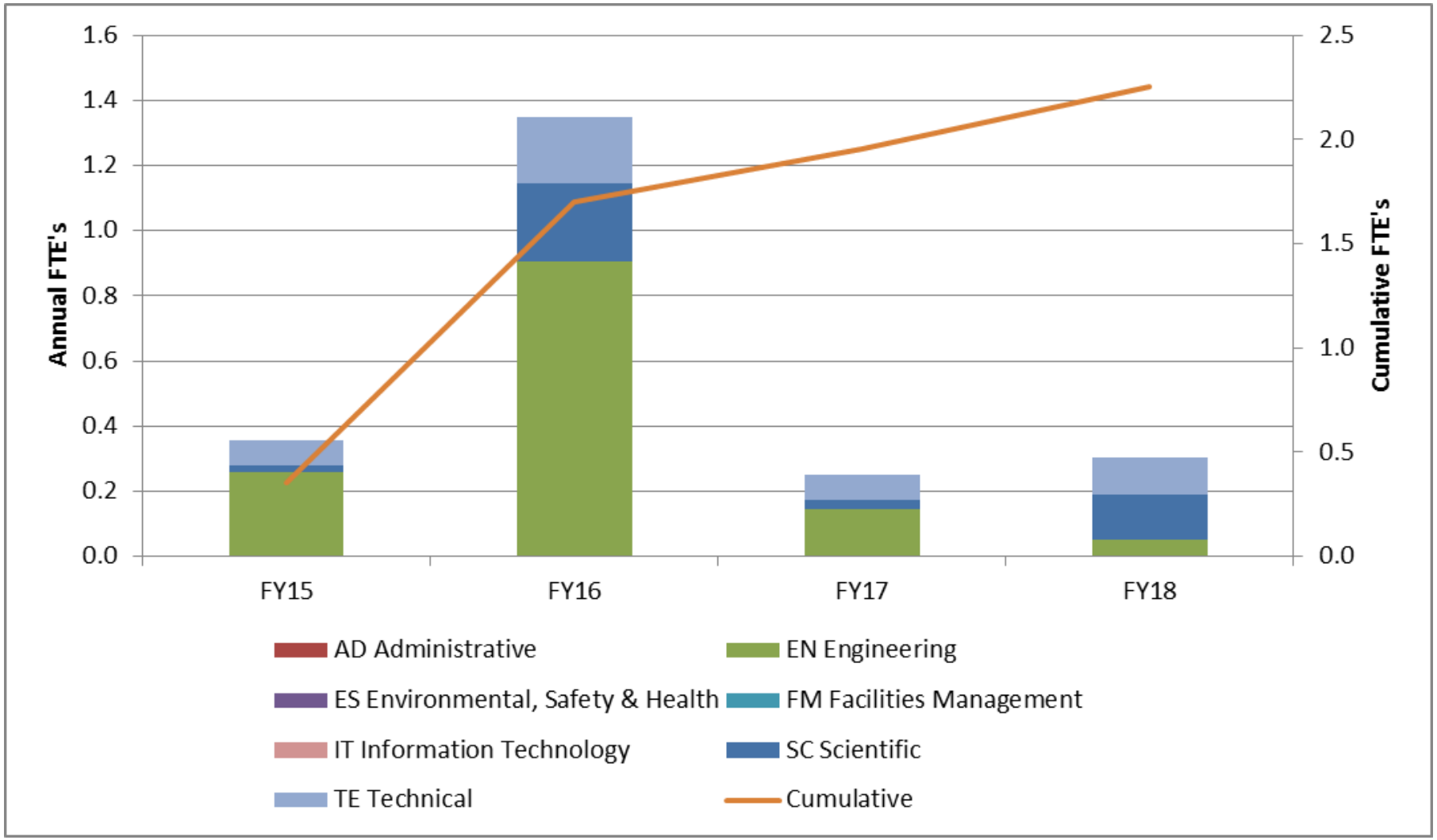


Quality of Estimate

475.08.06 Cosmic Ray Veto Electronics



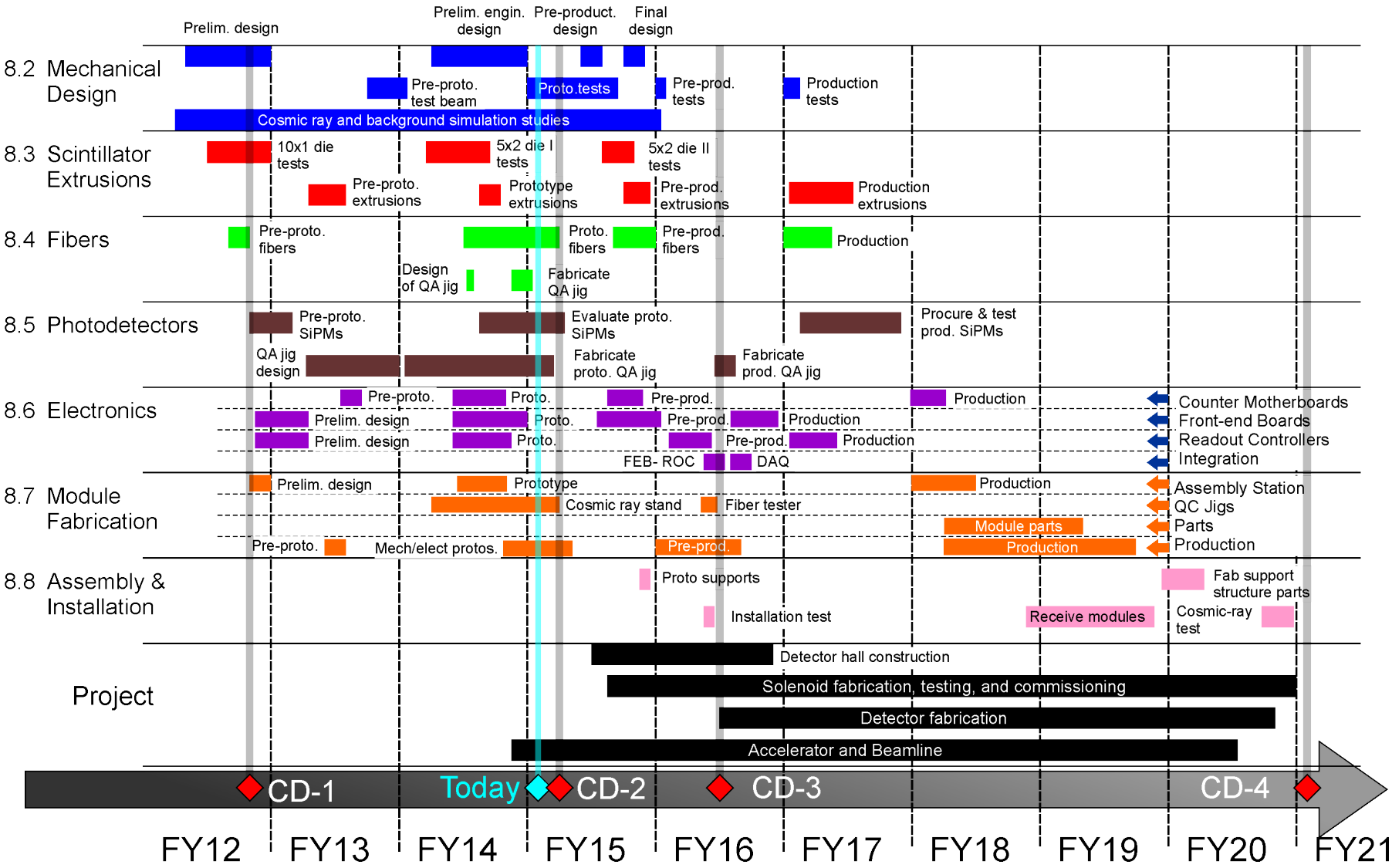
Labor Resources by Discipline



Milestones

47508.6.1.1025	T5 - Prototype counter motherboards tested
47508.6.3.001025	T5 - Prototype readout controllers tested
47508.6.2.001035	T5 - Prototype front-end board tested
47508.6.1.1045	T5 - Pre-production counter motherboards tested
47508.6.2.001065	T5 - Pre-production front-end board tested
47508.6.3.001055	T5 - Pre-production readout controllers tested
47508.6.2.001150	T5 - Front end boards completed
47508.6.4.001045	T5 - Pre-production electronics integrated with DAQ
47508.6.3.001080	T4 - Readout Controllers Completed
47508.6.1.1060	T5 - Production counter motherboards tested

Schedule


Prelim. design
Prelim. engin. design
Pre-product. design
Final design
8.2 Mechanical Design
Pre-proto. test beam
Proto.tests
Pre-prod. tests
Production tests
Cosmic ray and background simulation studies
8.3 Scintillator Extrusions
10x1 die tests
5x2 die I tests
5x2 die II tests
Pre-proto. extrusions
Prototype extrusions
Pre-prod. extrusions
Production extrusions
8.4 Fibers
Pre-proto. fibers
Proto. fibers
Pre-prod. fibers
Production
Design of QA jig
Fabricate QA jig
8.5 Photodetectors
Pre-proto. SiPMs
Evaluate proto. SiPMs
Procure & test prod. SiPMs
QA jig design
Fabricate proto. QA jig
Fabricate prod. QA jig
8.6 Electronics
Pre-proto.
Proto.
Pre-prod.
Production
Prelim. design
Counter Motherboards
Front-end Boards
Readout Controllers
Integration
FEB- ROC
DAQ
8.7 Module Fabrication
Prototype
Cosmic ray stand
Fiber tester
Module parts
Assembly Station
QC Jigs
Parts
Mech/elect protos.
8.8 Assembly & Installation
Proto supports
Fab support structure parts
Installation test
Receive modules
Cosmic-ray test
Project
Detector hall construction
Solenoid fabrication, testing, and commissioning
Detector fabrication
Accelerator and Beamline
CD-1
Today
CD-2
CD-3
CD-4
FY12
FY13
FY14
FY15
FY16
FY17
FY18
FY19
FY20
FY21

Summary

- The electronics is commercial off the shelf
- The design is derived from previous successful projects
- We have begun design and fabrication of the first prototypes.
- We will test performance in a magnetic field and under radiation exposure