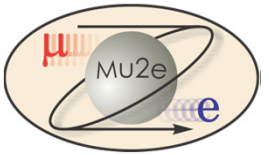
Fermilab

Mu2e Tracker Electronics



Vadim Rusu
Front End Electronics L3 Manager
10/22/2014

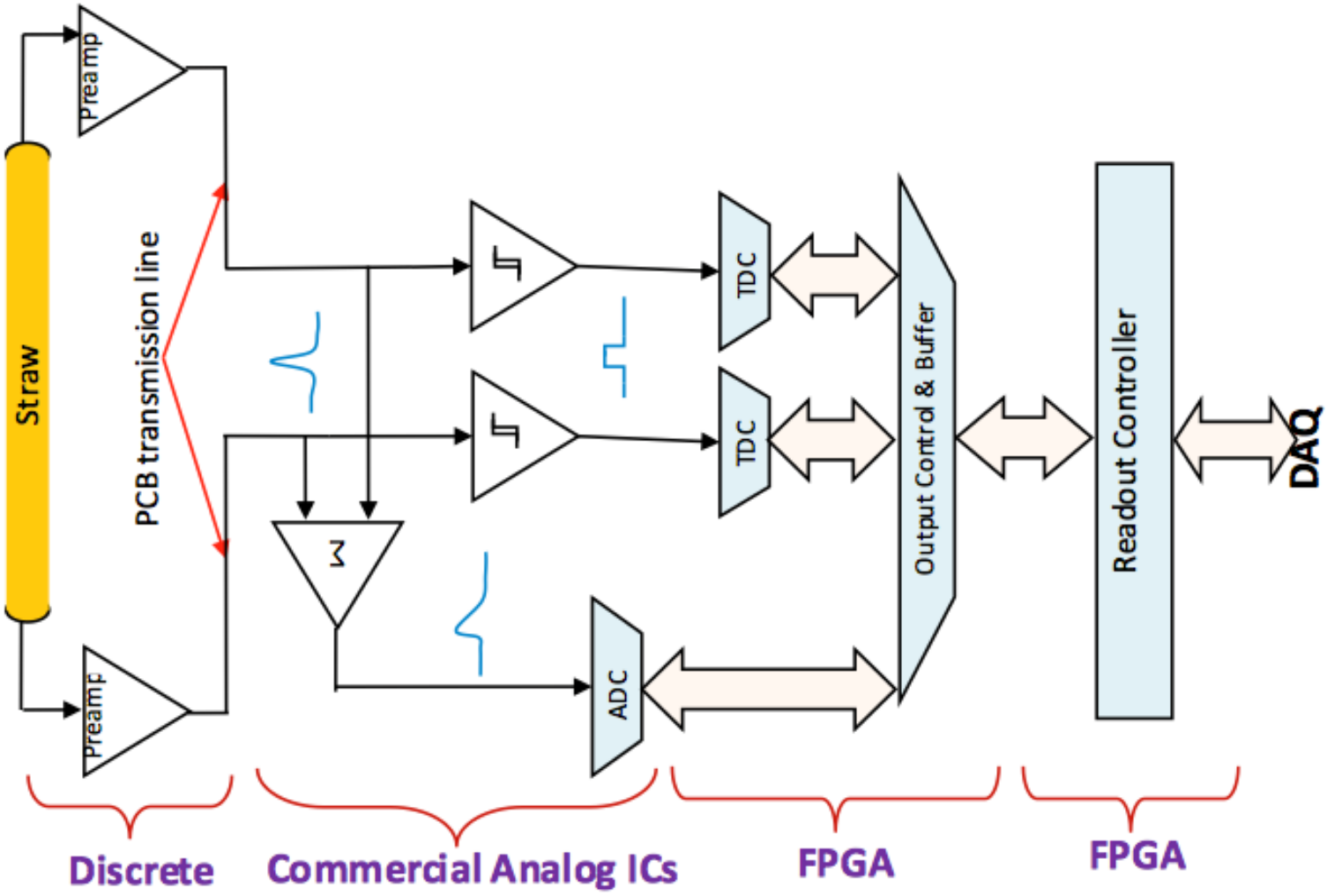
Outline

- Requirements
- Design and Implementation
- Prototypes
- Cost

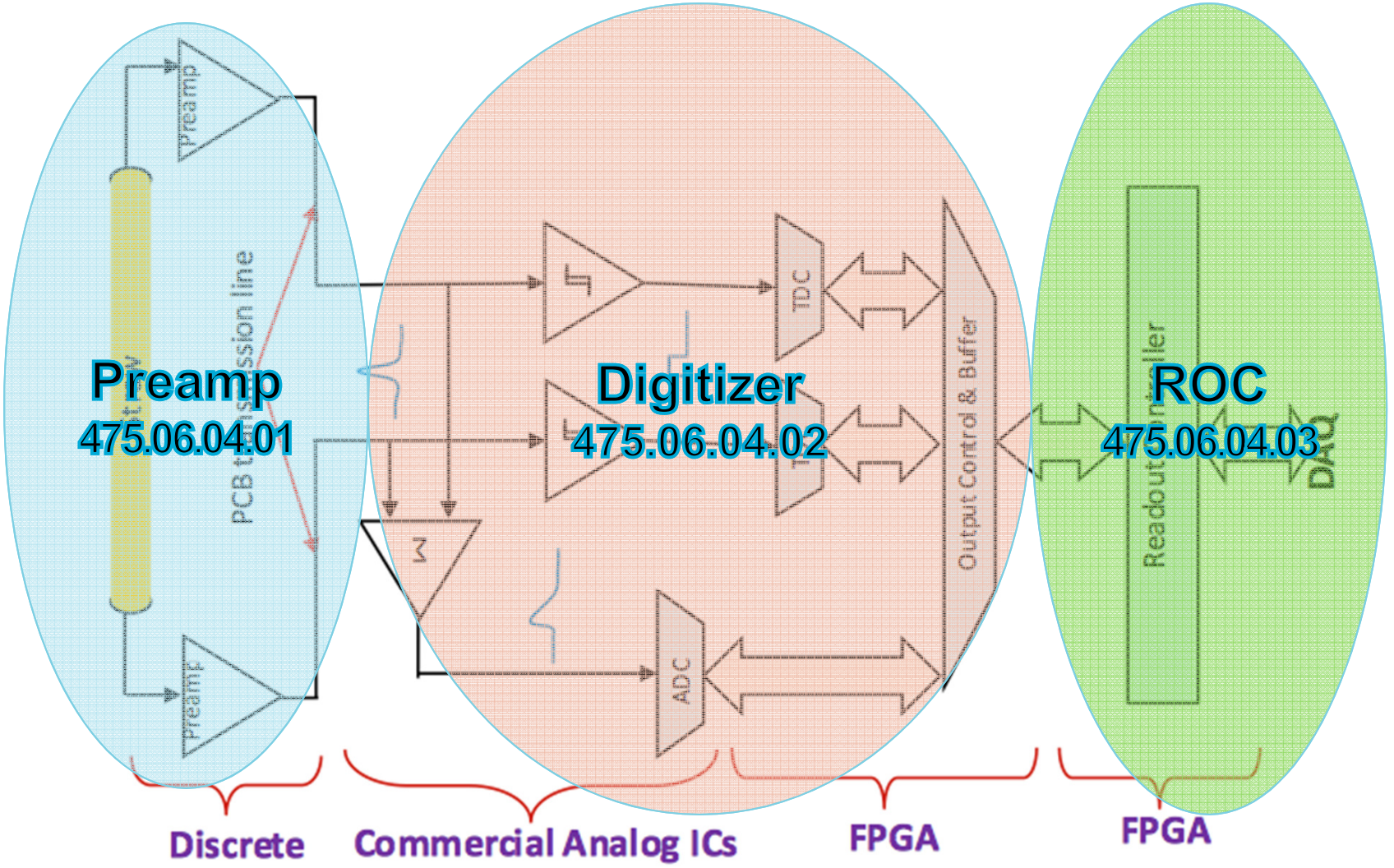
Electronics requirements

- Amplification and digitization of the straw signals
- Transmit the digitized data to DAQ
- Record both ends of the straw (time division – 3cm resolution)
- Measure pulse height for dE/dx
- Supply HV to anode wires (and HV disconnect)
- Run triggerless mode (soft trigger may be implemented at the DAQ level)
- B field perturbation <1G in the active region
- Rad hard (2×10^{12} n/cm^2)
- 10kW power
- <12 × 96 dead channels in 5 years at 90% CL

Tracker Front End Scheme



Tracker Front End Scheme



Implementation

- Entire electronics chain implemented in commercially available components
  - Reduced risk
  - Reliable cost estimates (manufacturer quotes and catalog)
  - Upgradeable (ride technology wave)
  - Flexibility
    - All key functionalities implemented in FPGAs
    - Reconfigurable

Preamp requirements

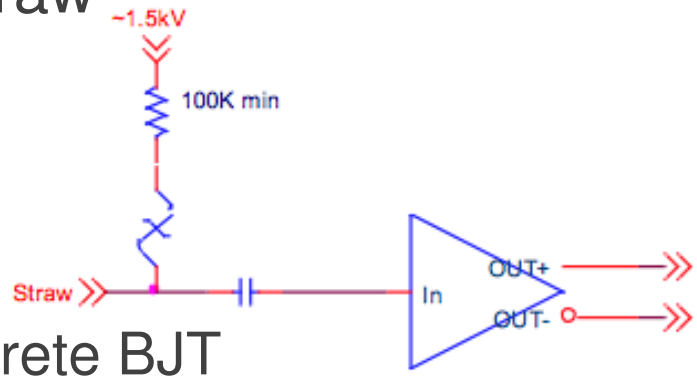
- Bandwidth 100-300MHz
- Typical electron pulse >5x noise floor
- Dynamic range x10 typical electron pulse
  - Clip larger pulses to avoid x-talk downstream from large proton pulses
- Shaping – return to baseline <200ns
  - >50% efficiency for typical electron pulse after a typical proton pulse
- >100kOhm R from the HV bus
  - <1nA leakage through blocking capacitor
  - HV remote disconnect

Doc-db 3879

Preamp implementation

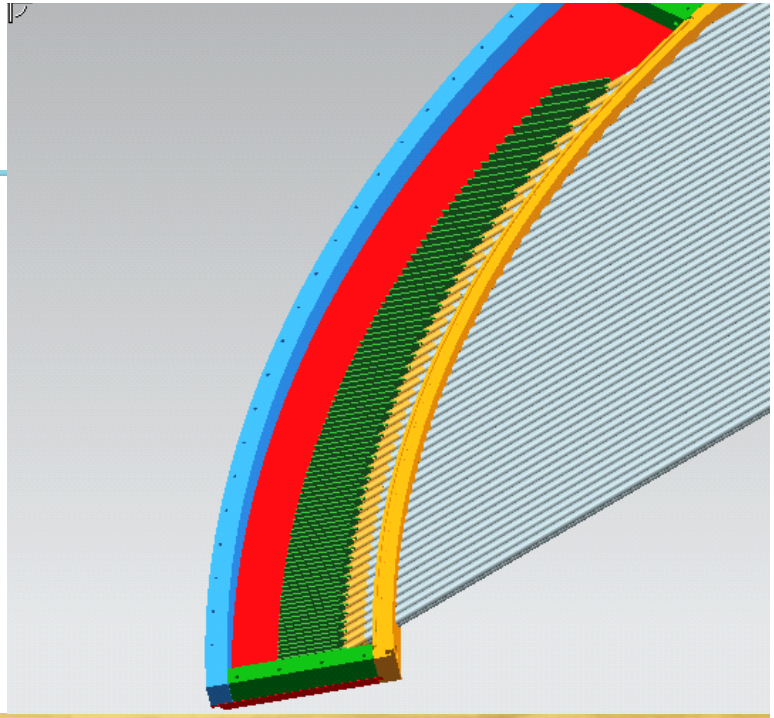
A. Mukherjee/V. Rusu
FNAL

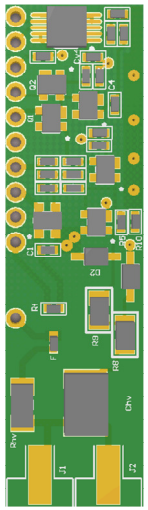
- 41472 preamps (2x straws)
- Small/simple PCBs at the end of the straw
- Low power (~15mW)
- Configurable gain and threshold
- Input stage
  - Low noise/high f_T SiGe technology discrete BJT
  - Active 300Ohm termination to avoid reflections
  - ESD Transient protection
- Output stage
  - Differential output (good CMRR avoids ground loops)
  - Termination and pull-up at digitizer input
- Advanced stage of prototyping



Preamp performance

- 250MHz -3dB point
- 2mV RMS output noise
- 10mV typical electron pulse response
- Dynamic range 150mV
- ~50ns shaping time



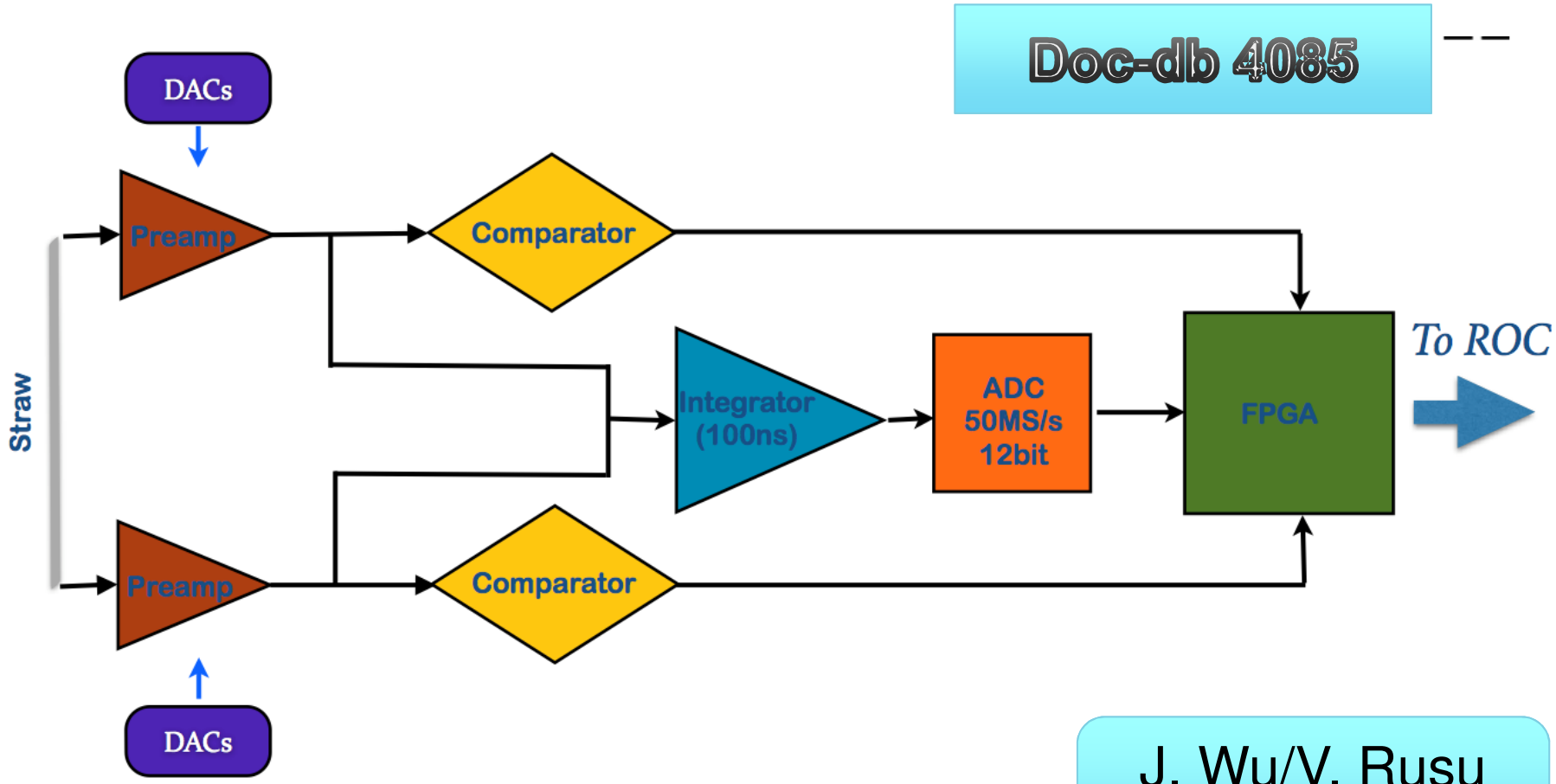


Digitizer requirements

- <70ps ΔT resolution (time division)
- 1ns drift time resolution
  - 1700ns range (at least a microbunch)
- 7 bits ADC resolution
  - X10 typical electron pulse range
- 50MS/s sampling rate
- LVDS data to ROC (200Mb/s line)
  - Data to ROC
    - Header, 2x TDC, 8 ADC samples
- 150mW/straw

Doc-db 3879

Digitizer scheme

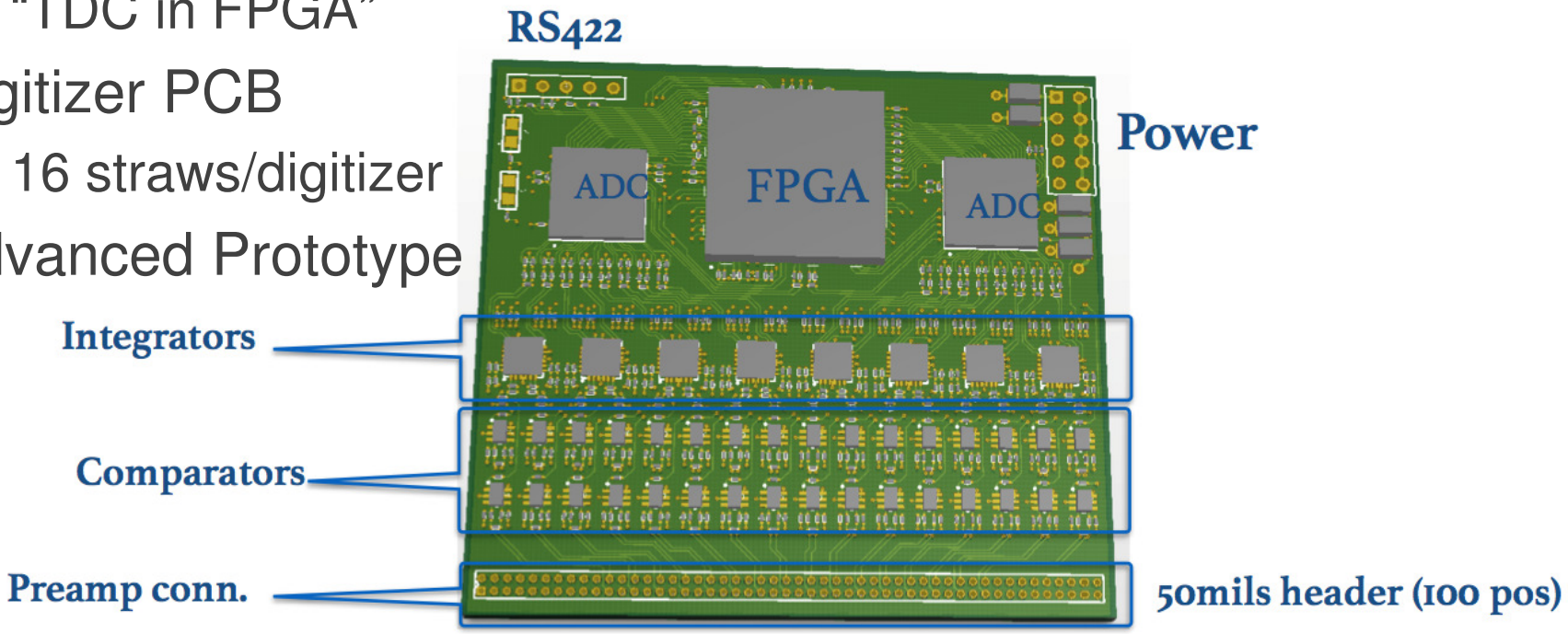


J. Wu/V. Rusu
FNAL

Digitizer implementation

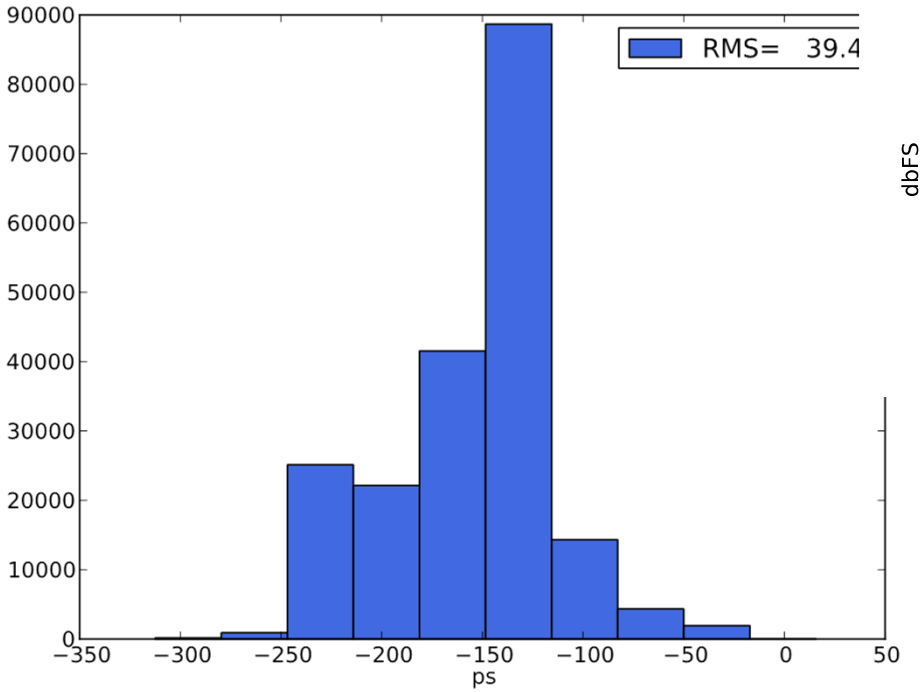
- 41472 TDC channels and 20736 ADC channels
- Commercial off-the-shelf components
  - Fast comparator and shaper
  - ADC (Maxim19527)
  - "TDC in FPGA"
- Digitizer PCB
  - 16 straws/digitizer
- Advanced Prototype

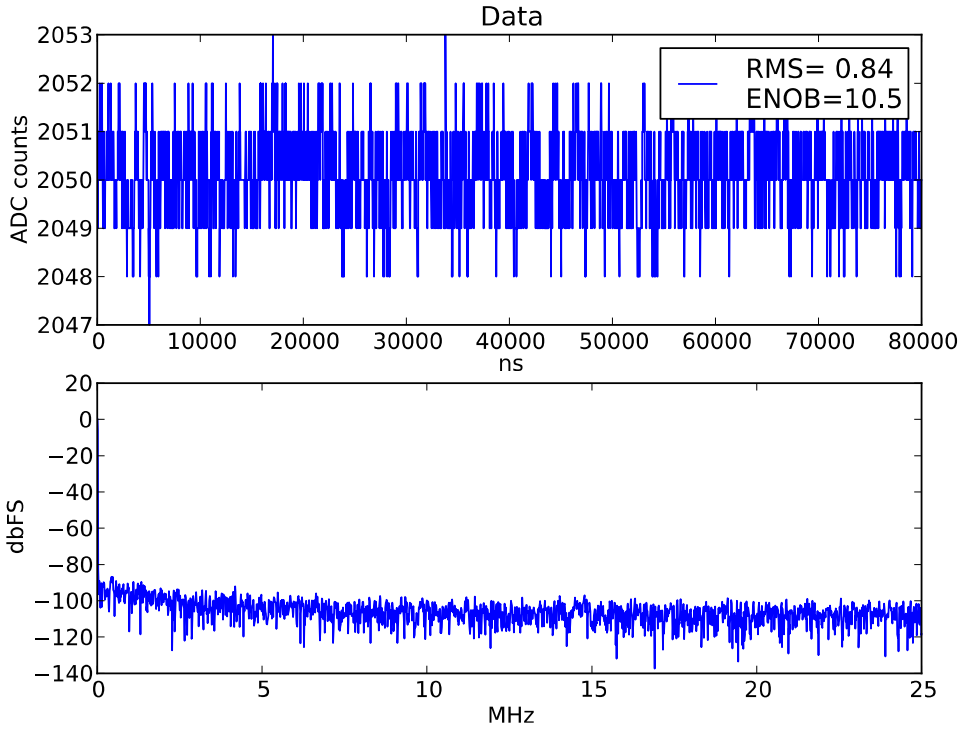
Doc-db 4085



Digitizer performance

Test bench measurements





Doc-db 4085

Readout Controller Requirements

- Received data from Digitizers
- Buffering
  - Continue data transfer in inter-spill time
- Transmits to DAQ
  - 230Mbps each ROC to DAQ
- Relies slow controls to front-end
  - Preamp settings
  - HV control (fuses)
  - Monitor environmental variables

Doc-db 3973

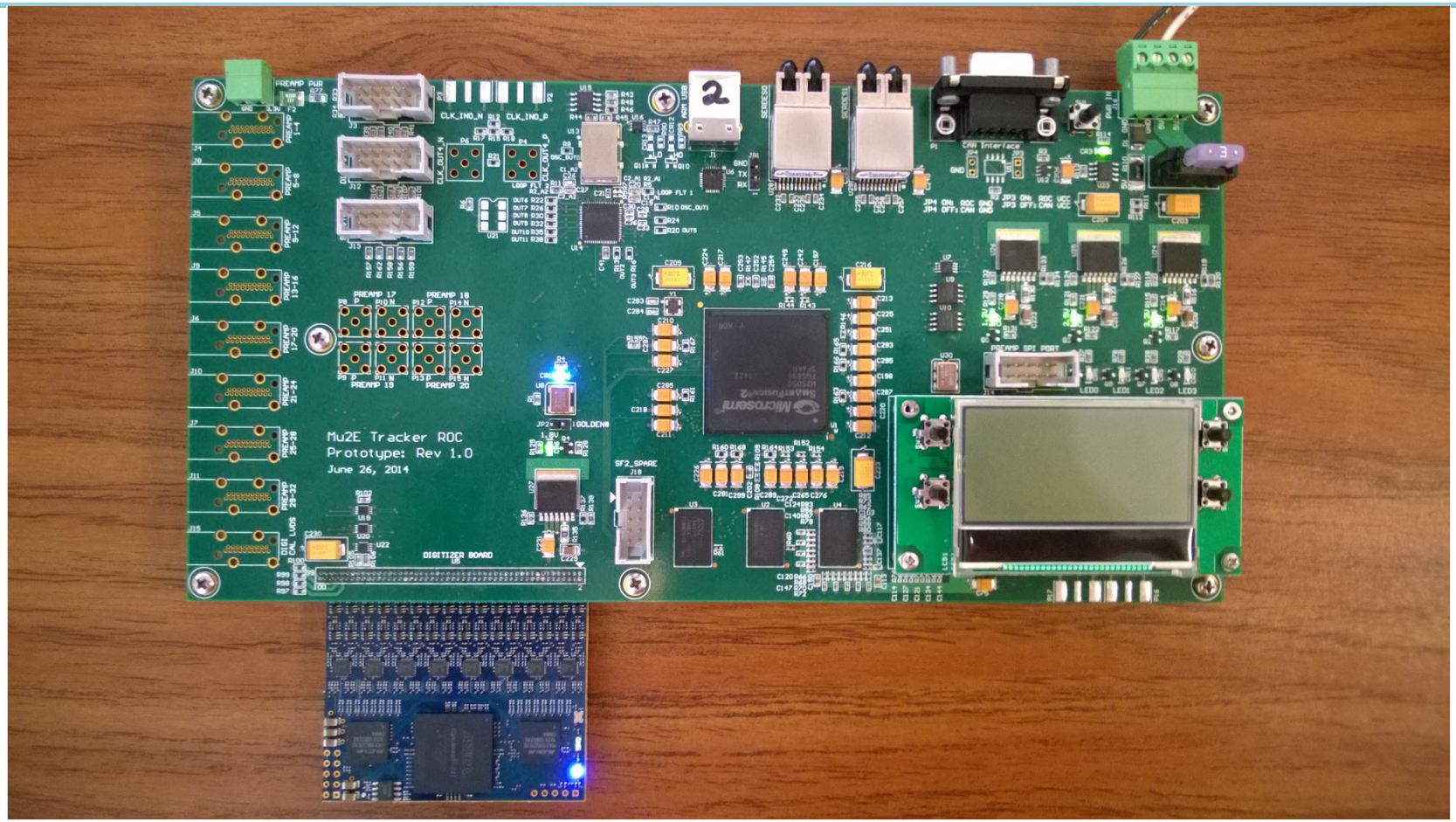
ROC Implementation

- SmartFusion FPGA (rad hard line from Microsemi)
- DDR3 on board for buffering
- 2.5 Gbps full-duplex fiber optics
  - Ring architecture
- Advanced prototype

Doc-db 3973

U of Houston – E. Hungerford
FNAL - G. Deuerling

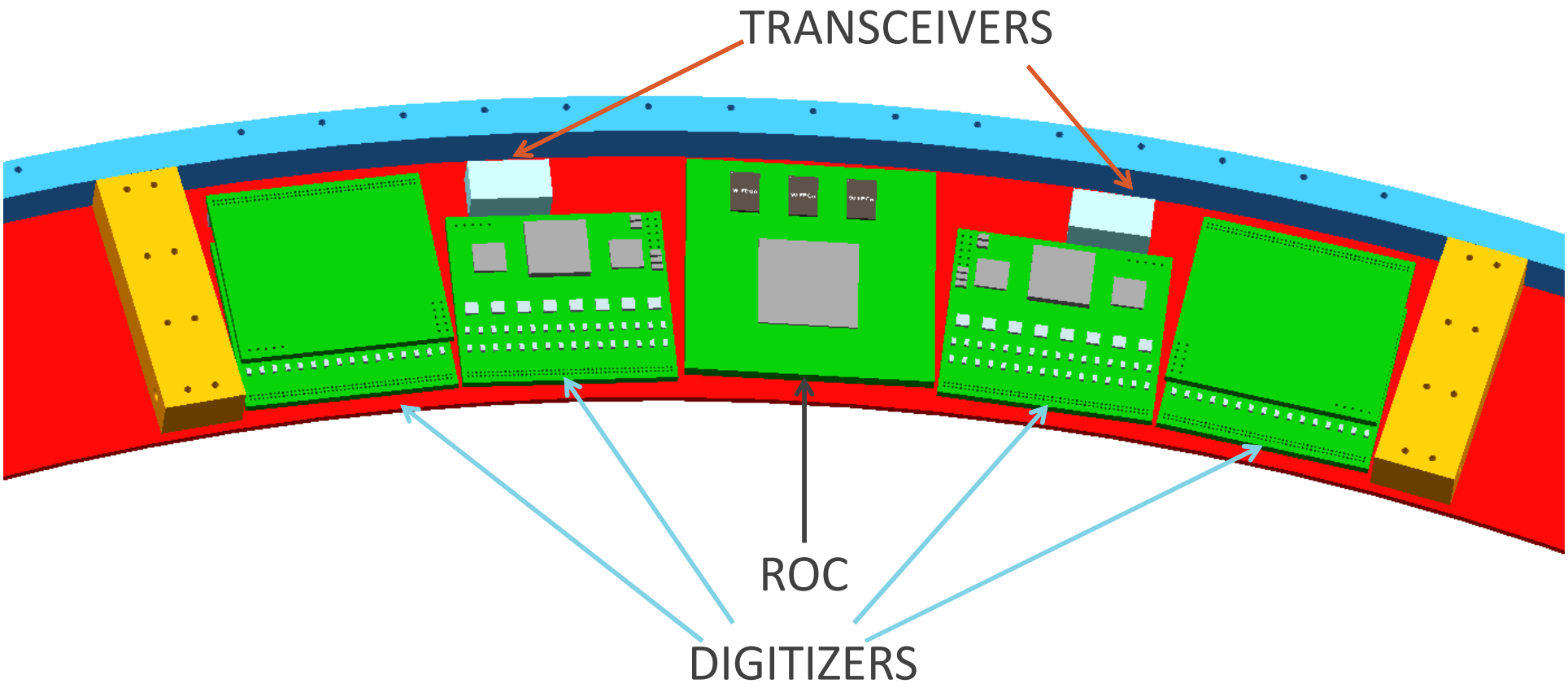
ROC/Digi Prototype



- Successfully established comm between ROC and digi
- LVDS data received on the ROC FPGA
  - USB readout – almost ready to try optical fiber

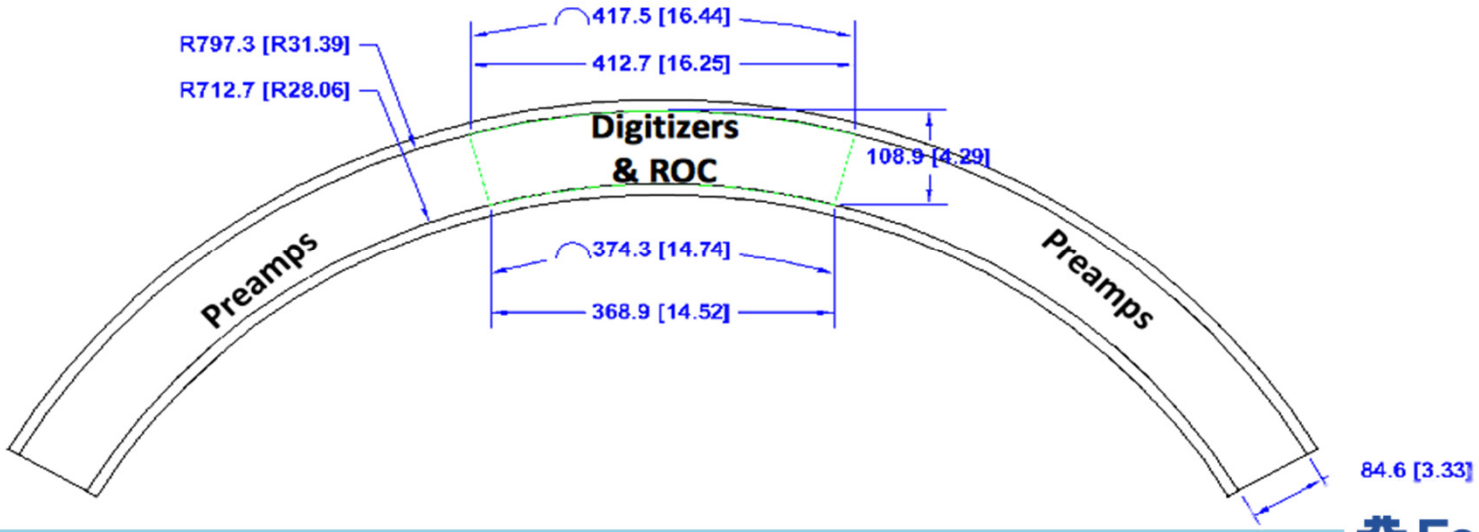
Assembly

- Tight fit, but it does fit.



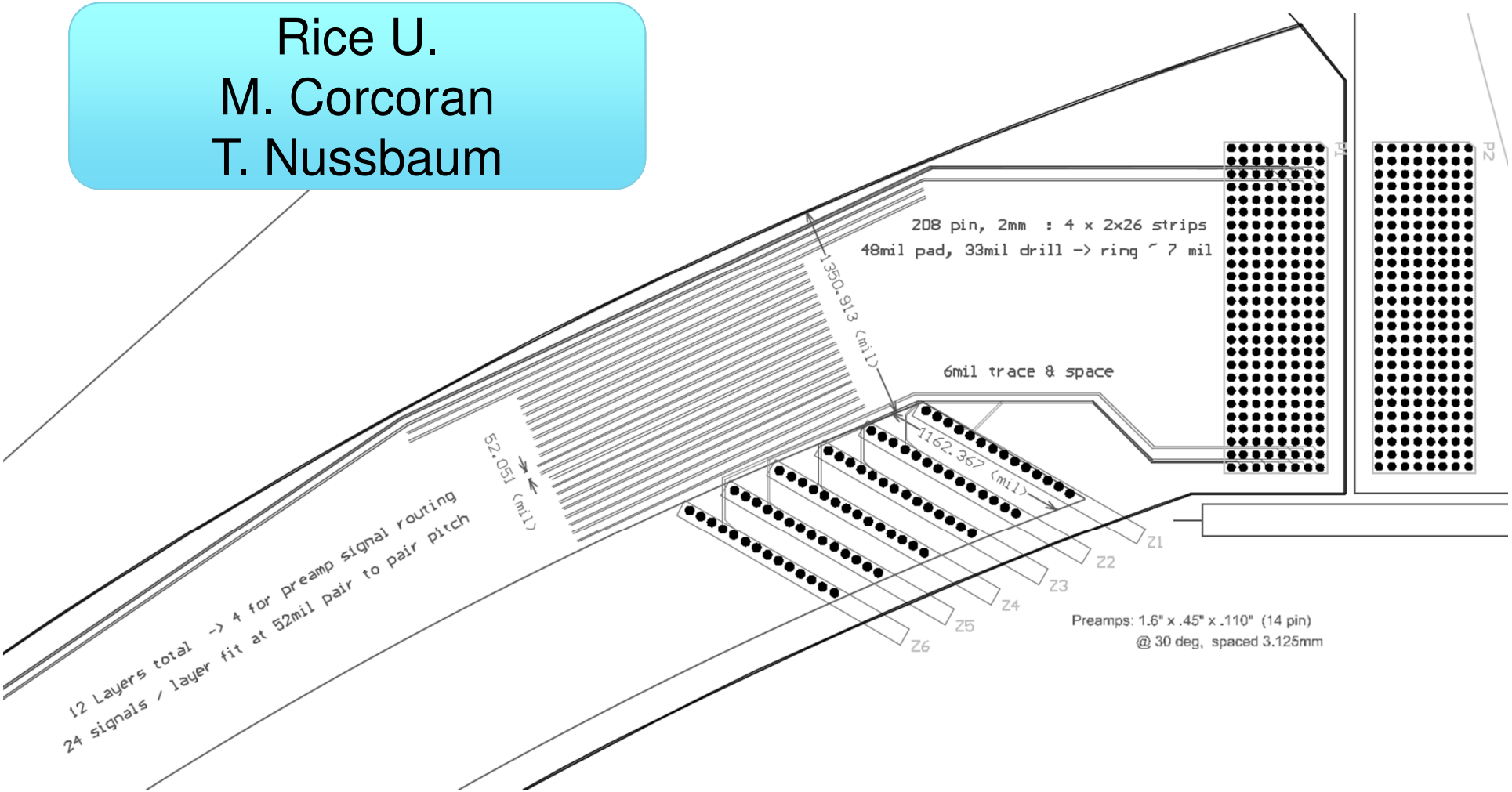
Infrastructure (Signal transmission)

- Investigated a long (55”) motherboard
  - Recommendation from Digitizer Review (April 2014)
  - Cost ineffective (+high assembly costs)
- Preamp mobo + ROC mobo
  - Effectively a transmission line board(s)
    - All components (preamp, digi, ROC) mezzanines
    - HV, slow controls on board

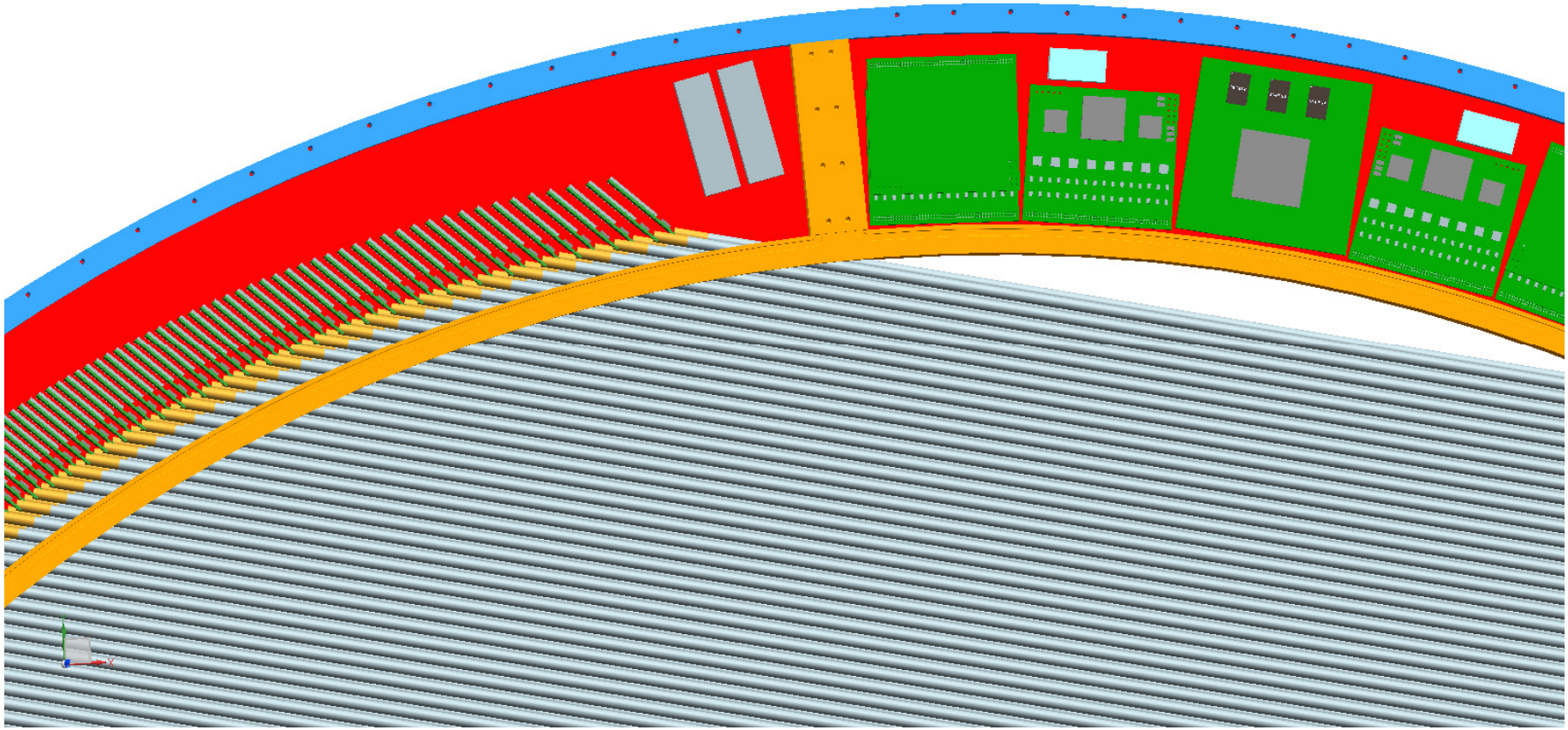


Transmission boards

Rice U.
M. Corcoran
T. Nussbaum



Assembly



Infrastructure (Power distribution)

- Five low voltage levels needed (<5V)
- 48V power line from outside the cryostat
  - Allows for lower current (B field)
- DC-DC converters outside the stations step down to a suitable voltage
- Regulators inside the gas volume for actual distribution

ES&H

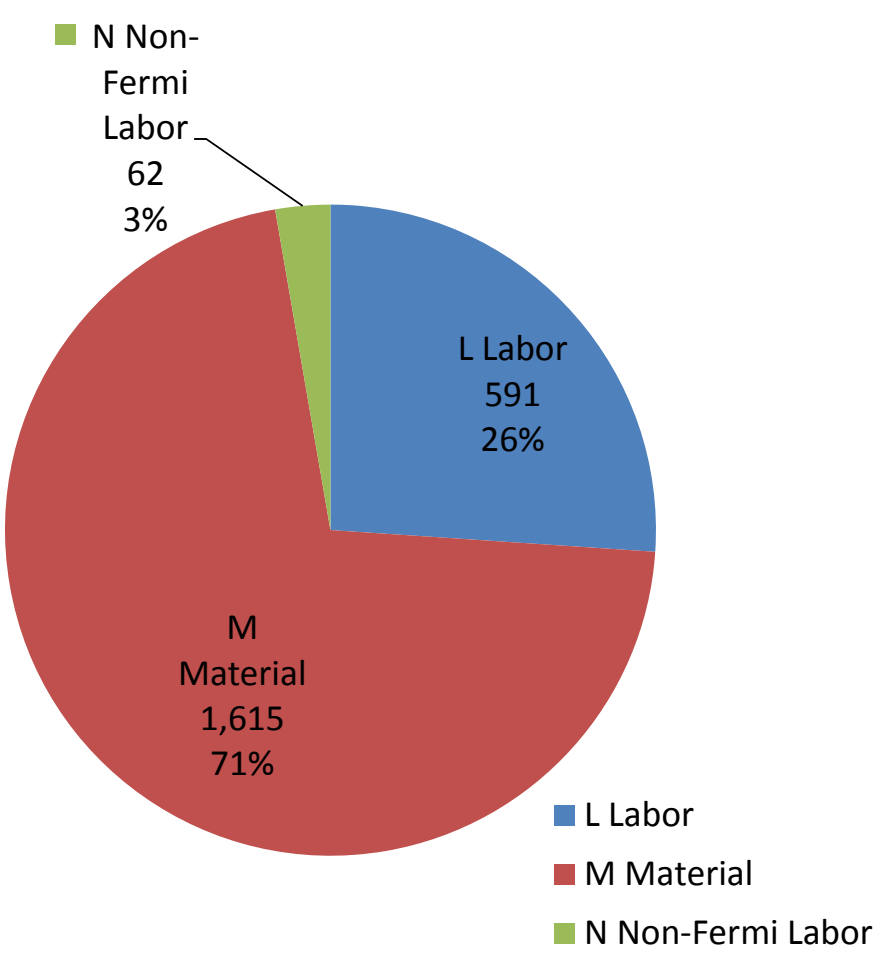
- High voltage is moderate by Fermilab standards
  1500V, <1mA and ~10mJ stored energy on any one line
- Power is from 48V supplies which have passive (limited capacity) and active (monitor and trip) current limit

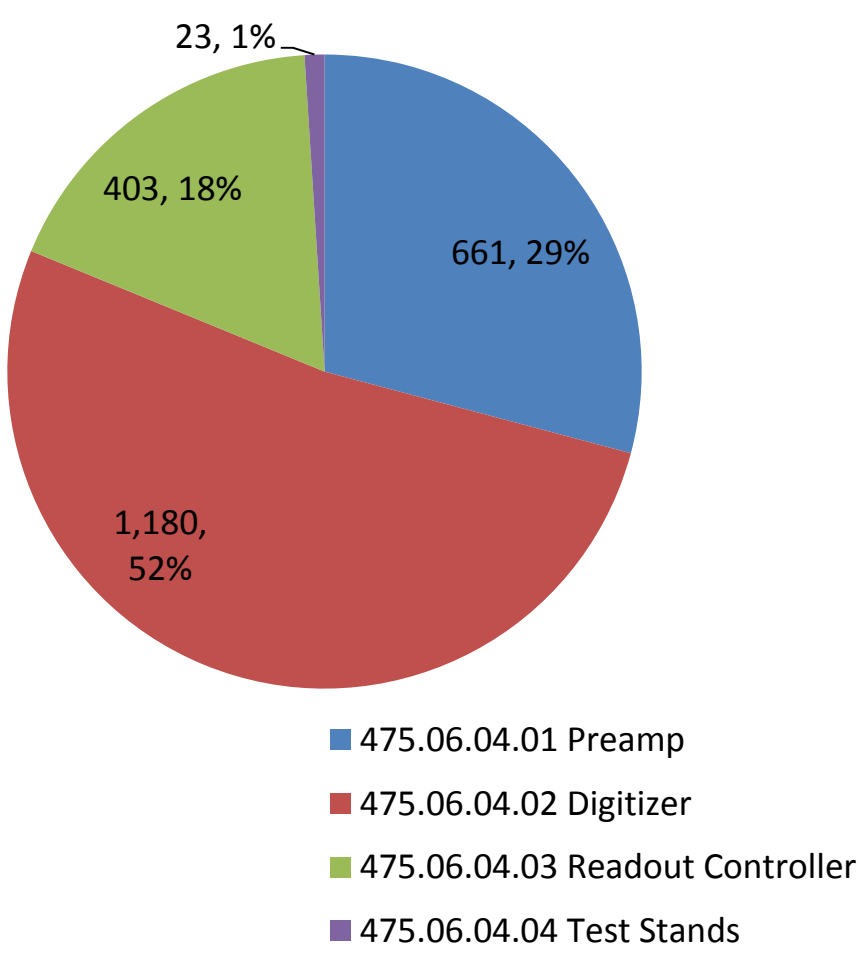
Cost Table

	Base Cost (AY K$)			Estimate Uncertainty (on remaining costs)	% Contingency on ETC	Total Cost
	M&S	Labor	Total			
475.06 Tracker						
475.06.04 Tracker Front End Electronics						
475.06.04.01 Preamp	563	98	661	216	35%	877
475.06.04.02 Digitizer	793	387	1,180	255	26%	1,435
475.06.04.03 Readout Controller	316	88	403	161	42%	564
475.06.04.04 Test Stands	4	19	23	11	145%	34
Grand Total	1,676	591	2,267	643	32%	2,910

Cost Breakdown

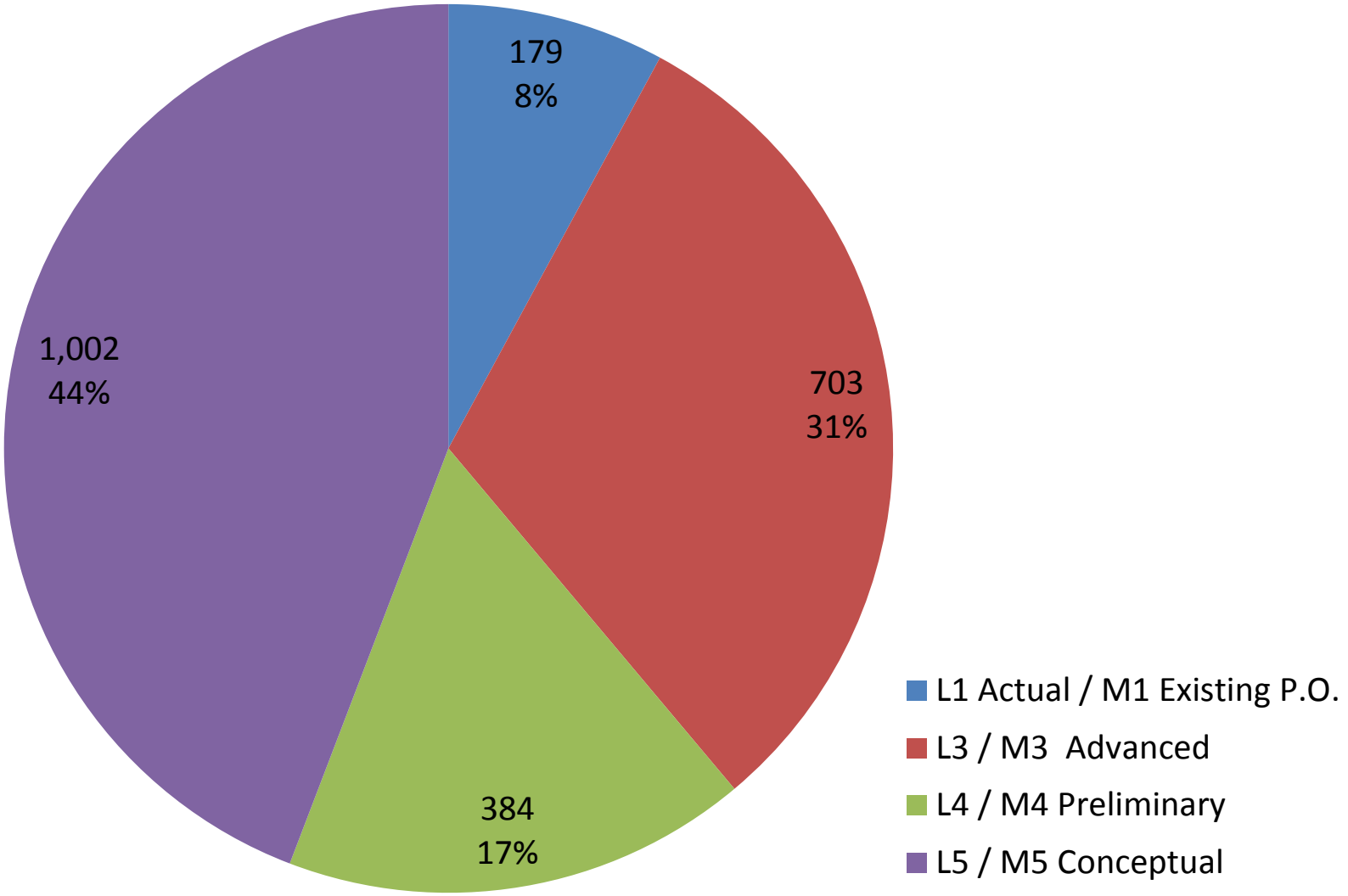
Base Cost (AY K$)





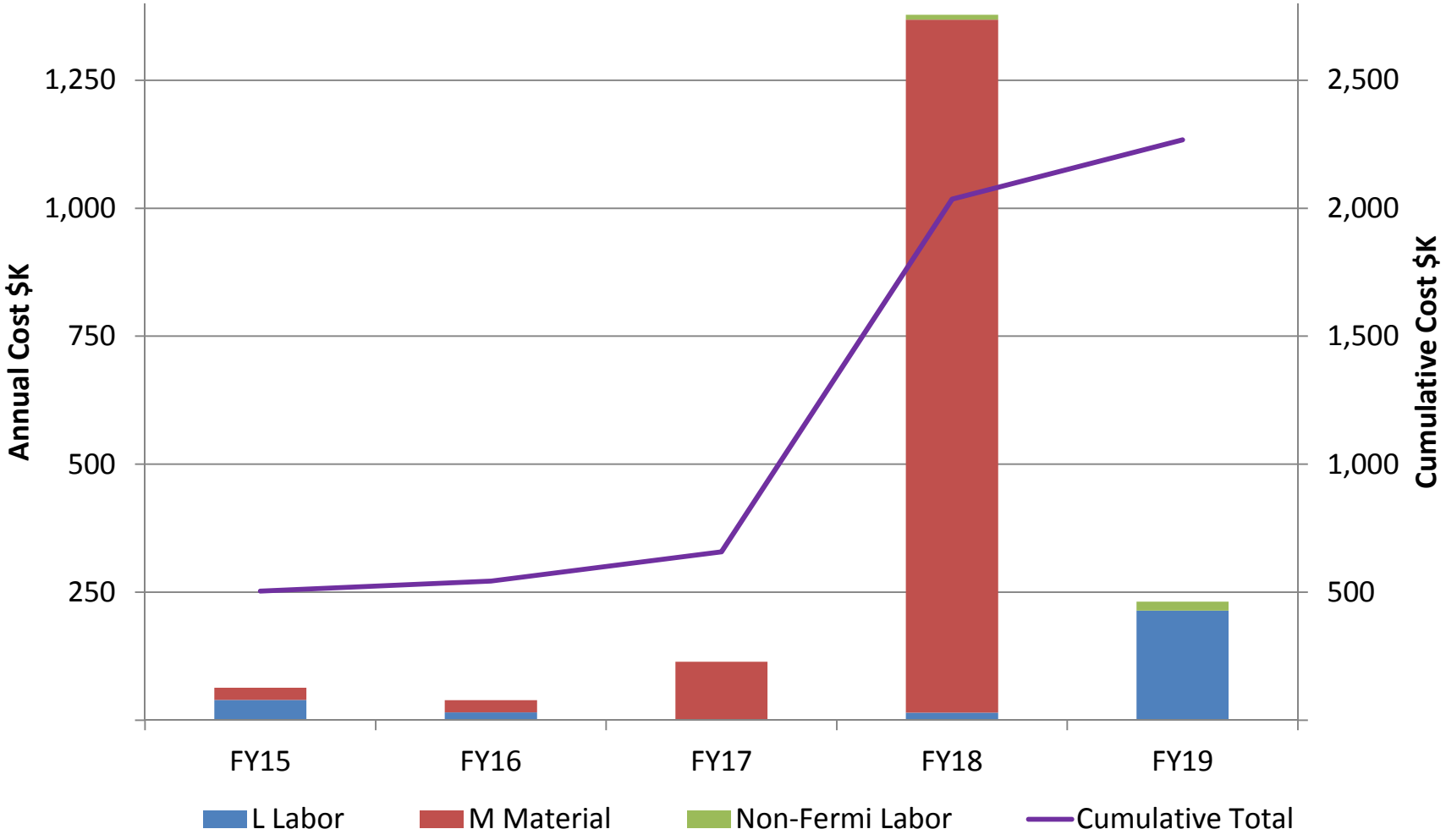
Quality of Estimate

Base Cost (AY K$)



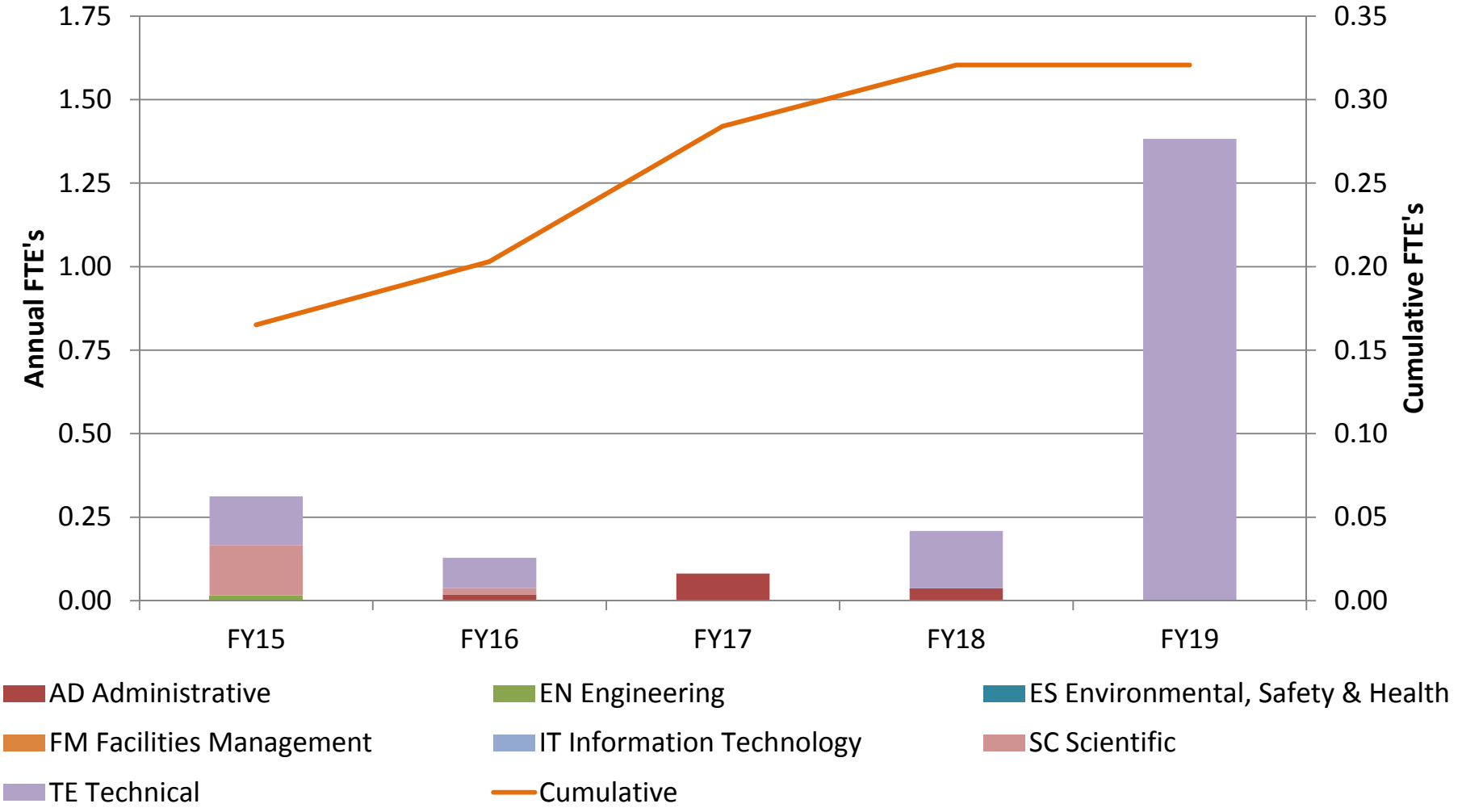
Labor & Material by FY

Base Cost (AY K$)



Labor Resources by FY

FTEs by Discipline

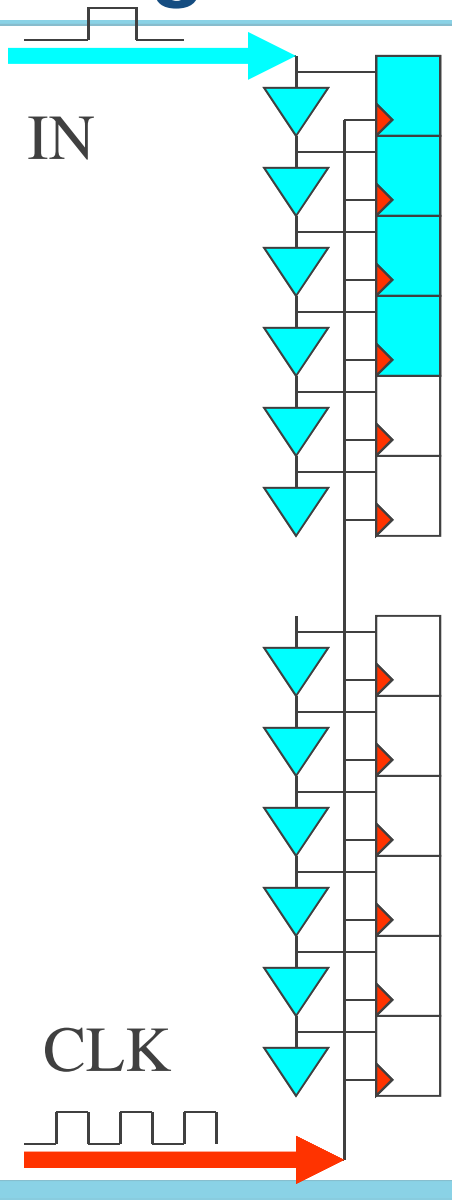


Conclusion

- Design of front end electronics meets the requirements
- Advanced prototypes on all sub-systems
- Initial integration pass under way
- Solid cost estimate based mostly on quotes

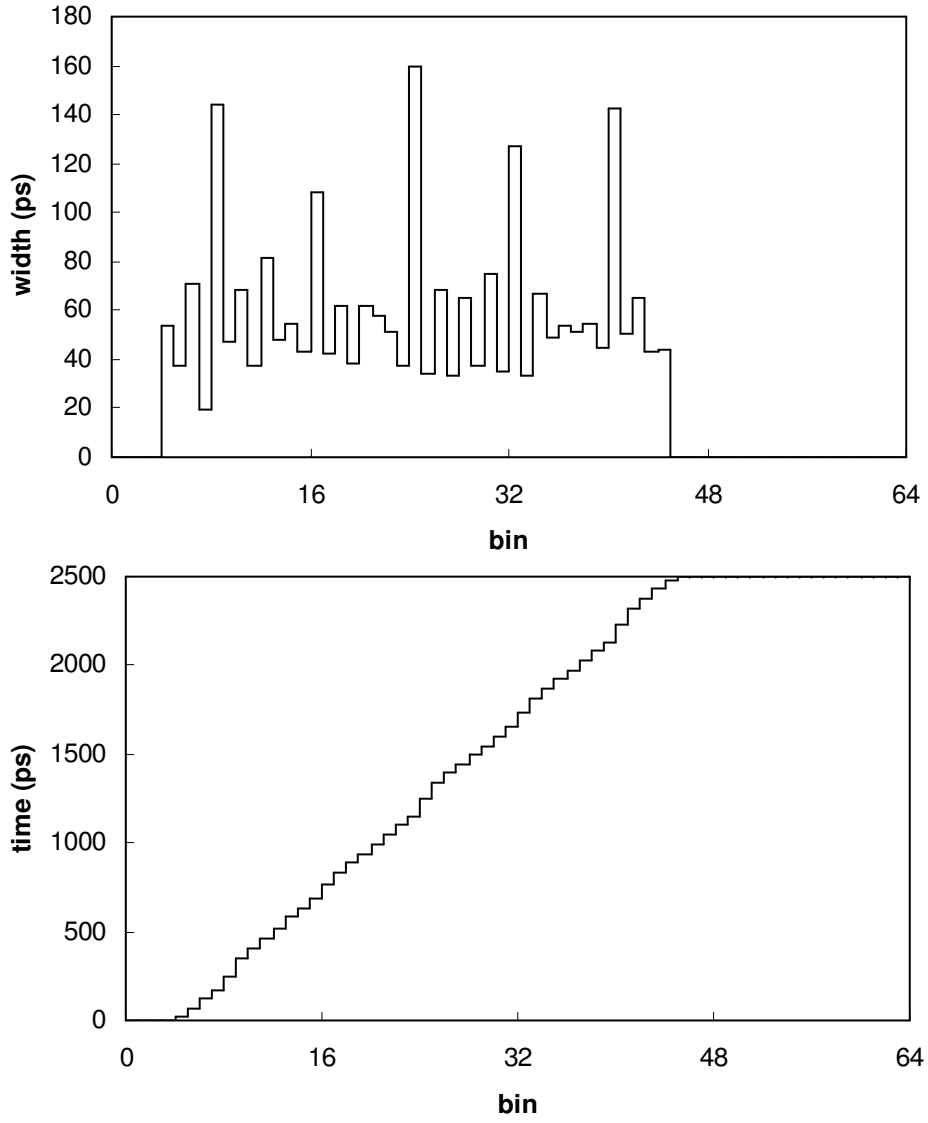
Backup

TDC Using FPGA Logic Chain Delay



- This scheme uses current FPGA technology
- Low cost chip family can be used. (e.g. EP2C8T144C6 $31.68)
- Fine TDC precision can be implemented in slow devices (e.g., 25 ps (RMS) in a 400 MHz chip).

Autocalibration using histogram method



- It provides a bin-by-bin calibration at certain temperature.
- It is a turn-key solution (bin in, ps out)
- It is semi-continuous (auto update LUT every 16K events)