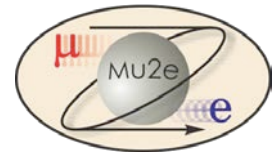




Mu2e CD-2 Review Trigger & DAQ

10/21/2014

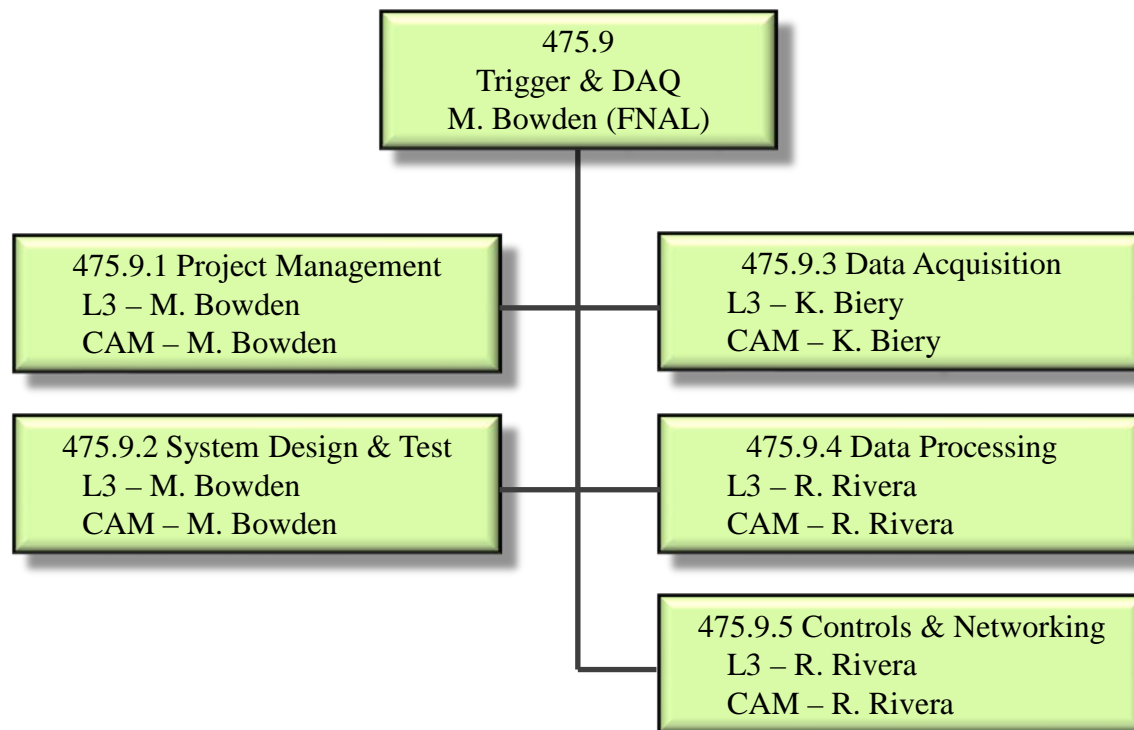


Topics

- 475.9.1 Management
Organization, Schedule, Cost Estimates, QA, Risks, ES&H
- 475.9.2 System Design & Test
Requirements, System Architecture, System Test
- 475.9.3 Data Acquisition
Data Readout, Timing System
- 475.9.4 Data Processing
Online Computing and Data Filters
- 475.9.5 Controls & Networking
General-purpose Networking, Slow Controls, Control Room

Management

Management



Management

- Basis of Estimate
 - 85% of DAQ costs are labor, mainly related to software and firmware development
 - software is always difficult to estimate
 - labor estimates use a top-down approach and are based on a recent project (NOvA) of similar scope and complexity
 - significant overlap in labor resources and software
 - NOvA effort involved both hardware and firmware development, Mu2e is firmware only (reduced engineering cost)
 - Mu2e makes greater use of existing software developed for NOvA and other experiments (reduced software development cost)
 - M&S estimates are based on current catalog pricing

Management

WBS 9 Trigger & DAQ

Costs are fully burdened in AY \$k

	Base Cost (AY K\$)			Estimate Uncertainty (on remaining budget)	% Contingency on (on remaining budget)	Total Cost
	M&S	Labor	Total			
475.09.01 TDAQ Project Management	3	1,162	1,165	118	23%	1,284
475.09.02 TDAQ System Design and Test		361	361	23	35%	385
475.09.03 Data Acquisition	317	1,513	1,831	459	37%	2,290
475.09.04 Data Processing	310	551	860	208	30%	1,068
475.09.05 Controls and Networking	125	458	583	154	34%	737
475.09.99 Risk Based Contingency				244	-	244
Grand Total	755	4,045	4,800	1,207	41%	6,007

Management

	Base Cost (AY K\$)			Estimate Uncertainty (on remaining budget)	% Contingency on (on remaining budget)	Total Cost
	M&S	Labor	Total			
475.09.01 TDAQ Project Management						
475.09.01.01 Conceptual Design (Post CD-0)	3	317	321		-	321
475.09.01.02 Preliminary & Final Design (Post CD-1)		340	340	10	-	350
475.09.01.03 Implementation & Close-out (Post CD-3)		505	505	108	21%	613
Grand Total	3	1,162	1,165	118	23%	1,284

	Base Cost (AY K\$)			Estimate Uncertainty (on remaining budget)	% Contingency on (on remaining budget)	Total Cost
	M&S	Labor	Total			
475.09.02 TDAQ System Design and Test						
475.09.02.01 Conceptual Design- Sys Design and Test		203	203		-	203
475.09.02.02 Prototype System- Sys Design and Test		91	91		-	91
475.09.02.03 Pilot System- Sys Design and Test		41	41	14	35%	56
475.09.02.04 Production System- Sys Design and Test		26	26	9	35%	35
Grand Total		361	361	23	35%	385

Management

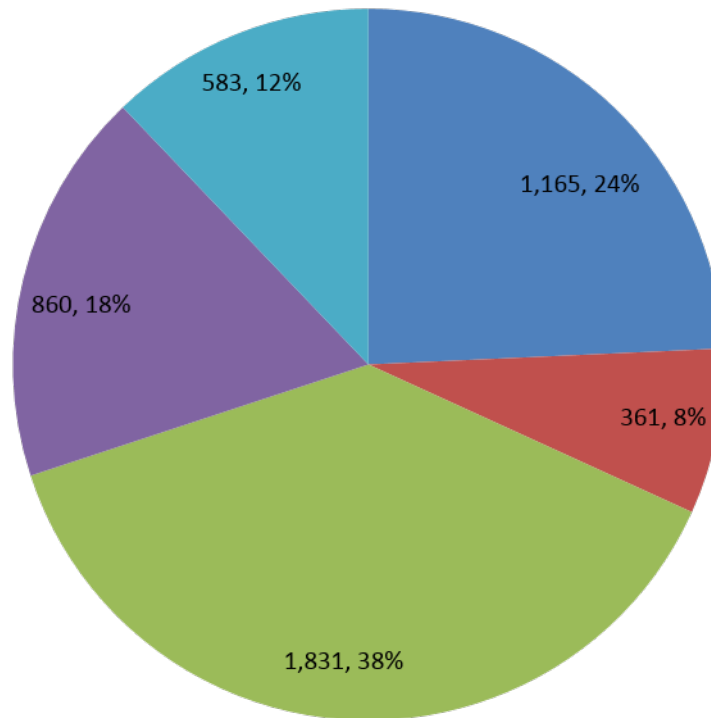
	Base Cost (AY K\$)			Estimate Uncertainty (on remaining budget)	% Contingency on (on remaining budget)	Total Cost
	M&S	Labor	Total			
475.09.03 Data Acquisition						
475.09.03.01 Prototype System- Data Acquisition	16	363	379		-	379
475.09.03.02 Pilot System- Data Acquisition	58	487	545	178	52%	723
475.09.03.03 Production System- Data Acquisition	244	663	907	281	31%	1,188
Grand Total	317	1,513	1,831	459	37%	2,290

	Base Cost (AY K\$)			Estimate Uncertainty (on remaining budget)	% Contingency on (on remaining budget)	Total Cost
	M&S	Labor	Total			
475.09.04 Data Processing						
475.09.04.01 Prototype System- Data Processing		133	133		-	133
475.09.04.02 Pilot System- Data Processing	41	196	237	77	38%	313
475.09.04.03 Production System- Data Processing	269	222	491	131	27%	622
Grand Total	310	551	860	208	30%	1,068

	Base Cost (AY K\$)			Estimate Uncertainty (on remaining budget)	% Contingency on (on remaining budget)	Total Cost
	M&S	Labor	Total			
475.09.05 Controls and Networking						
475.09.05.01 Prototype System- Control and Network		88	88		-	88
475.09.05.02 Pilot System- Control and Network	13	150	163	55	44%	218
475.09.05.03 Production System- Control and Network	112	219	331	99	30%	431
Grand Total	125	458	583	154	34%	737

Management

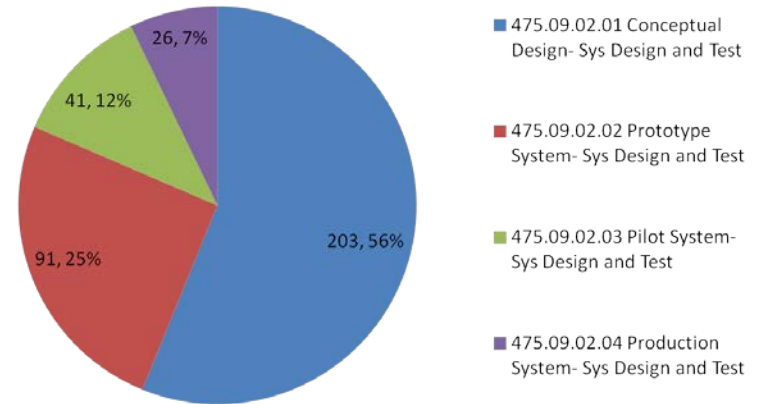
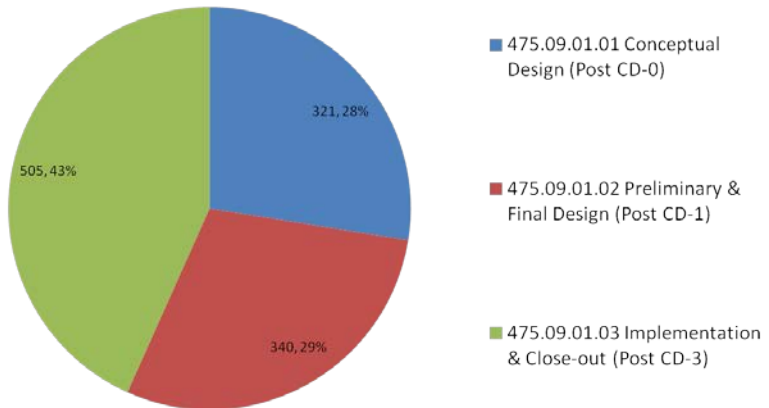
Cost Breakdown



- 475.09.01 TDAQ Project Management
- 475.09.02 TDAQ System Design and Test
- 475.09.03 Data Acquisition
- 475.09.04 Data Processing
- 475.09.05 Controls and Networking

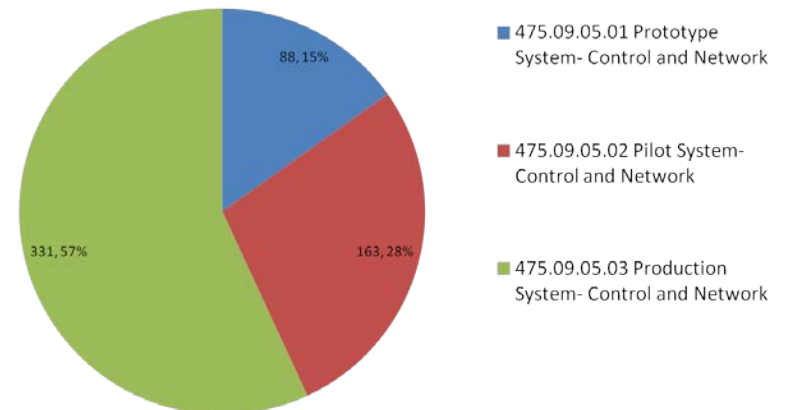
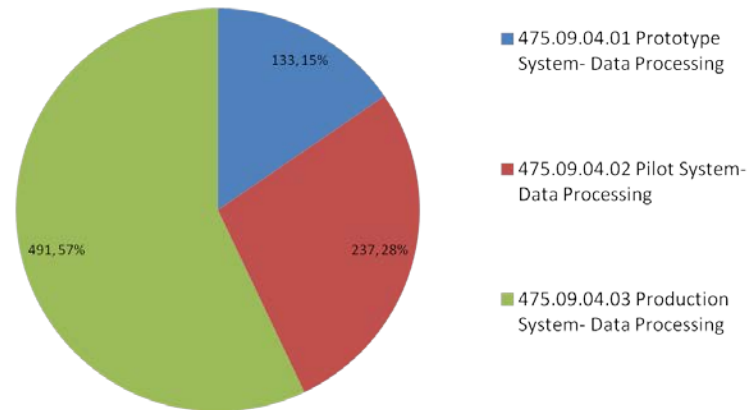
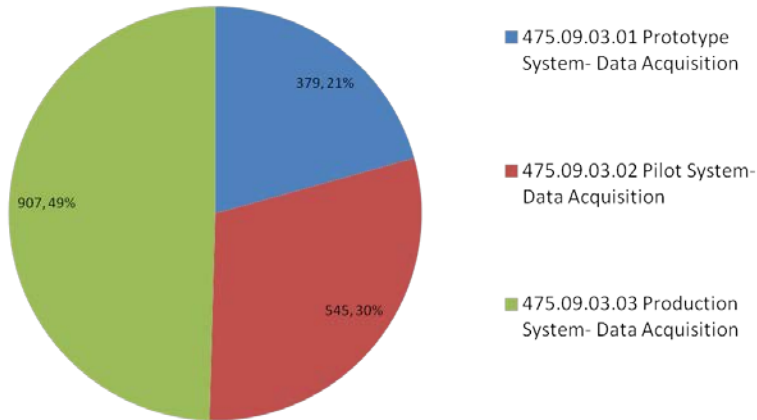
Management

Cost Breakdown (by L3 Activity)



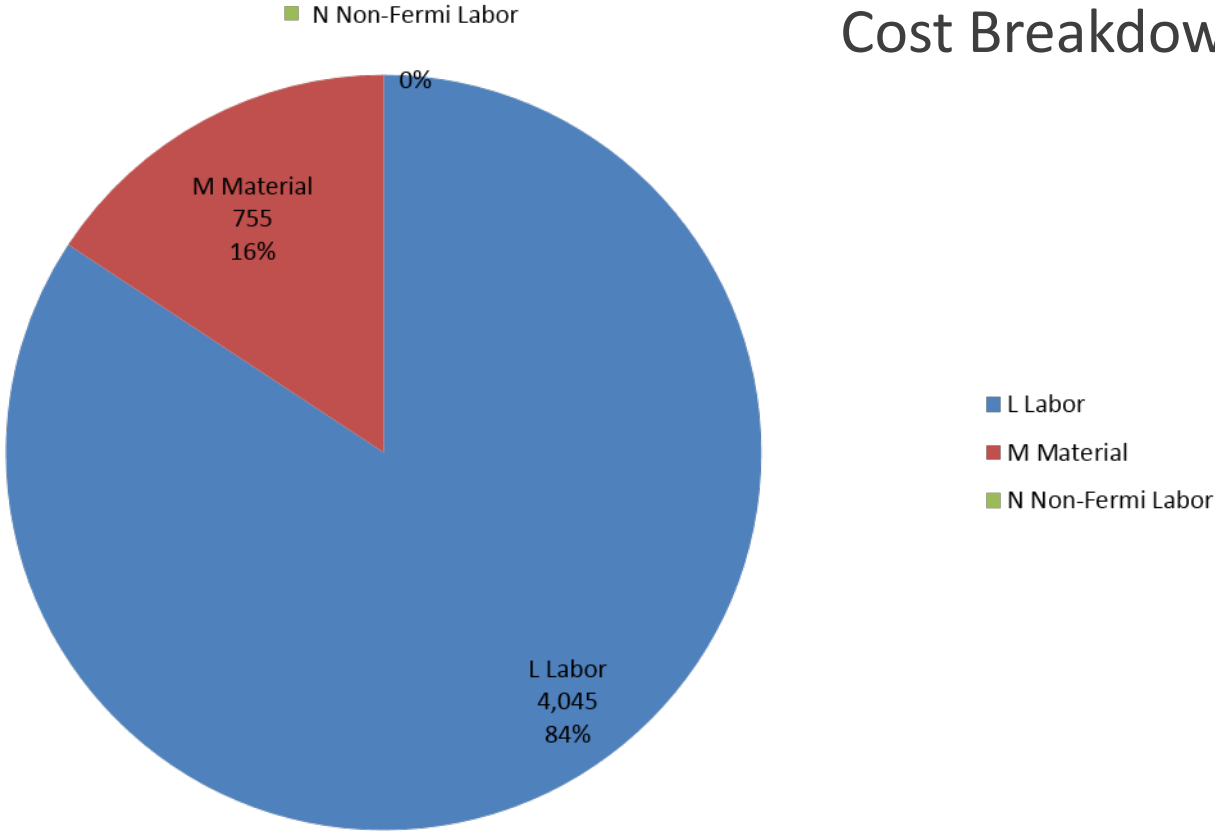
Management

Cost Breakdown (by L3 Activity)



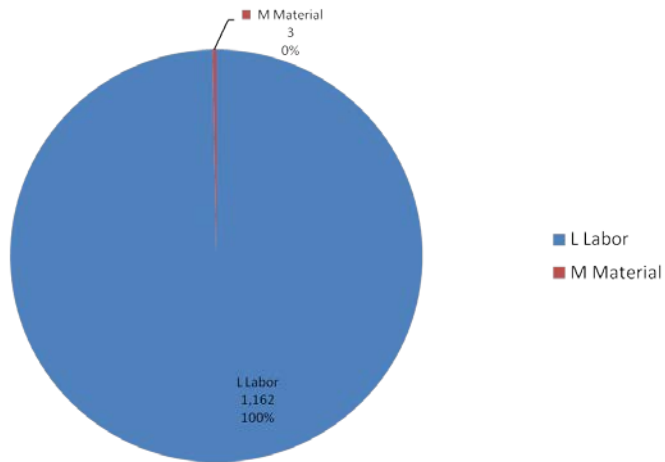
Management

Cost Breakdown

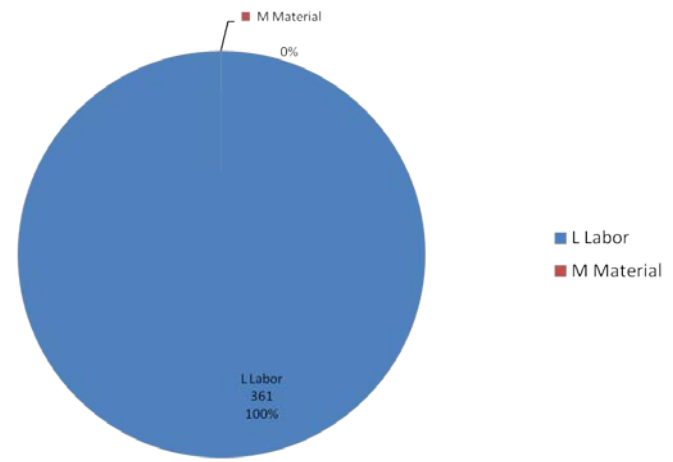


Management

Cost Breakdown (by L3 Activity)



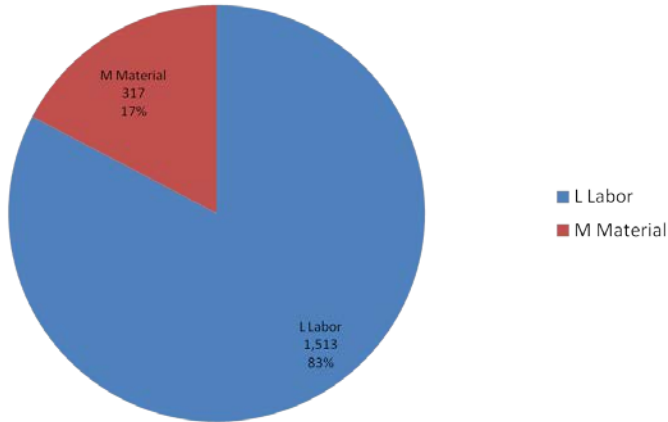
475.09.01



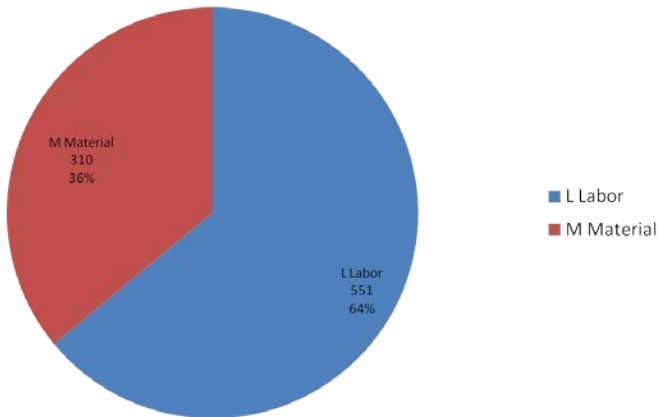
475.09.02

Management

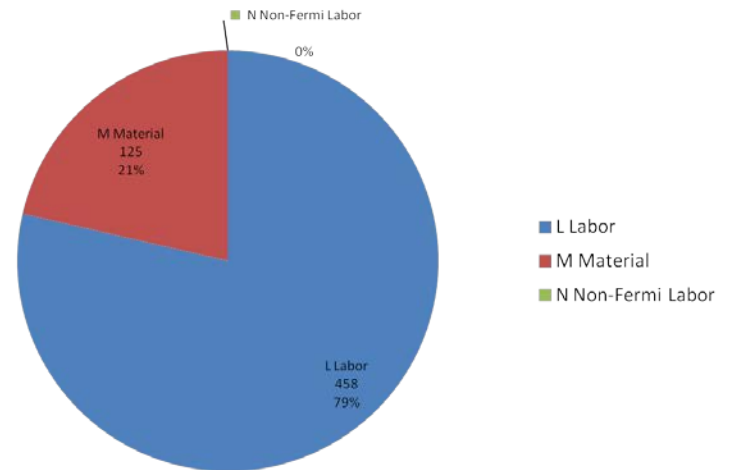
Cost Breakdown (by L3 Activity)



475.09.03



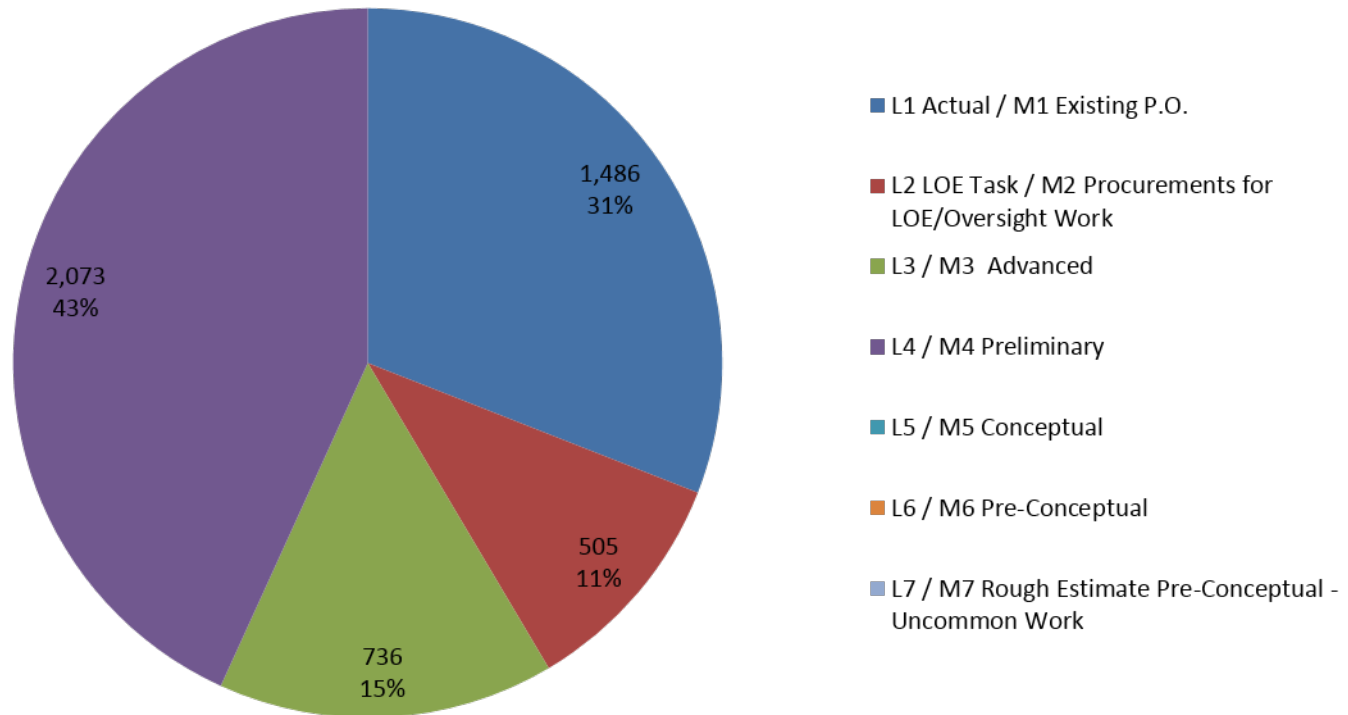
475.09.04



475.09.05

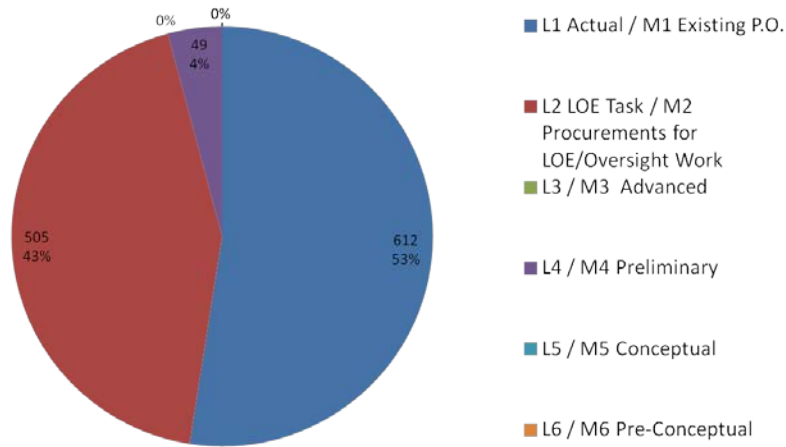
Management

Quality of Estimate

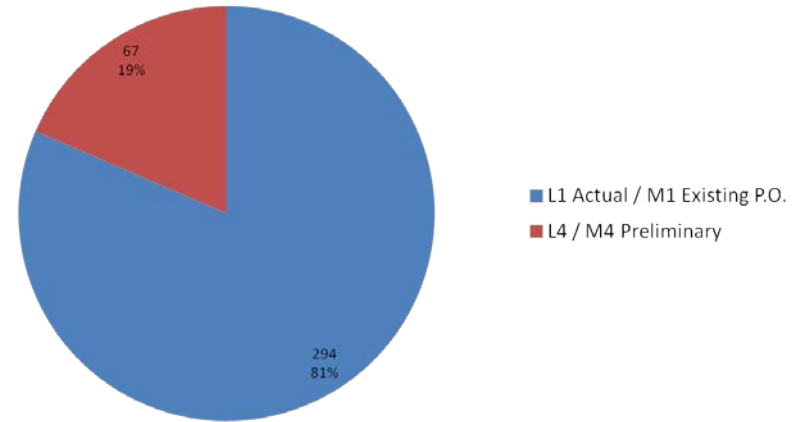


Management

Quality of Estimate (by L3 Activity)



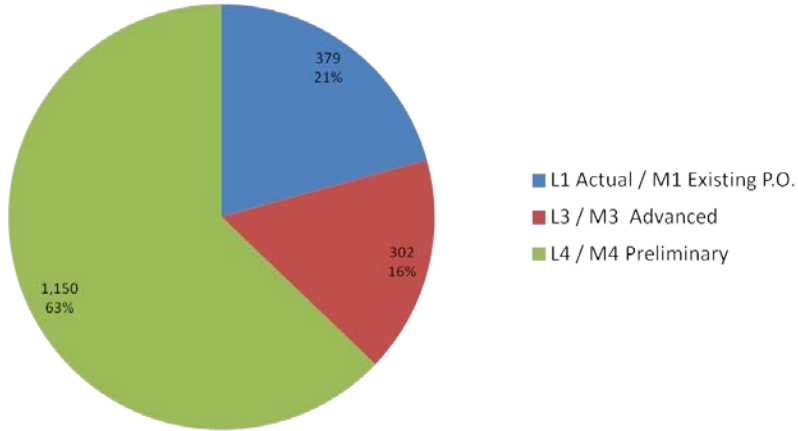
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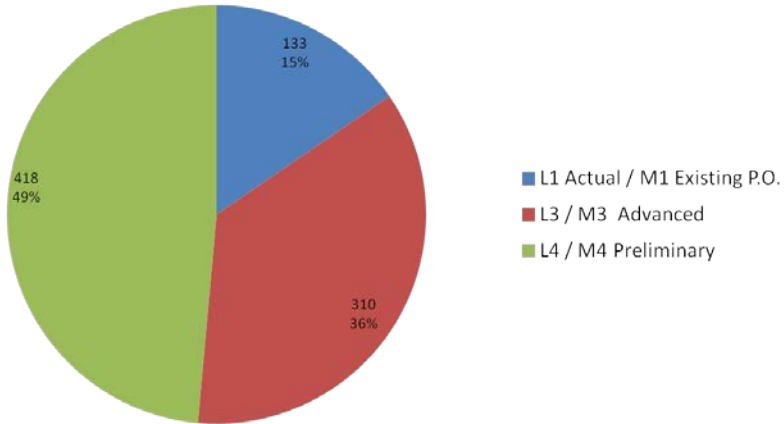
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Management

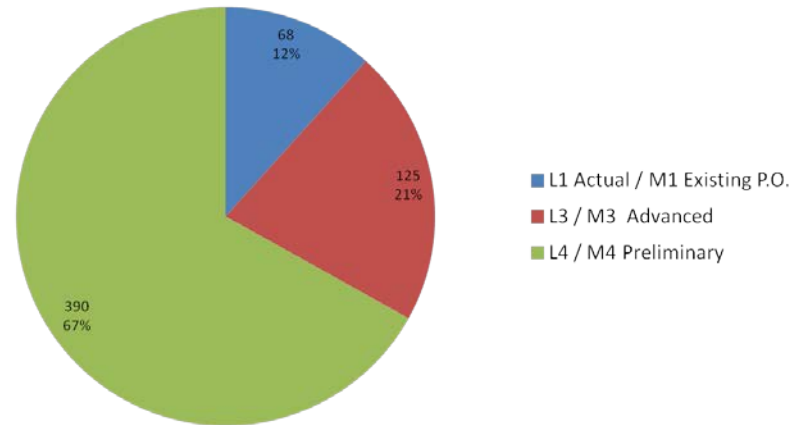
Quality of Estimate (by L3 Activity)



475.09.03



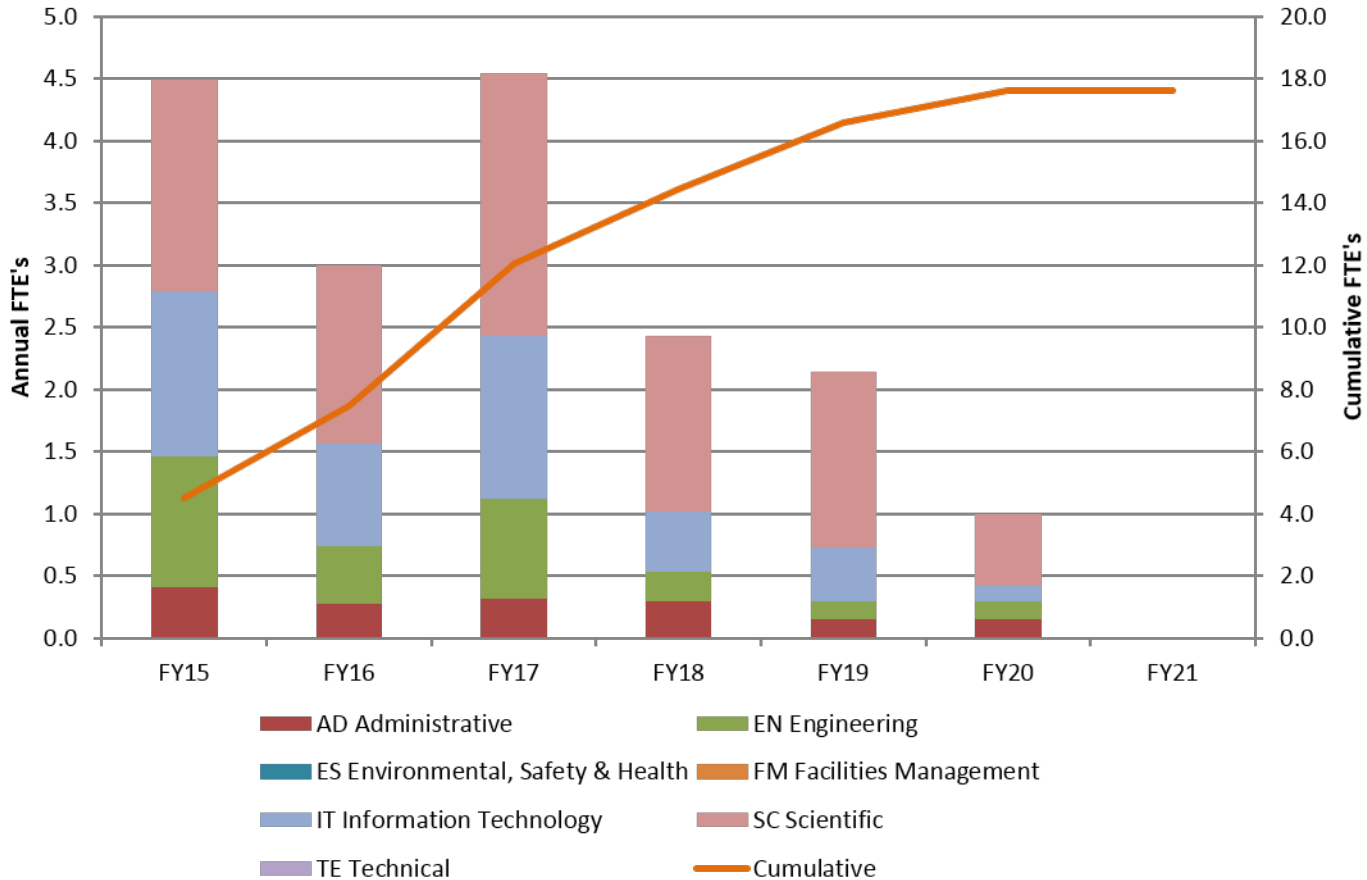
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475.09.05

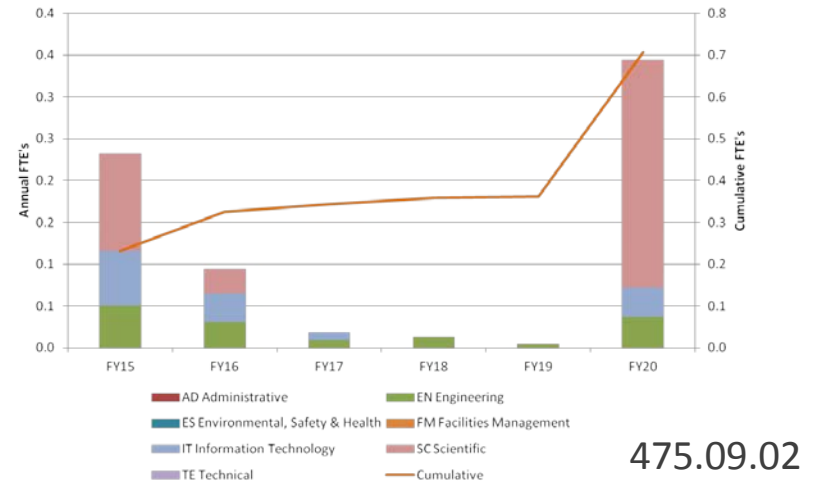
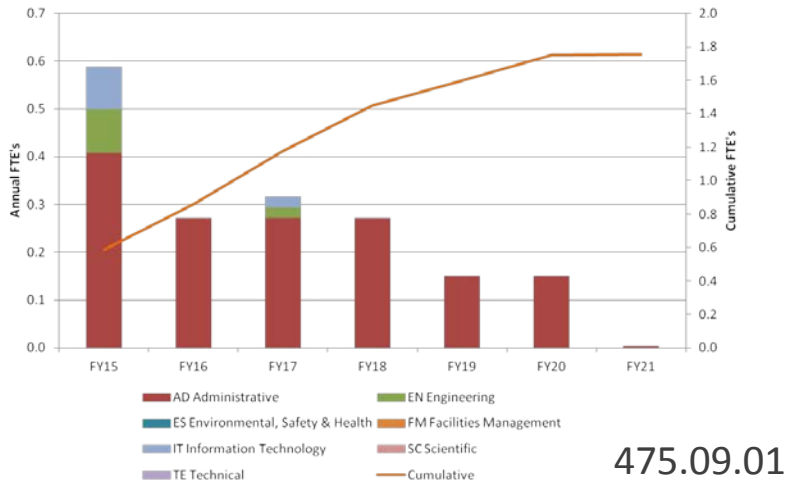
Management

Resources by FY



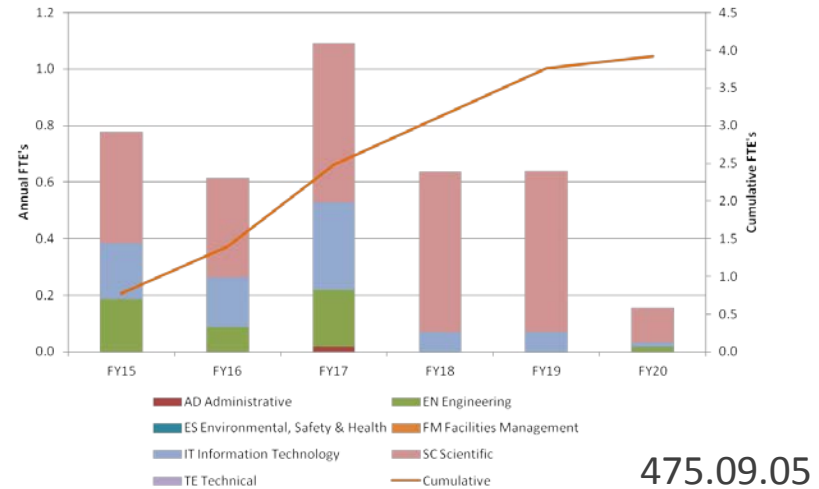
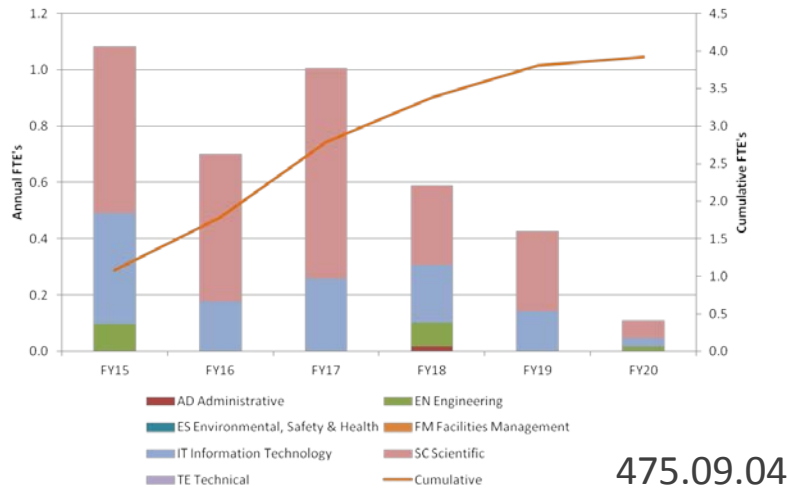
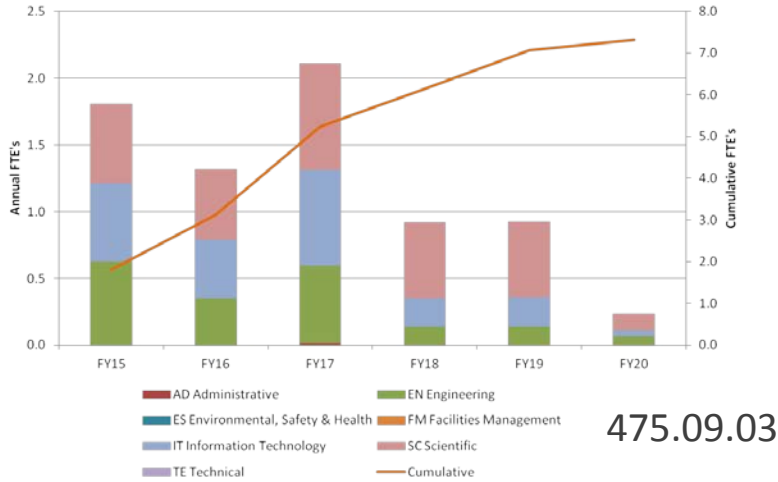
Management

Resources by FY (by L3 Activity)



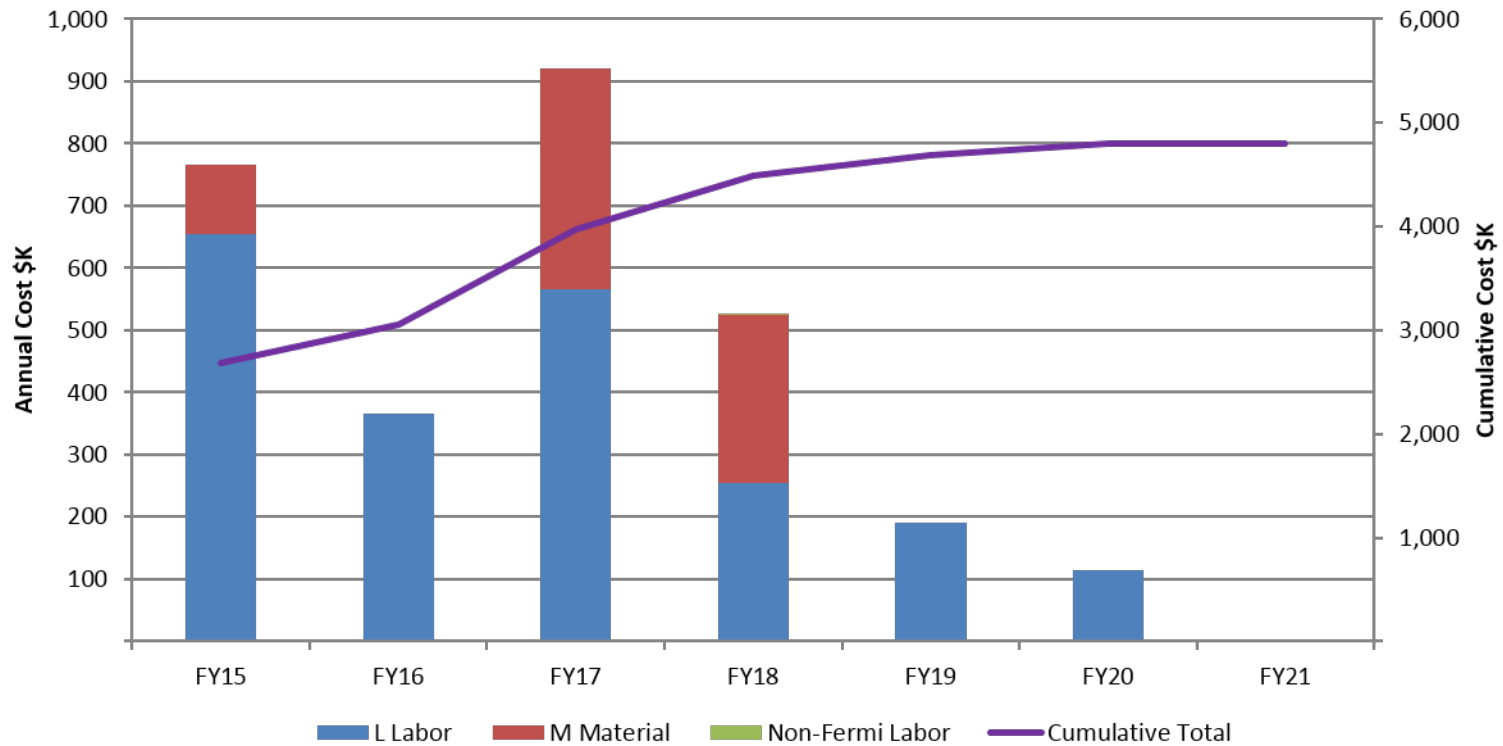
Management

Resources by FY (by L3 Activity)



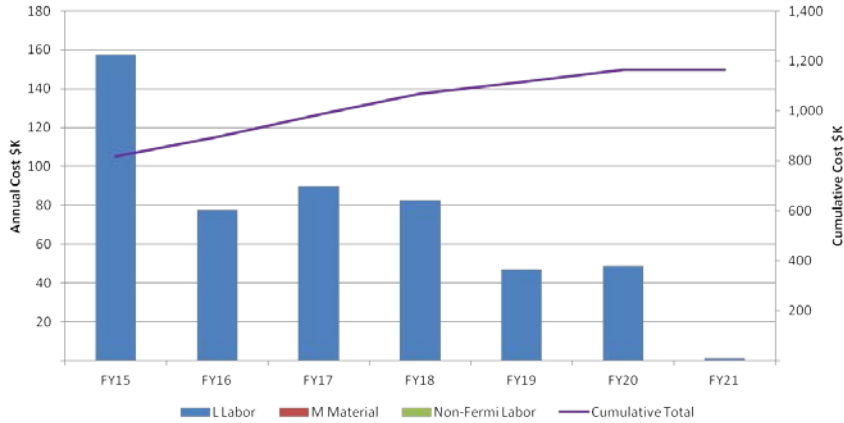
Management

Resources by FY

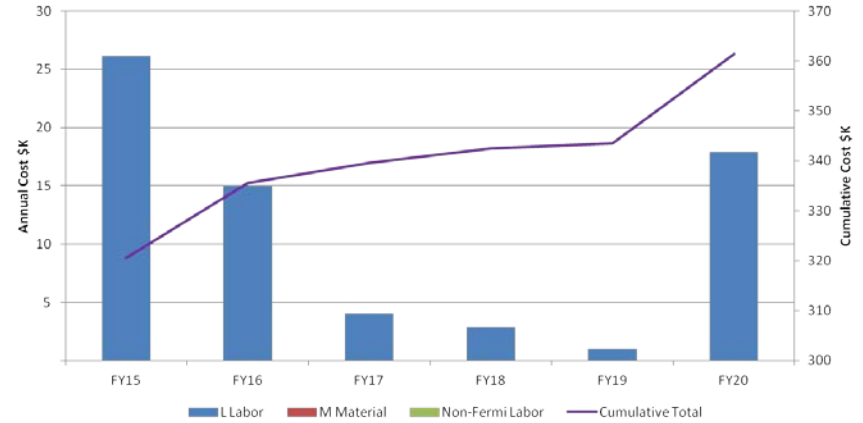


Management

Resources by FY (by L3 Activity)



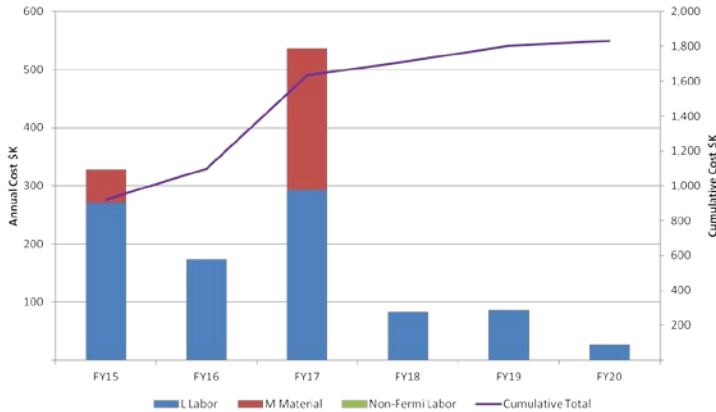
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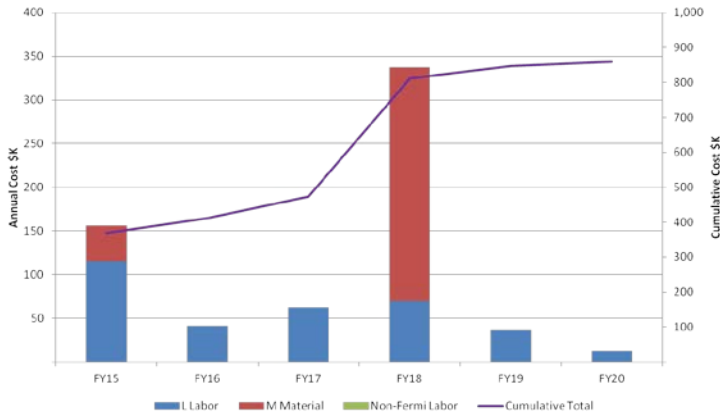
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Management

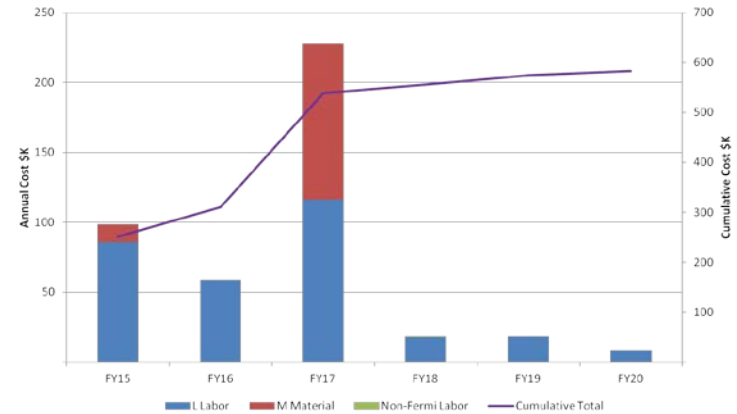
Resources by FY (by L3 Activity)



475.09.03

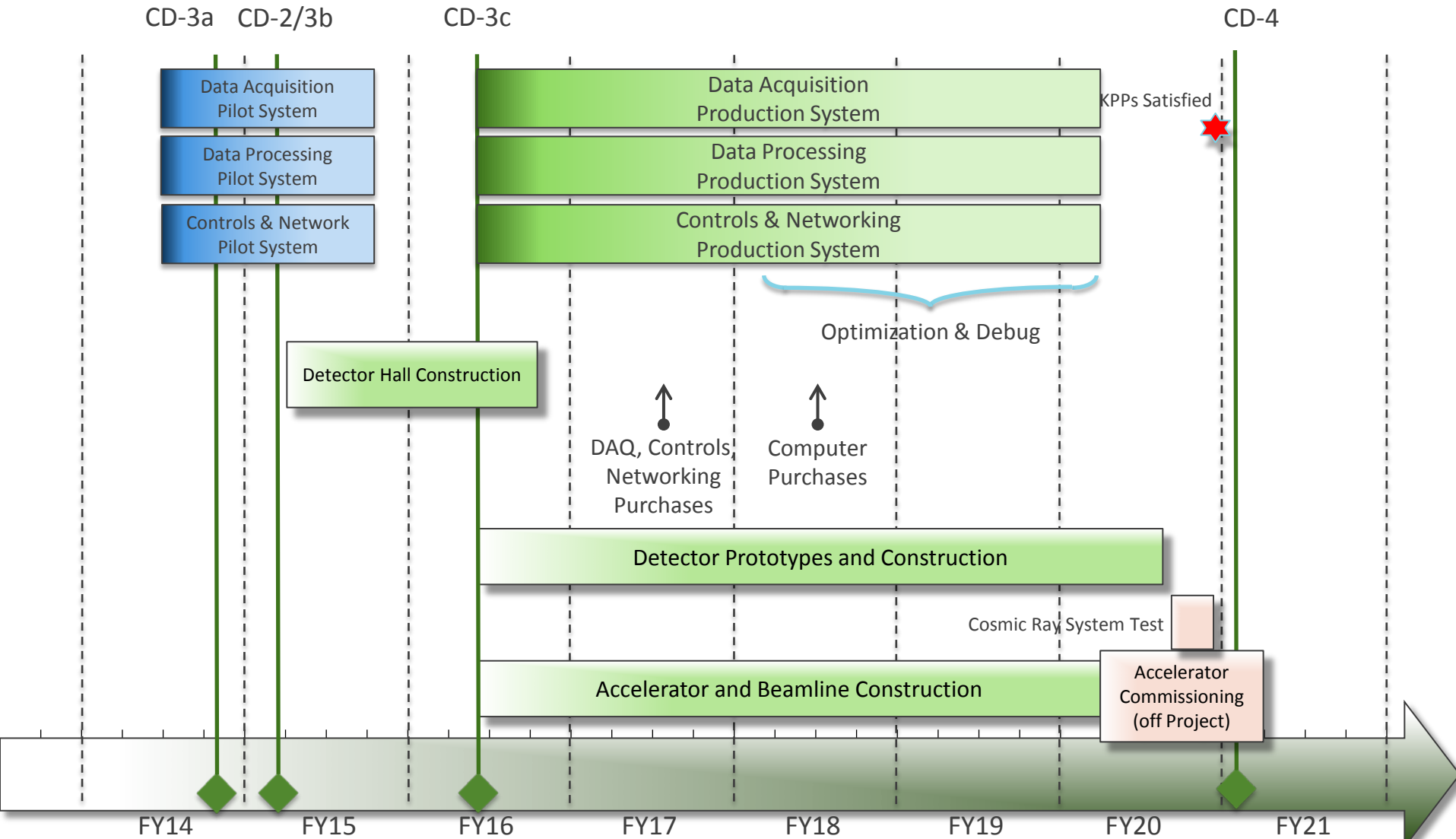


475.09.04



475.09.05

Management



Management

Major Milestones

- Completion of Pilot System development for Data Acquisition, Data Processing, and Controls and Networking tasks (July 2015)
- Completion of Production System development for Data Acquisition, Data Processing, and Controls and Networking tasks (January 2020)
 - last two years are optimization & debug at reduced level of effort
- Cosmic Ray Test (final integration with detectors and full readout test) (June 2020)

Management

Improvements since CD-1

- better data rate estimates due to improved background simulations
- switch to a triggered CRV readout to accommodate higher background rates and lower thresholds (CRV data not needed for online analysis)
- rejection rate reduced from 99.8% to 99.0% to allow independent Calorimeter filters

Management

Performance

- Tests have been performed on the primary DAQ interfaces - digitizer to readout controller (LVDS), readout controller to data transfer controller (optical link), and data transfer controller to DAQ server (PCIe) to verify bandwidth requirements
- Optimized version of the online Tracker filter meets processing requirement

Management

Remaining work before CD-3

- Development and test of a small (15%) DAQ Pilot system
 - end-to-end data transfer test
 - DAQ and detector Readout Controller (ROC) interface tests
 - preliminary Calorimeter filter benchmarks

Management

Quality Assurance

- DAQ system can be tested to a high level of confidence using simulated data, prior to Cosmic Ray test
- Full DAQ system is a scaled version of the Pilot system
- In-situ testing - diagnostic features include monitoring of data link bit-error rate and optical power levels, memory and processor tests using large simulated data sets

Management

Risks

- Insufficient manpower for DAQ software (TRIG-128)
 - Cause: uncosted labor resources are not available for scheduled tasks
 - Mitigation strategy: use additional costed labor (~\$500k)
- Insufficient DAQ online processing (TRIG-130)
 - Cause: improvements in processor performance and filter optimization are less than expected
 - Mitigation strategy: add DAQ servers (~\$75k)

Management

ES&H

- ES&H issues are minimal
 - High voltage (208 VAC, no exposed connections)
 - Class 1 lasers (eye safe)
 - no radiation or magnetic field issues

System Design & Test

System Design & Test

Requirements

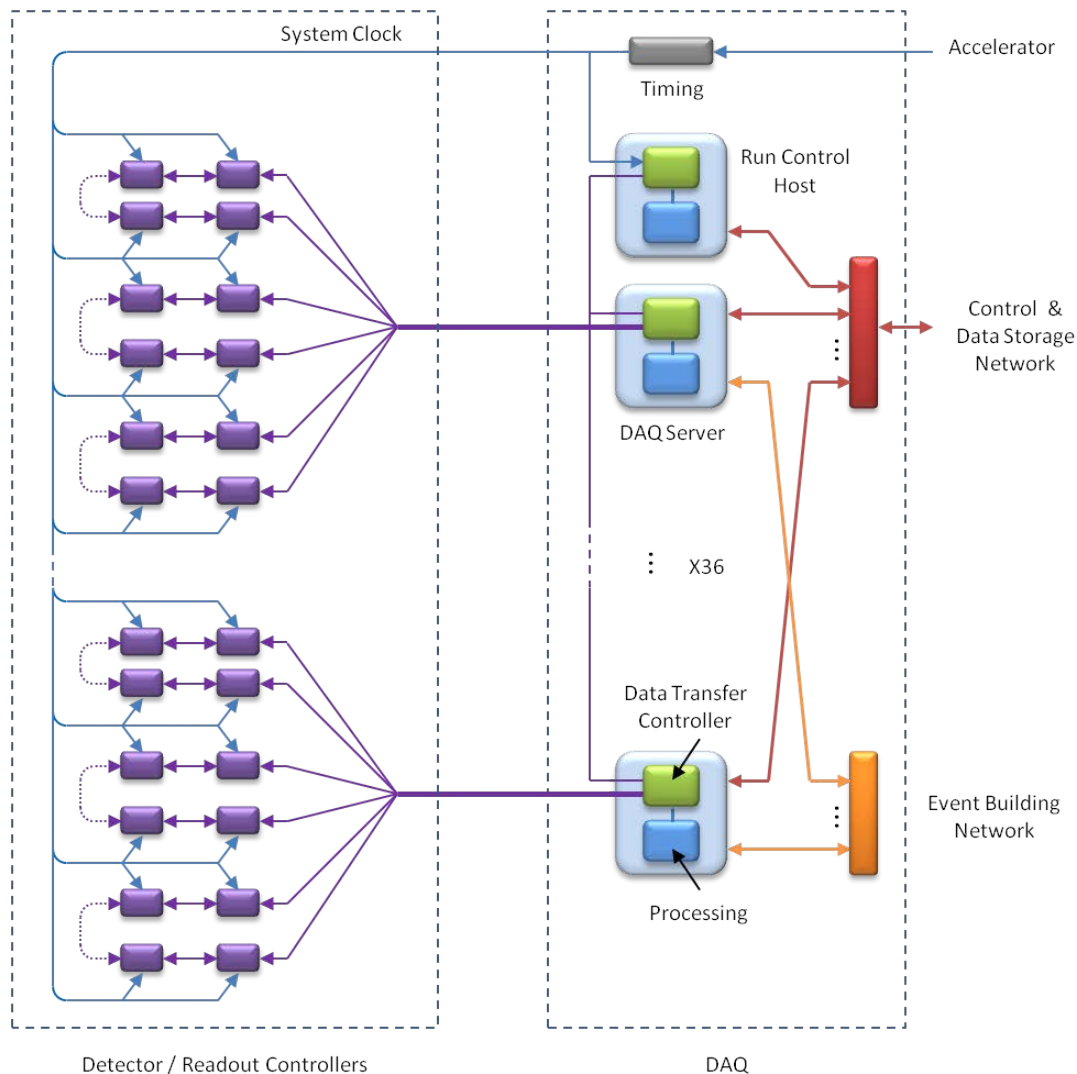
- Requirements for the DAQ are described in mu2e-docdb 1150.
- Collect and assemble data from the Tracker (~13 GBytes/sec) and Calorimeter (~8 GBytes/sec) for online analysis.
- Provide online filtering to reduce data Tracker & Calorimeter data volume by $\geq 99\%$.
- Combine with data from CRV, Extinction and Target Monitors for transfer to offline storage.

System Design & Test

Requirements

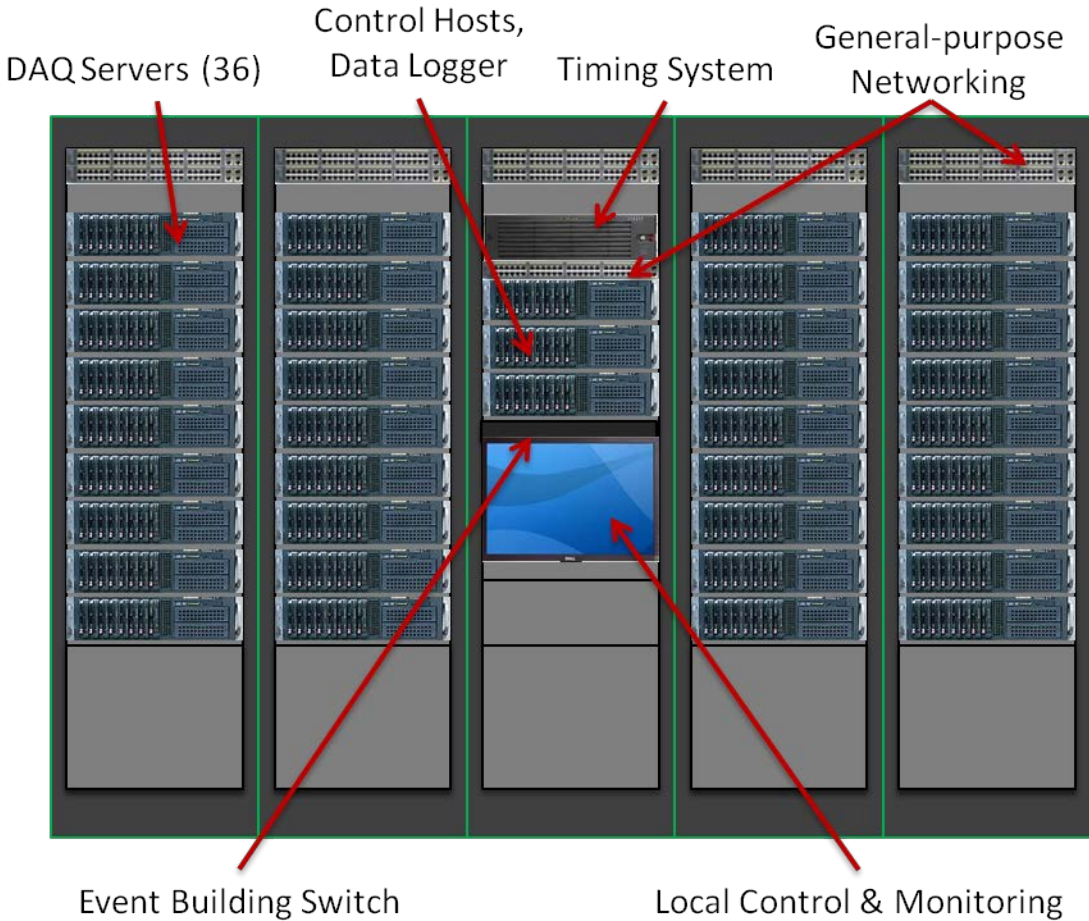
- Provide global timing synchronization
- Provide fast and slow control networks
- Provide connections to offline storage and site networking
- Provide control room/operator interfaces

System Design & Test

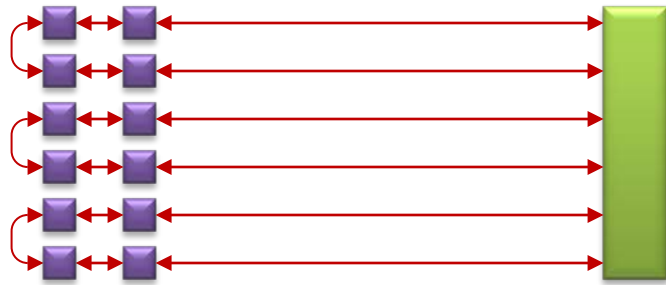


- architecture supports both streaming (Tracker, Calorimeter) and triggered (CRV) readout
- DAQ Servers handle data readout, event building and processing
- bidirectional front-end interface for fast control and readout
- large front-end buffers for uniform data transfer
- all commercial DAQ hardware
- scalable... 1 GByte/sec per DAQ server

System Design & Test

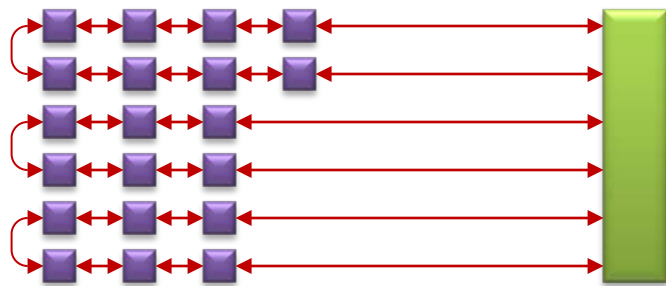


System Design & Test



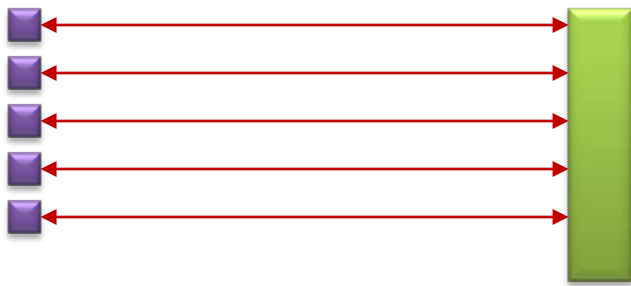
Tracker

20 DAQ Servers
12 ROCs/Server



Calorimeter

12 DAQ Servers
20 ROCs/Server



CRV

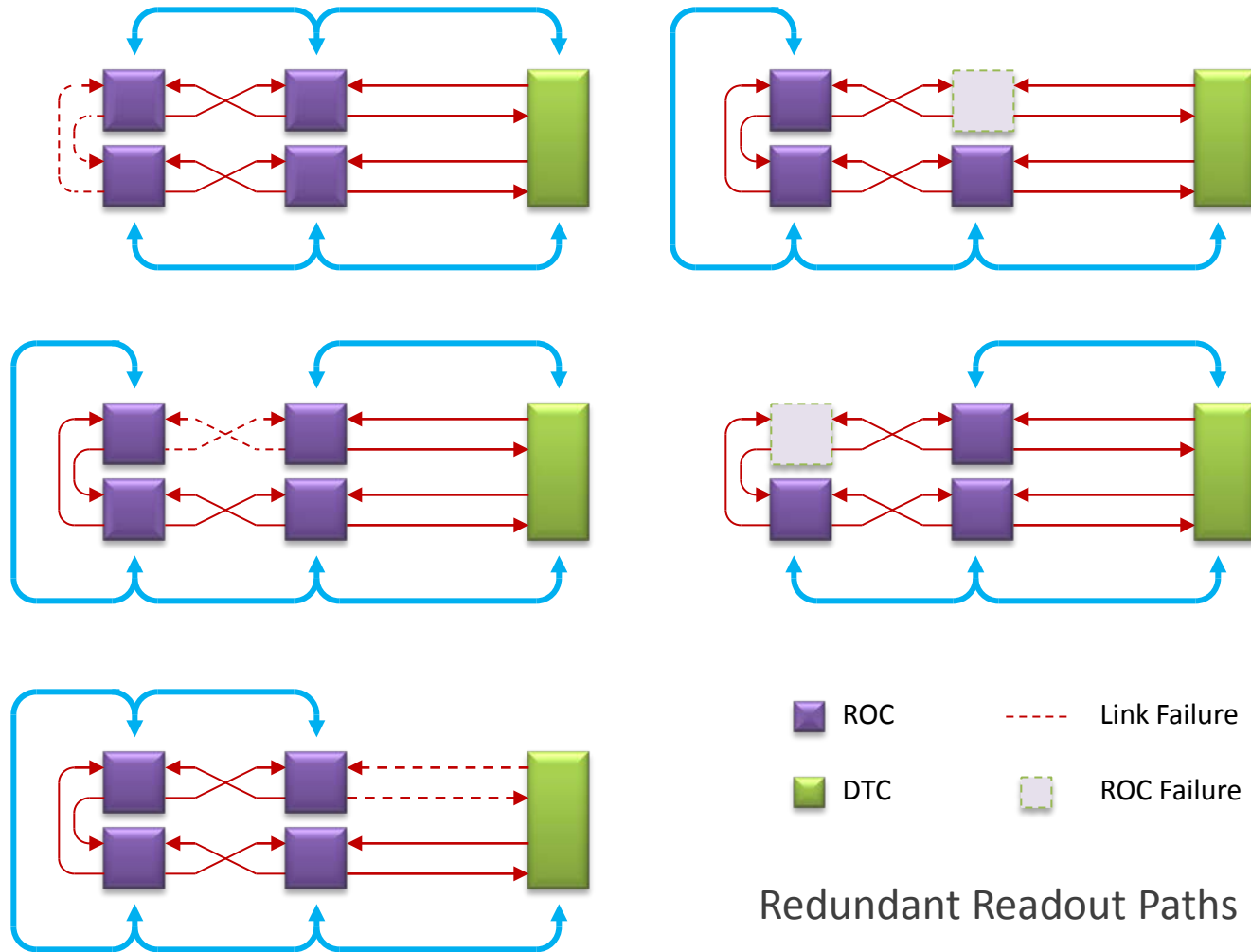
3 DAQ Servers
5 ROCs/Server

ROCs

DAQ Server

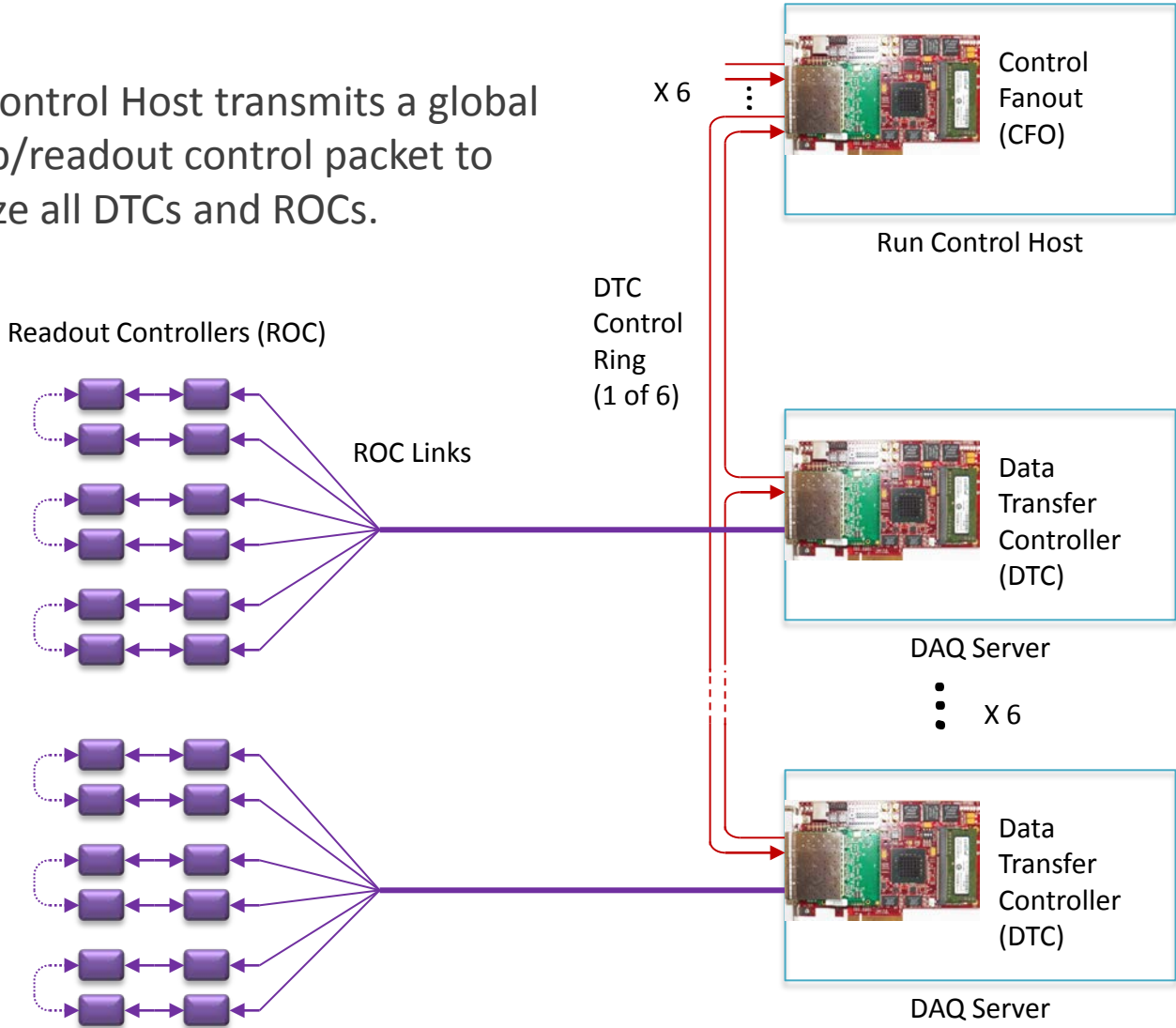
- 36 DAQ Servers
- 216 optical data Links
- Multiple Readout Controllers per link to balance load
- 240 Tracker ROCs (2 per link)
- 240 Calorimeter ROCs (3 or 4 per link)
- 15 CRV ROCs (1 per link)
- Links are bidirectional (control & data)
- Redundant paths to mitigate any single-point failure

System Design & Test

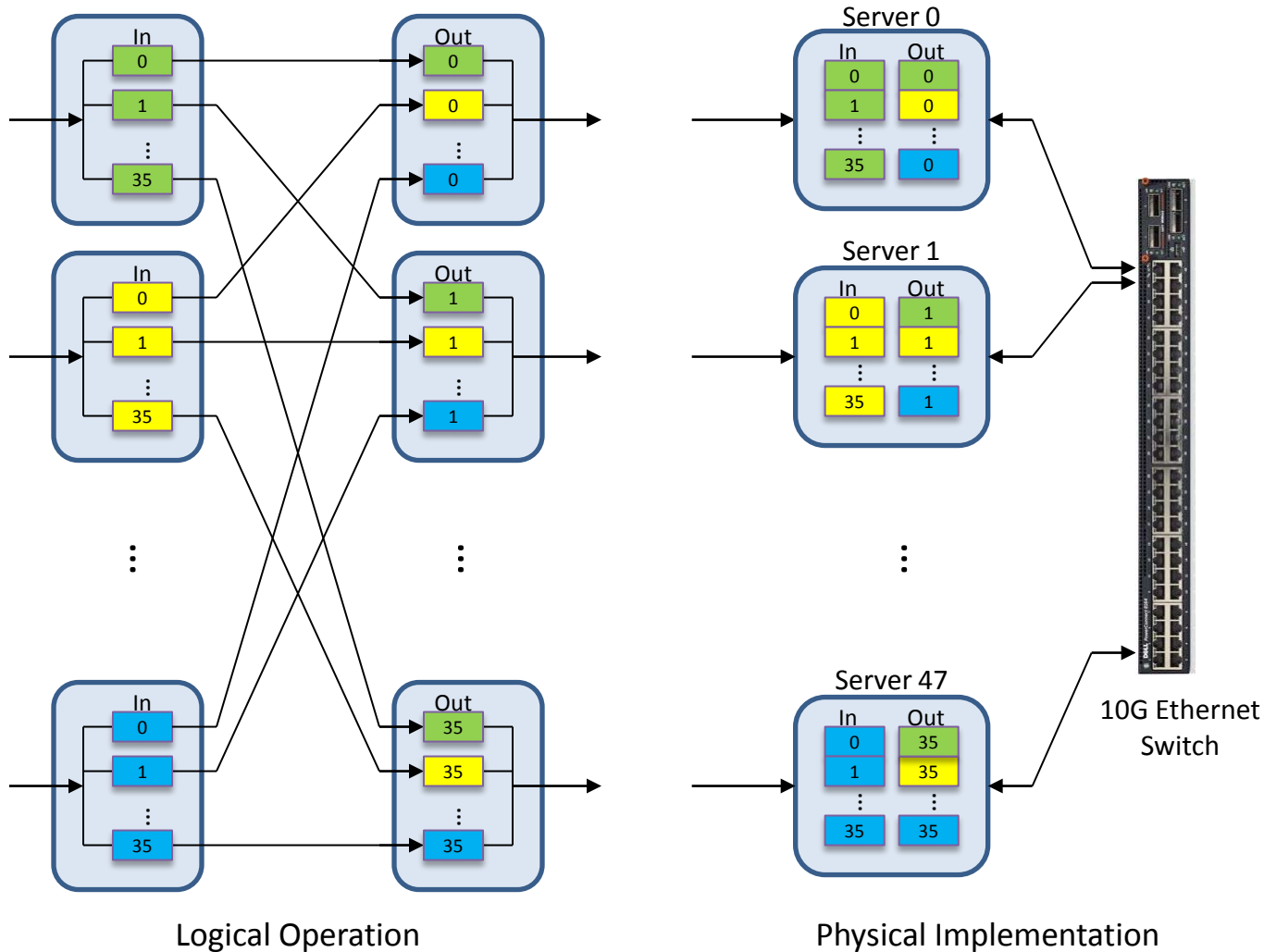


System Design & Test

The Run Control Host transmits a global timestamp/readout control packet to synchronize all DTCs and ROCs.



System Design & Test



The Event Building (EVB) function is performed by the DAQ Servers over a 10G Ethernet network.

Mu2e uses a folded network which reduces switch size and allows all EVB buffering to be done in server memory.

Data Acquisition

Data Acquisition

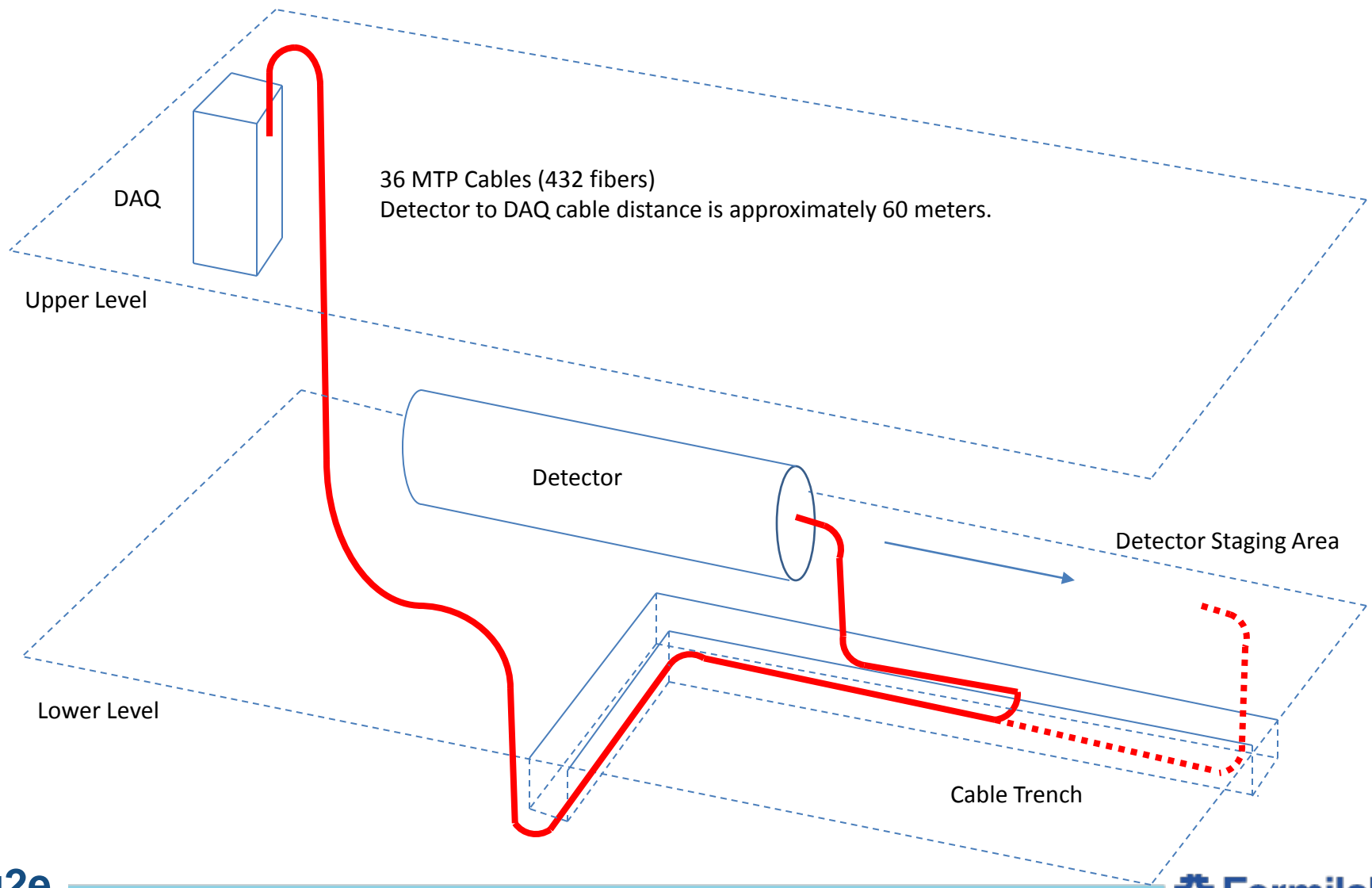


Commercial (off-the-shelf) hardware

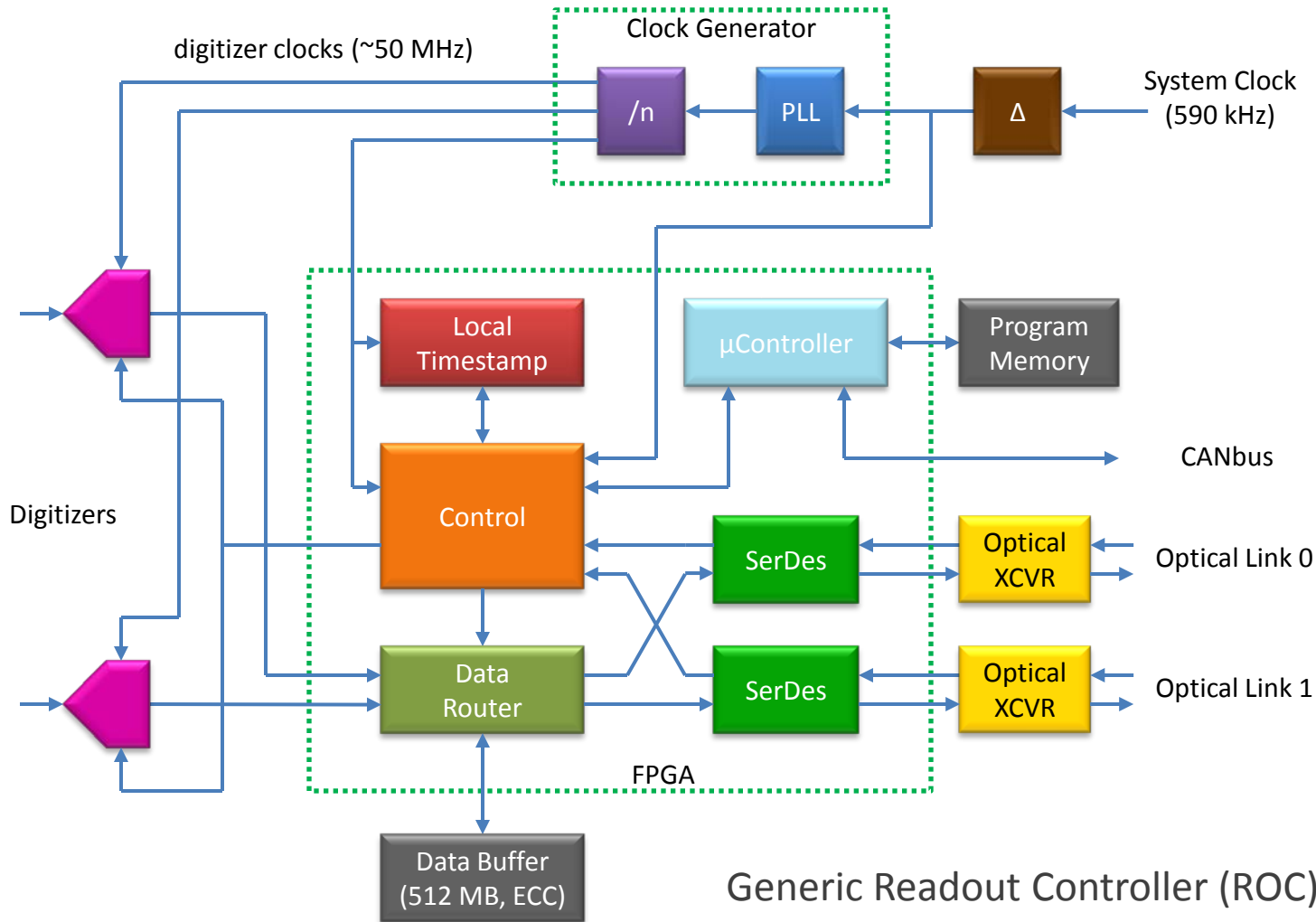
- DAQ server
 - 3U rack-mount computer
 - integrated DAQ and online processing
- Data Transfer Controller (DTC)
 - PCIe card with FPGA, memory, and an 8-port SFP+ optical interface
 - 1 GByte/sec readout bandwidth
- Event Building network
 - 48 port 10G Ethernet switch



Data Acquisition

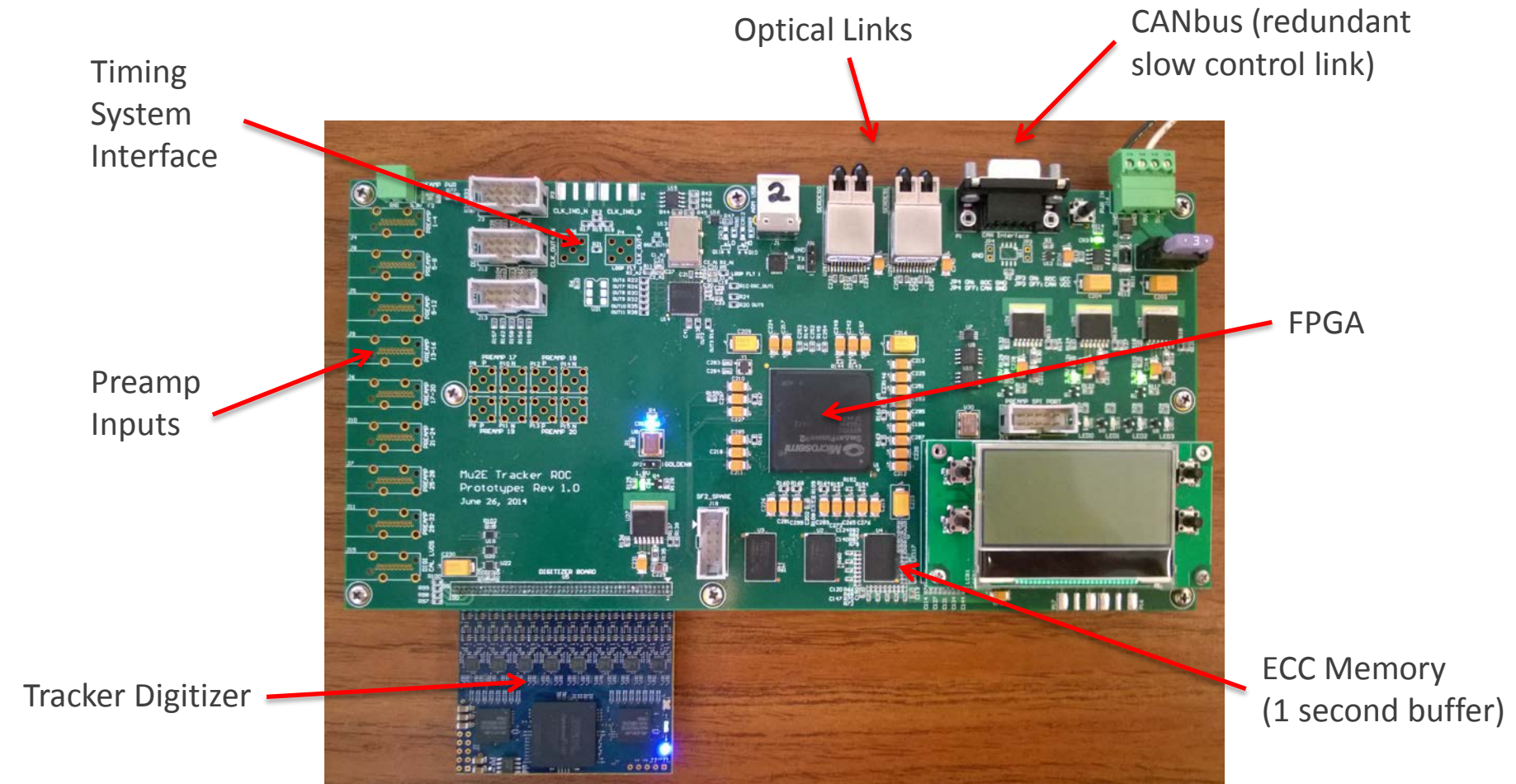


Data Acquisition



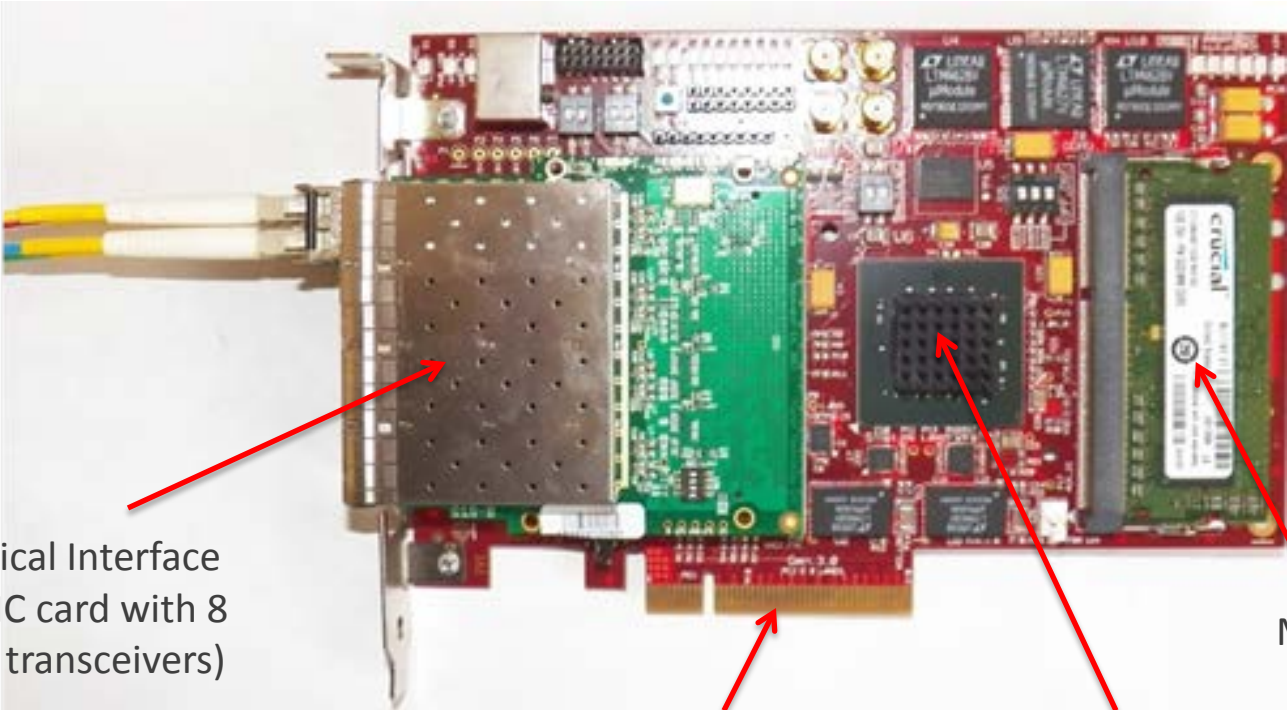
Generic Readout Controller (ROC) Architecture

Data Acquisition



Tracker Readout Controller (ROC) Prototype

Data Acquisition



Optical Interface
(FMC card with 8
SFP transceivers)

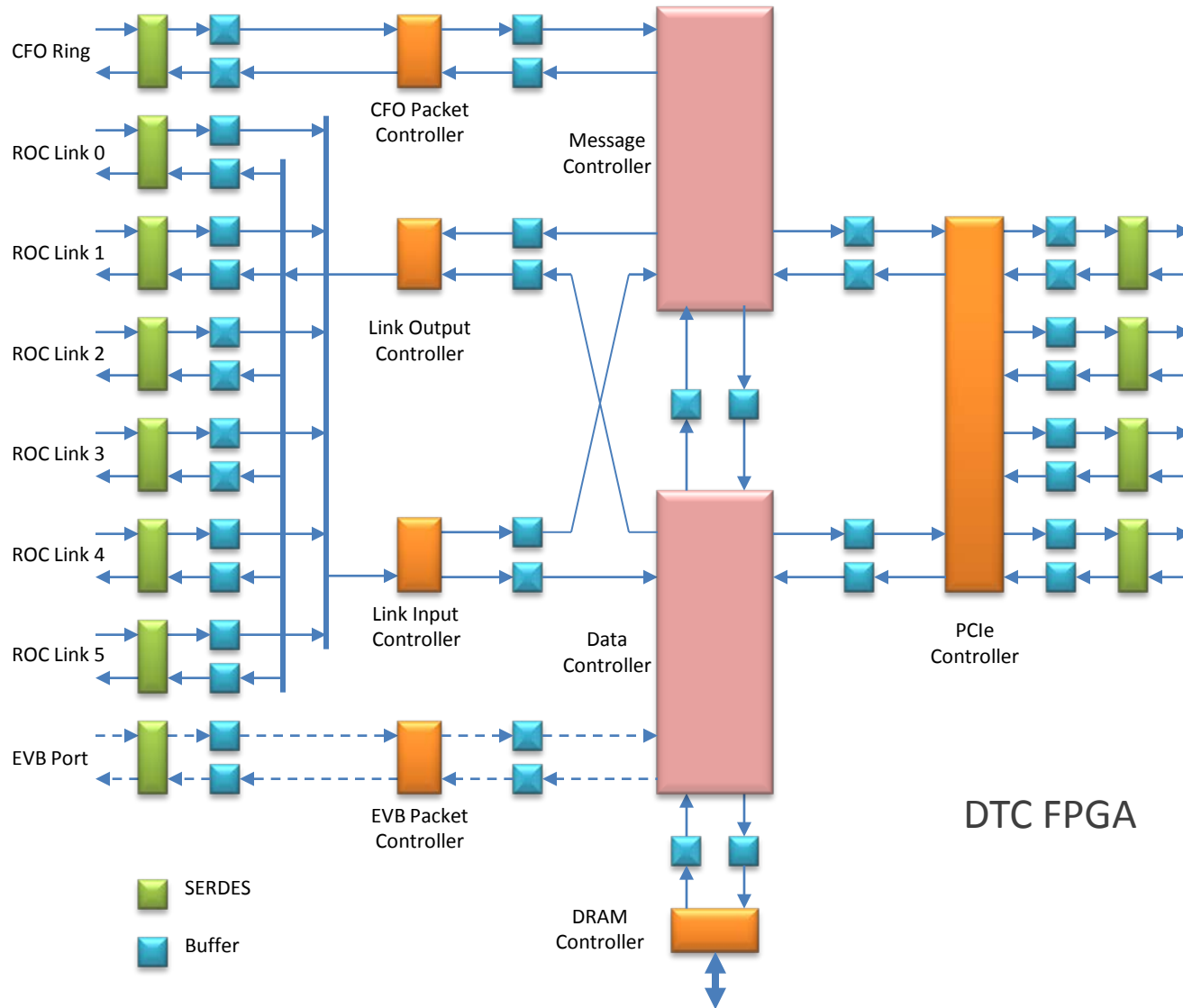
PCIe Interface

FPGA

Memory

Data Transfer Controller (DTC)

Data Acquisition



Data Acquisition

The screenshot shows the Xilinx Performance & Status Monitor interface for a Kintex-7 Base TRD. The interface is divided into several sections:

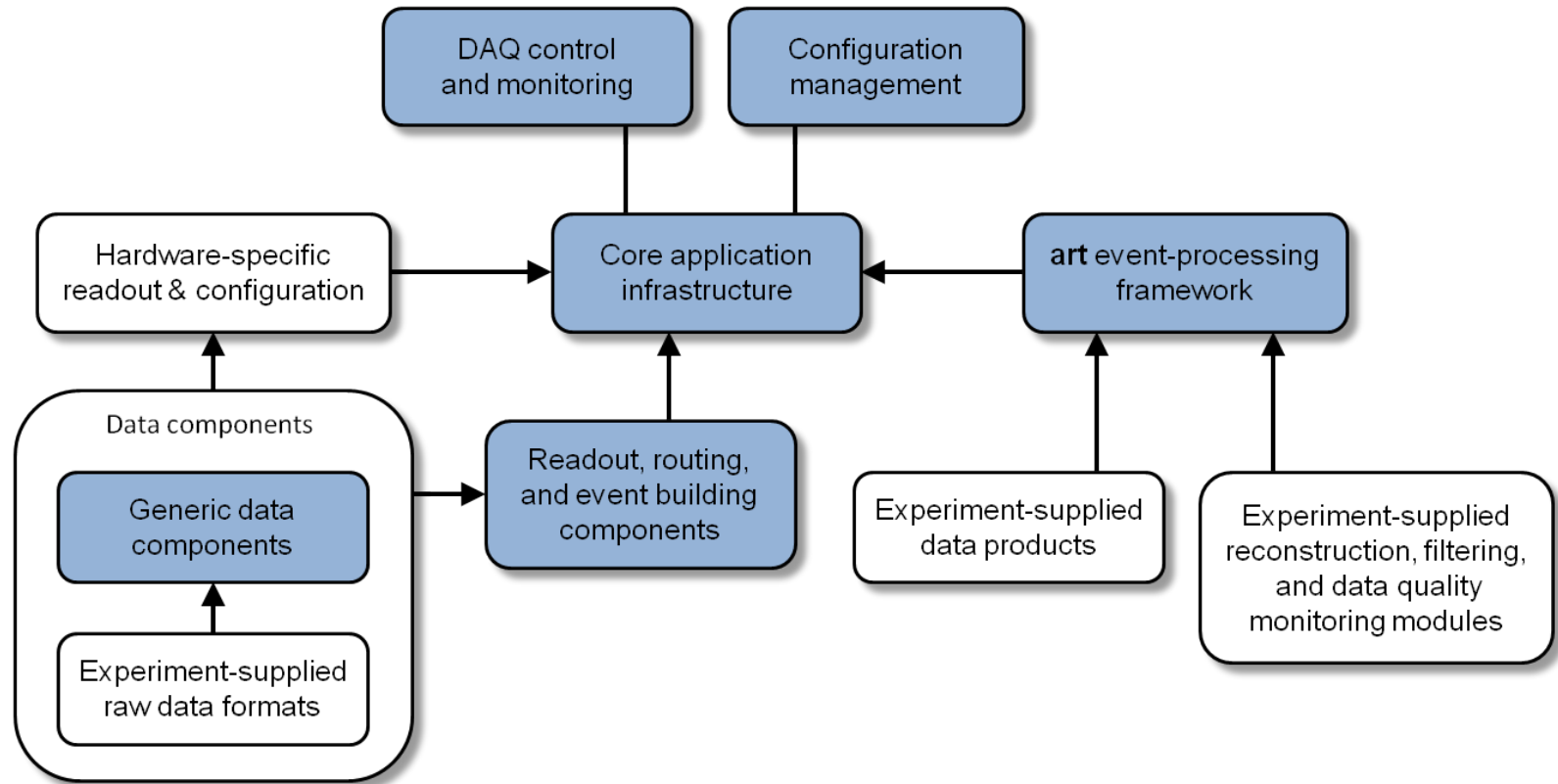
- Raw Data Path0:** Includes checkboxes for "Enable TX->RX Loopback" (checked), "Enable TX Checker" (unchecked), and "Enable RX Generator" (unchecked). A "Packet Size" field is set to 32768, and a "Stop Test" button is present.
- Raw Data Path1:** Similar to Path0, with "Enable TX->RX Loopback" checked and other options unchecked. Packet size is also 32768.
- System Status:** The active tab, showing DMA & Software Status and PCIe Statistics.
- DMA & Software Status:** Contains two tables for Path0 and Path1. Path0 shows a throughput of 5.168 Gbps (Transmit) and 5.122 Gbps (Receive). Path1 shows a throughput of 5.046 Gbps (Transmit) and 5.055 Gbps (Receive). Both paths have DMA Active Time of 1000000000 ns and DMA Wait Time of approximately 300 ns. BD Errors and Short Errors are zero. # SW BDs is 3999 and # SW Buffers is 4000. "Interrupts Enabled" is unchecked.
- PCIe Statistics:** Shows "PCIe Transmit (writes) (Gbps)" at 11.361 and "PCIe Receive (reads) (Gbps)" at 11.164, which are circled in red. Below this is the "PCIe Endpoint Status" table.
- Host System's Initial Flow Control Credits:** Shows Posted Header (56), Non-Posted Header (62), Completion Header (0), Posted Data (276), Non-Posted Data (8), and Completion Data (0).
- Log:** At the bottom, it shows "[INFO] Kintex-7 Base TRD v1.5", "[INFO] Test Started", and "[INFO] Test Started".

DTC Bandwidth Tests (PCIe x4, gen2, 1 GByte/sec transmit and receive)

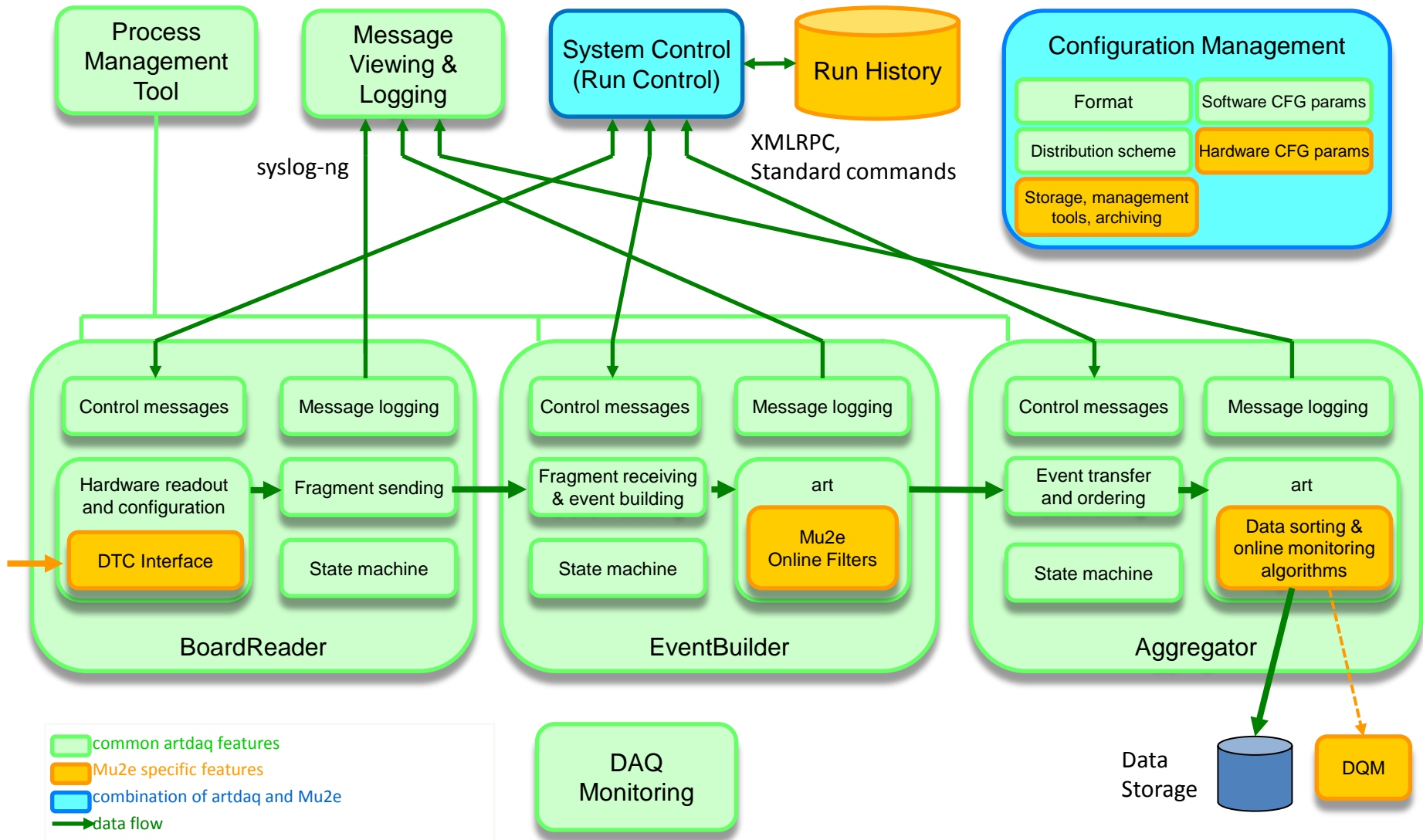
Data Acquisition

Software based on *art* and *artdaq*

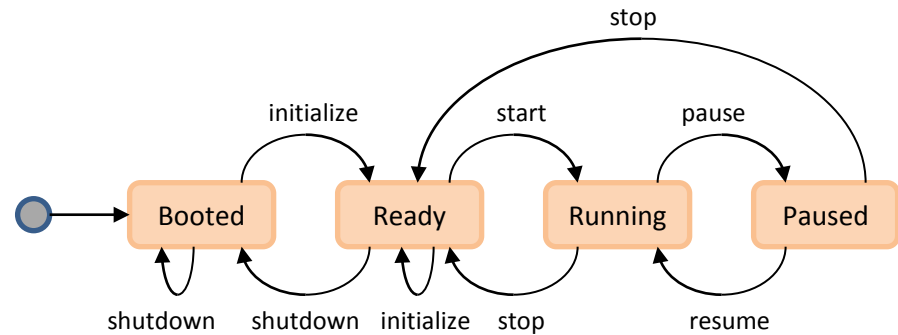
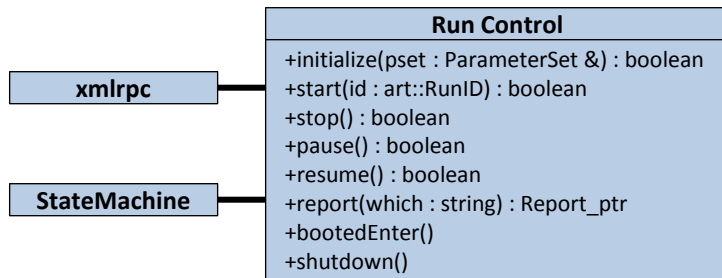
(a common DAQ & Online Processing framework developed for Mu2e and other current/future experiments)



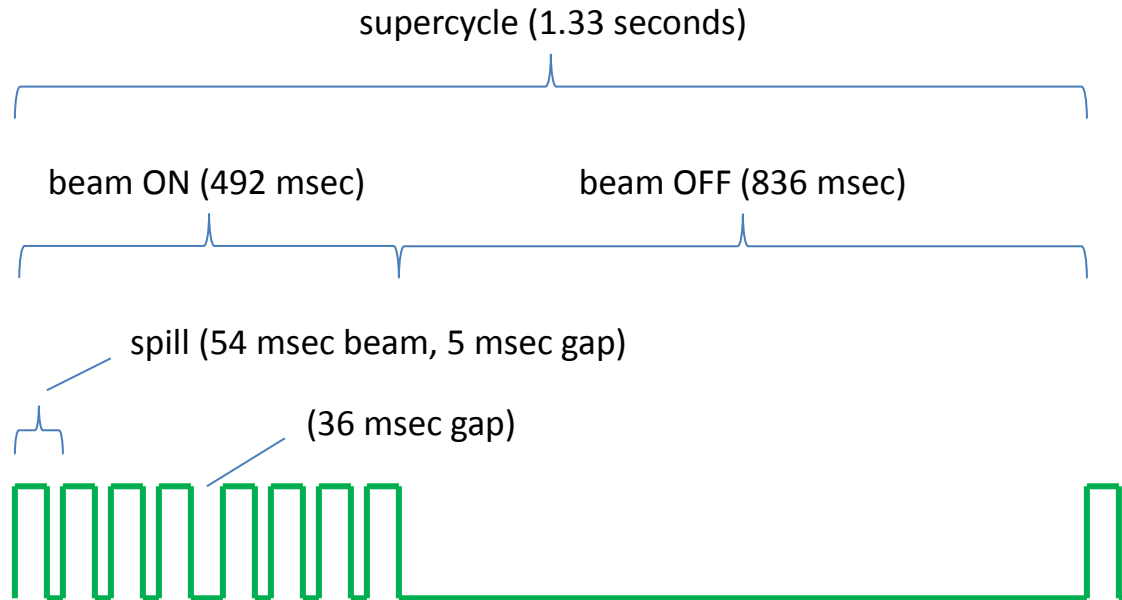
Data Acquisition



Data Acquisition



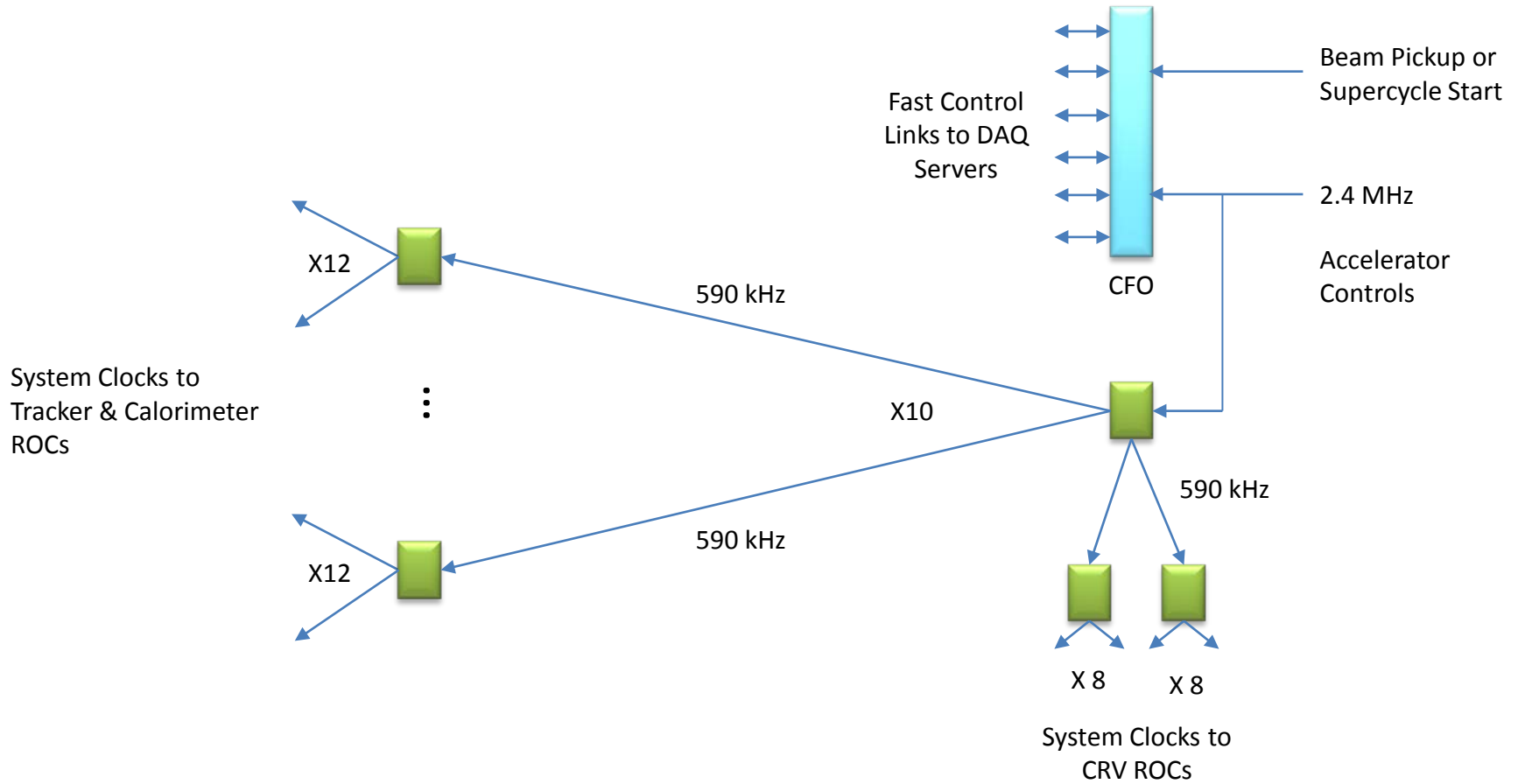
Data Acquisition



Readout Controllers capture data during the 492 msec beam ON period and transmit data to the DAQ over the full 1.33 second supercycle.

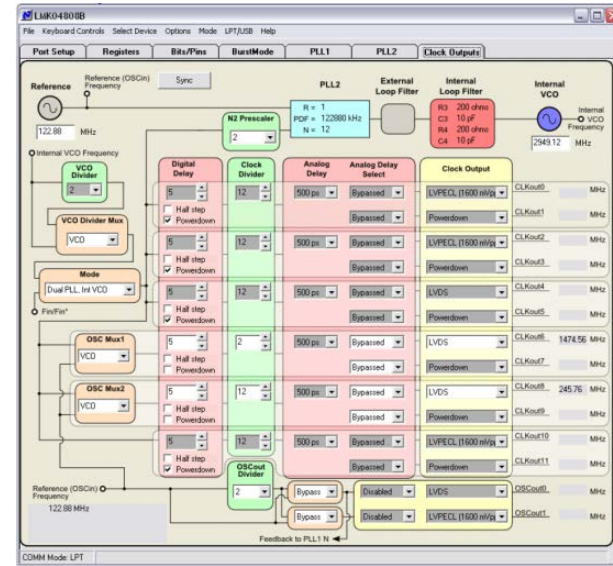
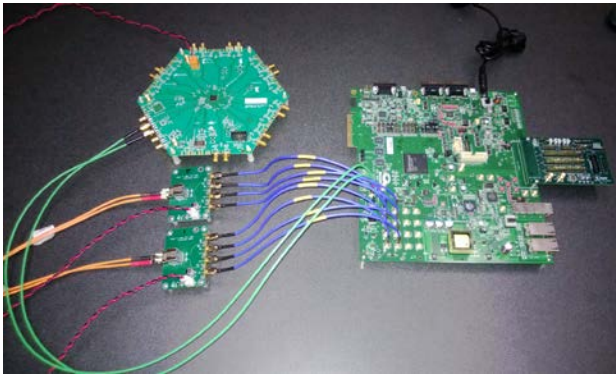
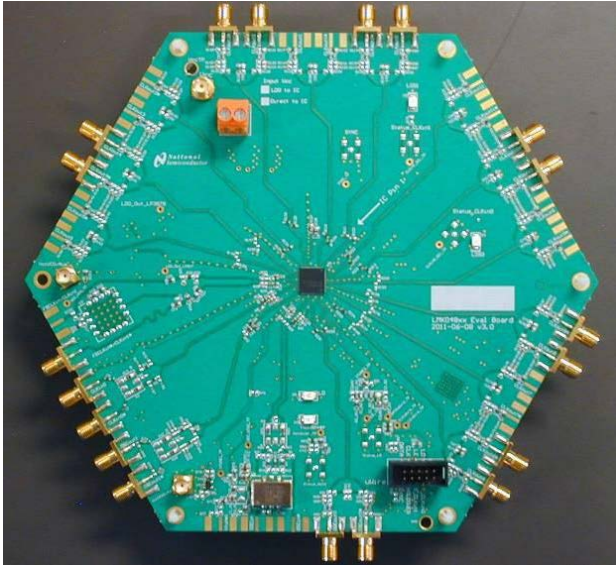
Beam Structure

Data Acquisition



System Clock Fanout

Data Acquisition



- clock generator on ROC provides final System Clock alignment and acquisition clock multiplier
- clock phase alignment is programmable in 25 psec steps

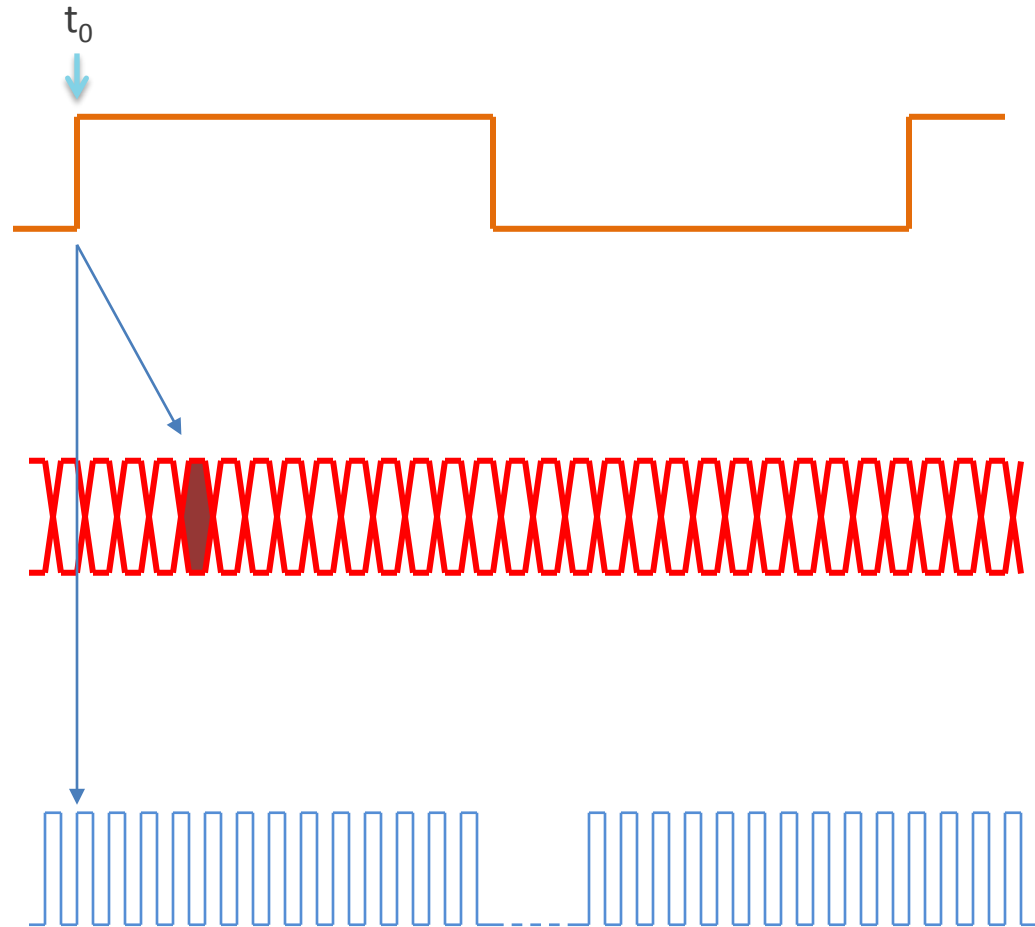
Timing System

Data Acquisition

System Clock - 1695 ns (590 KHz), phase-locked to accelerator. Leading edge of System clock is t-zero reference for Readout Controller Internal Timestamp counters.

Control/Data Link - 2.5 Gbps (DAQ \leftrightarrow Readout Controllers). A control packet is sent for each System Clock period to specify Readout Controller operation during the next System Clock (μ Bunch). The control packet includes the μ Bunch Timestamp.

Readout Controller acquisition clocks - \sim 50 MHz (varies with detector), phase-locked to System Clock, drives Readout Controller Internal Timestamp counter and ADCs/TDCs.



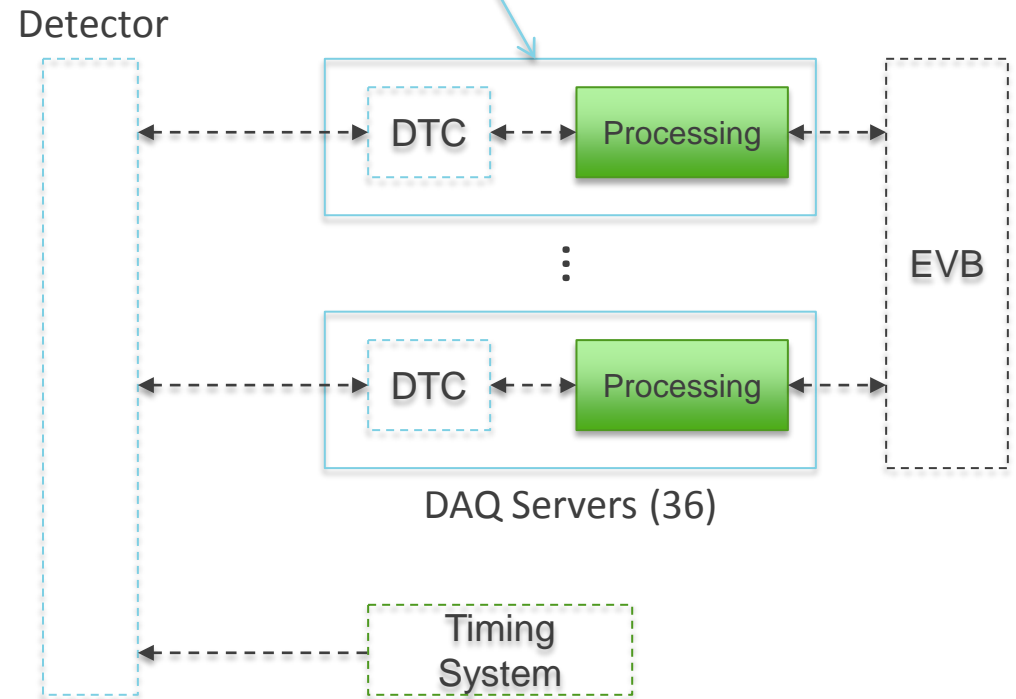
Timing System

Data Processing

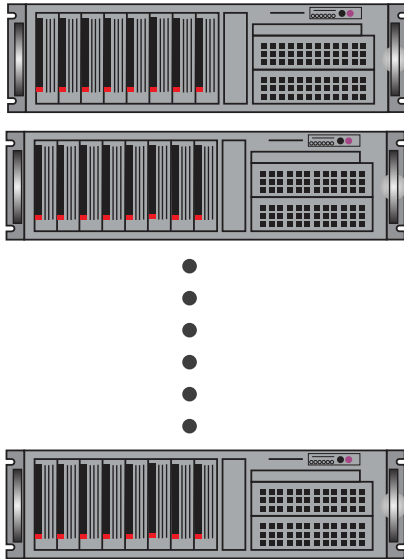
Data Processing

Scope

- DAQ Servers
- Data Logger, DCS Host & Run Control Host
- Data Processing software running on DAQ Servers
- Online data filters and analysis



Data Processing



DAQ Servers

- 36 DAQ Servers
- 192k events/sec
- using XEON-PHI processor
64 cores X 36 servers → 2,304 total cores
Available processing time/event: 12 ms
- using dual XEON processors
20 cores X 36 servers → 720 total cores
Available processing time/event: 3.75 ms



Processing Requirements

Data Processing

Several algorithmic and compiler optimizations were applied to the reference Tracking filter to achieve a speedup of almost 30X.

Optimization stage for MakeStereoHits	Compiler	Execution Time (ms)	
		Xeon (speedup)	Xeon Phi (speedup)
Reference	gcc 4.4.7	132	-
Modified algorithm	gcc 4.4.7	6.67 (19.8x)	-
Modified algorithm	icc 14.0.1	2.04 (3.33x)	-
Additional optimizations	icc 14.0.1	1.88 (1.08x)	30.4

Optimization stage for FlagBkgHits	Compiler	Execution Time (ms)	
		Xeon (speedup)	Xeon Phi (speedup)
Reference	gcc 4.4.7	14.2	-
Reference	icc 14.0.1	8.03 (1.77x)	123
Optimizations (mem align/layout)	icc 14.0.1	5.01 (1.60x)	37.7 (3.26x)
Optimizations (single precision)	icc 14.0.1	3.37 (1.49x)	24 (1.57x)

Note : Speedup factors in parentheses are relative to previous stage

Data Processing

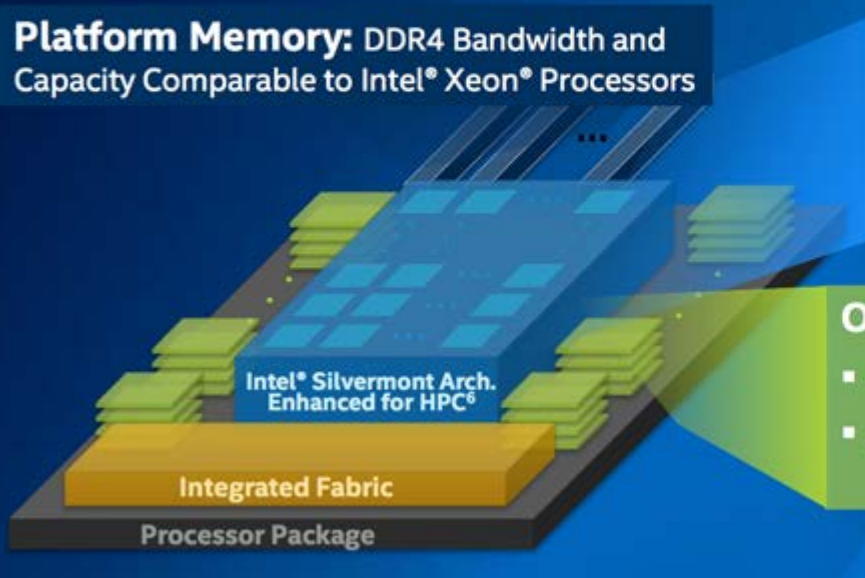
Trigger stage	Execution time (ms)	Scaled times (ms)
MakeStereoHits	1.88	1.18
FlagStrawHits	0.12	0.07
FlagBkgHits	3.37	2.12
TrkPatRec	0.71	0.45
TriggerResults	0.03	0.02
Total	6.11	3.84

Execution times were measured on a XEON E5-2630 and scaled for the E5-2687w.

Estimate of 3.84 ms/event using current generation processors is very close to the requirement of 3.75 ms/event (not including overheads). We expect an additional 2-3X improvement in processing performance between now and server purchases in 2018.

Data Processing

- Near-term processing roadmap (XEON PHI)
 - 3X performance over 5110P



The diagram shows a 3D perspective of the Intel Knights Landing processor package. At the base is the 'Processor Package' (dark grey). Above it is the 'Integrated Fabric' (orange). The top layer is the 'Intel® Silvermont Arch. Enhanced for HPC⁶' (blue), which is connected to multiple layers of 'On-Package Memory' (green) on both sides. The overall structure is a dense, multi-layered stack.

3+ TFLOPS¹
In One Package
Parallel Performance & Density

New for Knights Landing

(Next Generation Intel® Xeon Phi™ Products)

★ **2nd half '15**
1st commercial systems

Platform Memory: DDR4 Bandwidth and Capacity Comparable to Intel® Xeon® Processors

Compute: Intel® Silvermont Arch. (Intel® Atom™)²

- Low-Power Cores with HPC Enhancements³
- **3X** Single Thread Performance⁴ vs Prior Gen.
- Intel Xeon Processor Binary Compatible⁵

On-Package Memory: High Performance

- up to **16GB** at launch
- **1/3X** the Space⁶
- **5X** Bandwidth vs DDR4⁷
- **5X** Power Efficiency⁶

Jointly Developed with Micron Technology

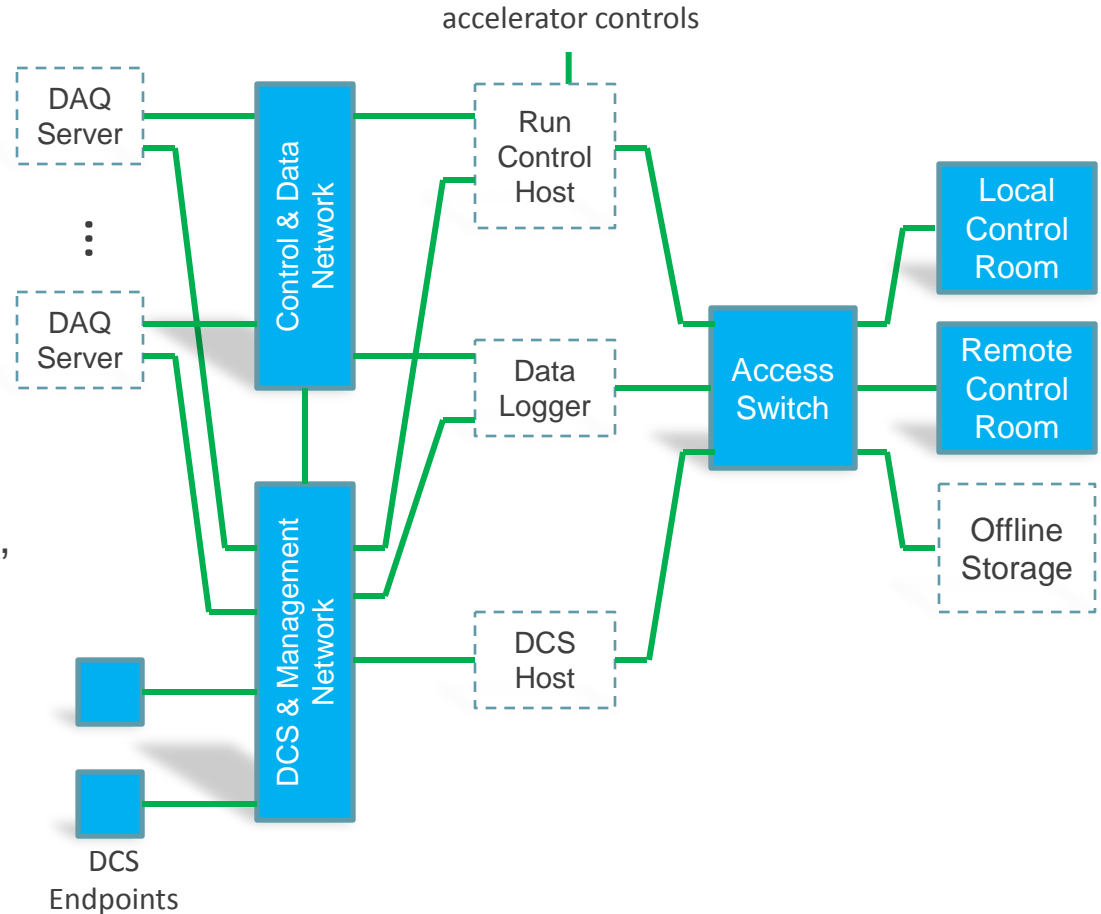
LEARN MORE: Knights Landing Webcast (Tuesday June 24th):
<https://www.brighttalk.com/webcast/10773/116329>

Controls & Networking

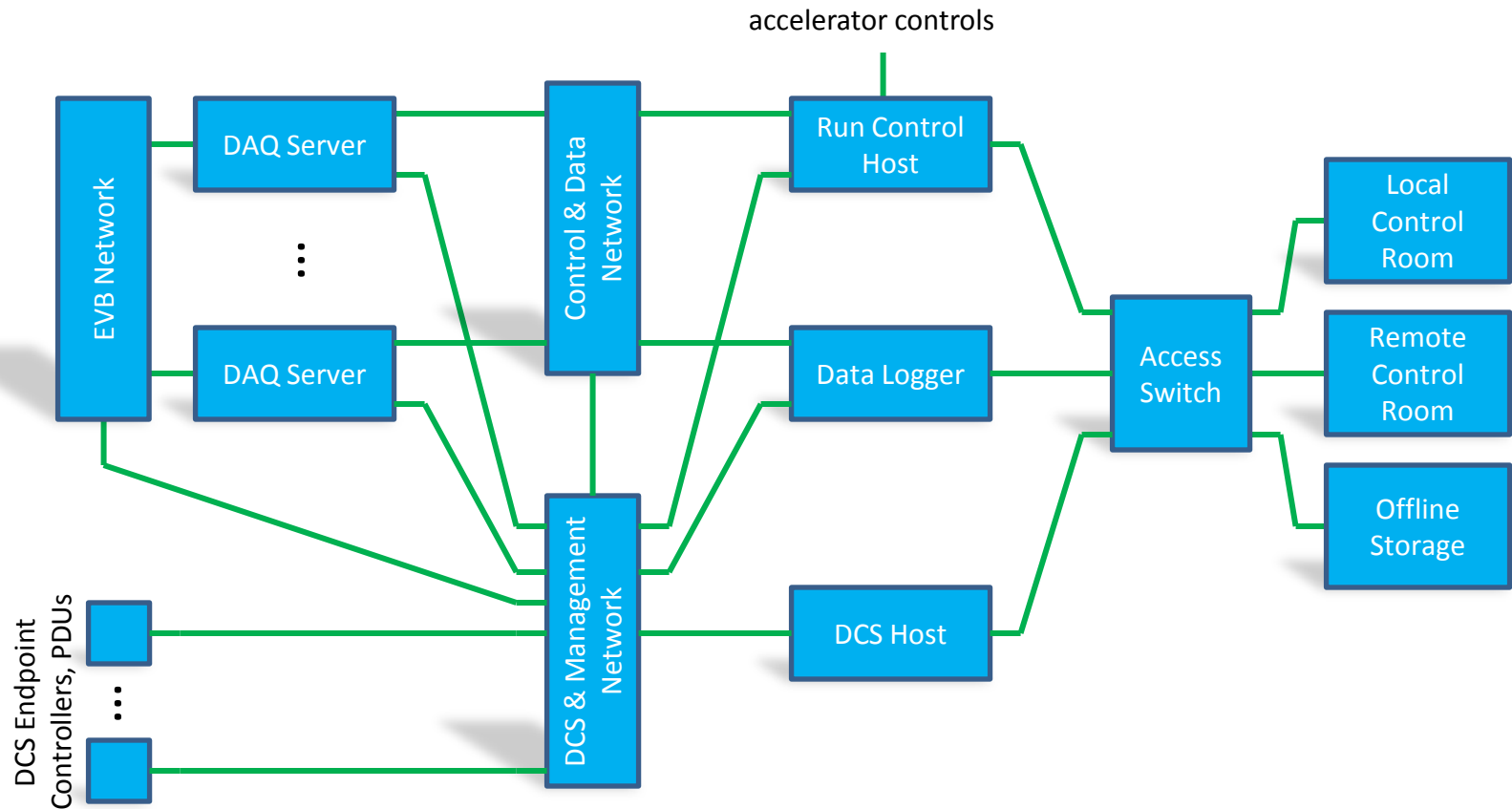
Controls & Networking

Scope

- Control Room
- General-purpose Networking
- Detector Control System (DCS) (lower speed data acquisition and control for environmental data, power supplies, accelerator status, etc)

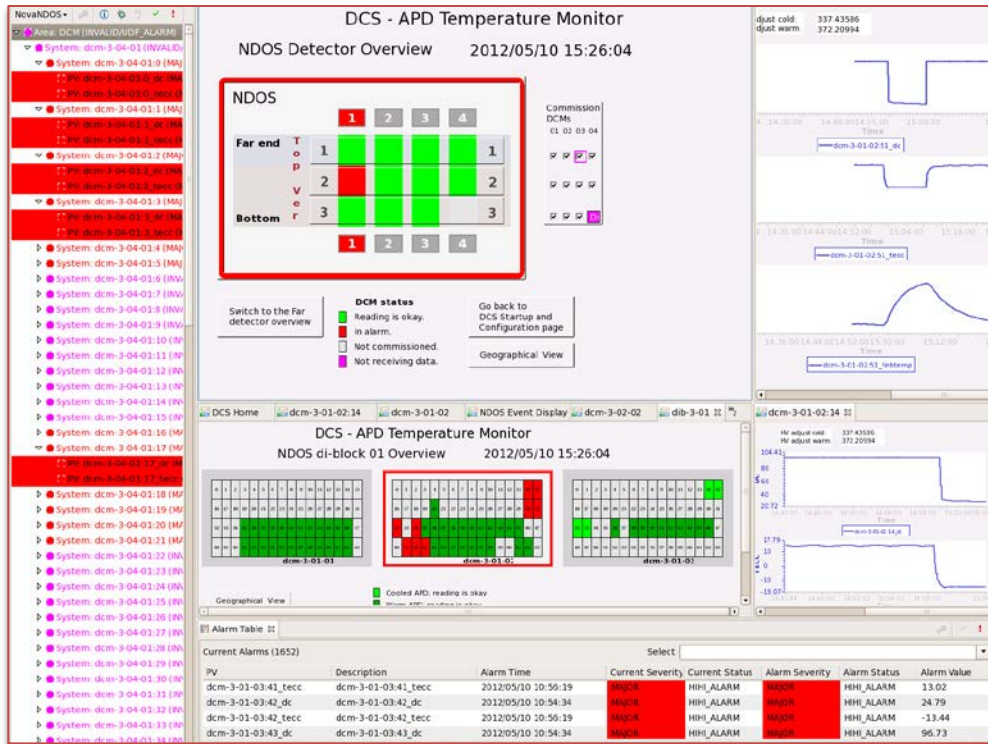


Controls & Networking



System Architecture - Networking Perspective

Controls & Networking



The Detector Control System (DCS) software will incorporate development work done for NOvA, along with current web based interface technology.

Screenshot from EPICS/CSS based DCS used in NOvA.

Controls & Networking



Mu2e Remote Control Room - Wilson Hall, 1st floor West
(shared use - LBNF, MicroBooNE, MINERvA, MiniBooNE, MINOS, Muon g-2, Mu2e, NOvA)

Summary

- Based on initial testing of DAQ components, we are confident that the system bandwidth and processing will meet requirements.
- Currently in the Pilot System development phase, expected to take approximately 1 year.
- Pilot phase goal is a small (6 server) functioning DAQ system, with the basic features necessary to communicate with detector readout controllers, buffer and exchange event data between servers, and measure online filter performance.
- 75% of effort is in firmware/software development. Estimates are based on a top-down approach using recent experiments of similar complexity.
- Costs are reduced through the use of commercial hardware and a common software framework.

Summary

- We have a design that fully satisfies the requirements
- Cost estimates for the DAQ are complete
 - 100% of the cost understood at the Preliminary Design level or higher
 - Risks are understood, mitigated to the extent possible and are under control.
- All interfaces are identified and defined
- Resource needs understood
- ES&H embedded into all aspects of the Project
- Responded to all recommendations from previous reviews
- DAQ is ready for CD-2