PURDUE UNIVERSITY CALUMET

CMS Compact Muon Solenoid

CERN

CMS Pixel Detector Upgrade

Xuan Chen

on behalf of the CMS FPIX Upgrade group

Senior, Physics Undergraduate Student

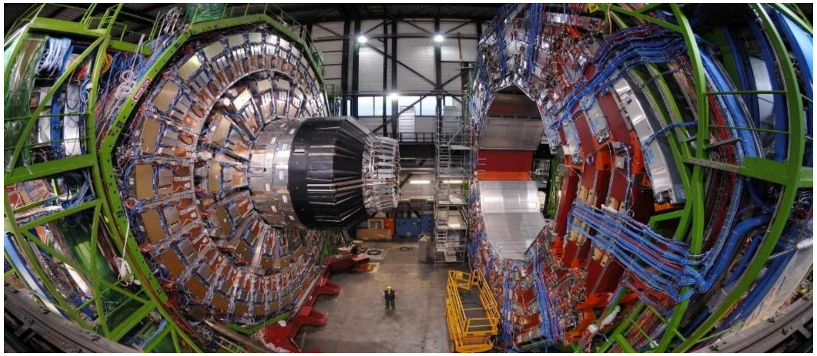
Advisors: Prof. Neeti Parashar, Dr. John Stupak III

photo by Michael.Hoch@cern.ch

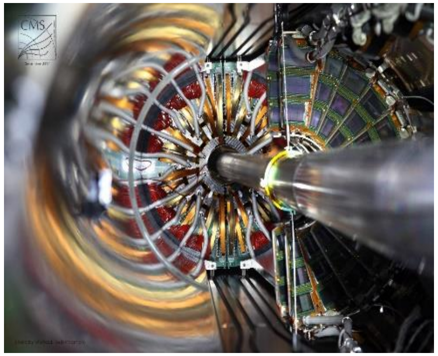
Outline

- The LHC
- The CMS detector
- The phase 0 pixel detector
- The phase 1 pixel detector upgrade

LHC



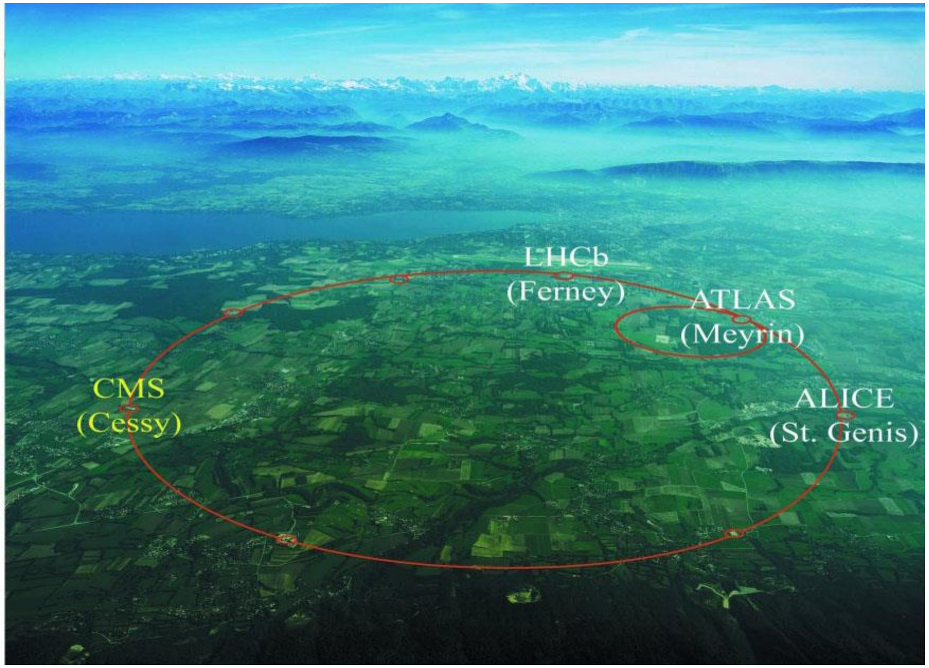
CMS



Pixel Detector

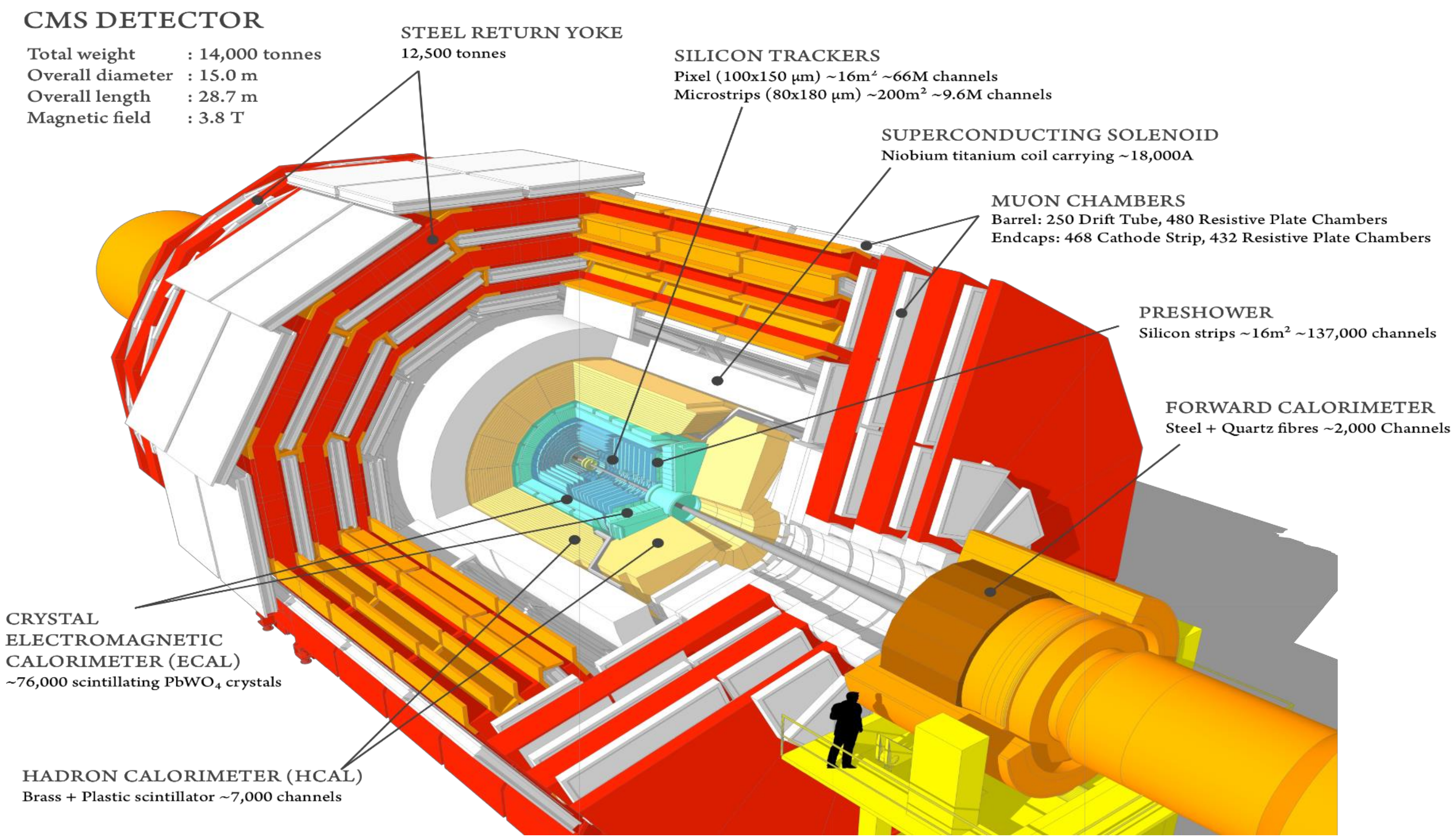
The Large Hadron Collider

- 17-mile circumference hadron collider across Switzerland and France
- Located at the European Organization for Nuclear Research (CERN)
- 14 Trillion electron-volt (TeV) proton-proton collision design energy
- Accelerates protons to 99.999999% the speed of light



- 4 state-of-the-art particle detectors: CMS, ATLAS, ALICE, LHCb
- Allows precision tests of the Standard Model of Particle Physics, and searches for the Higgs Boson and other New Physics beyond Standard Model

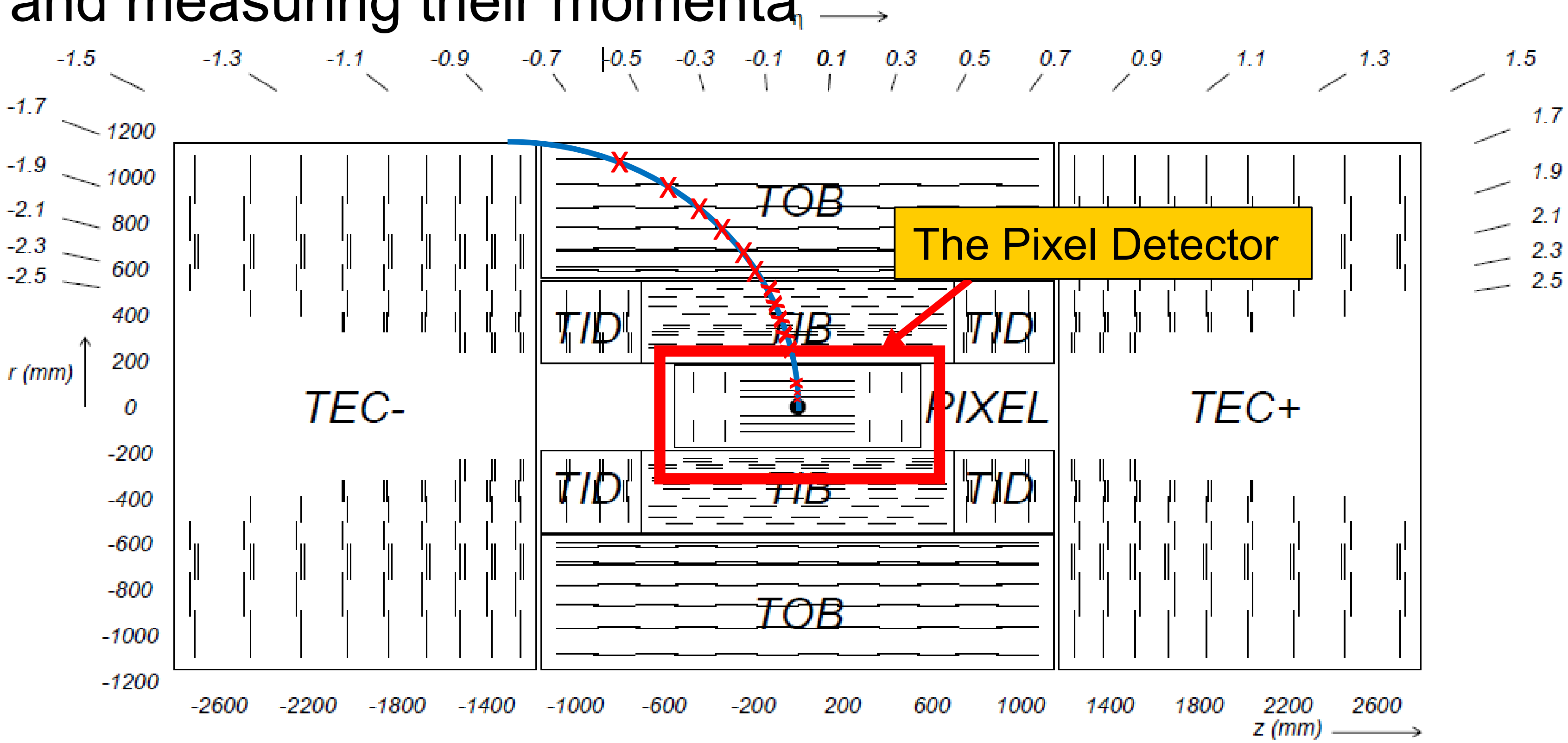
The Compact Muon Solenoid (CMS)



- General purpose, "onion-like" detector to study LHC collisions
- Designed for LHC luminosities of $10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ with 25 ns bunch spacing

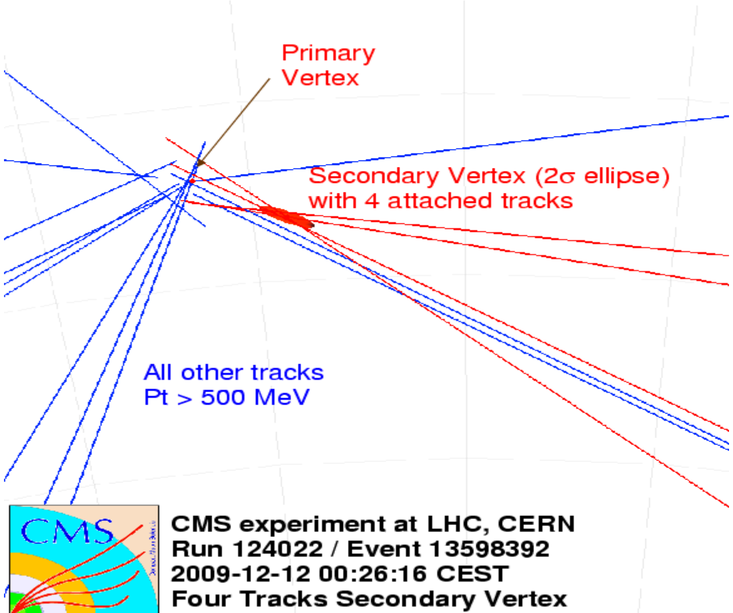
Silicon Tracker

- Responsible for recording the trajectory of charged particles and measuring their momenta

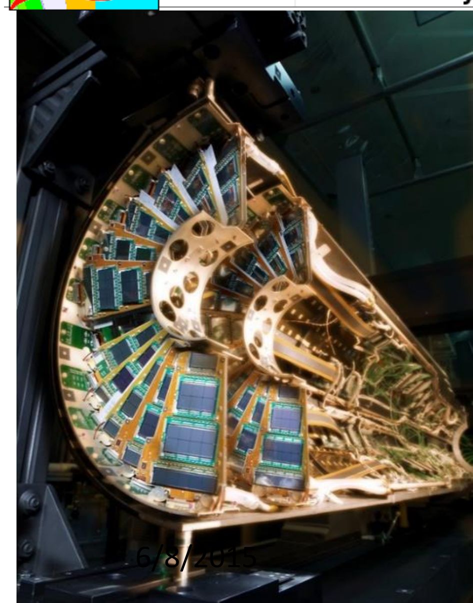


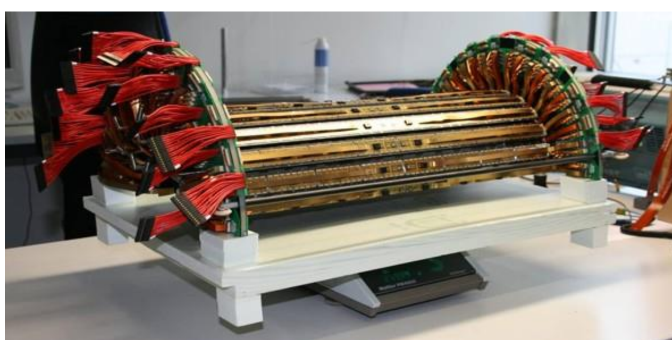
Pixel Detector:	▪ 3 Barrel Pixel Layers (BPIX), 2 x 2 Forward Pixel Disks (FPIX)
Si Strip Tracker:	▪ 4 Inner Barrel Layers (TIB), 6 Outer Layers (TOB)
	▪ 3 x 2 Forward Inner Disks (TID), 9 x 2 Outer Disks (TEC)

Current Pixel Detector – Phase 0



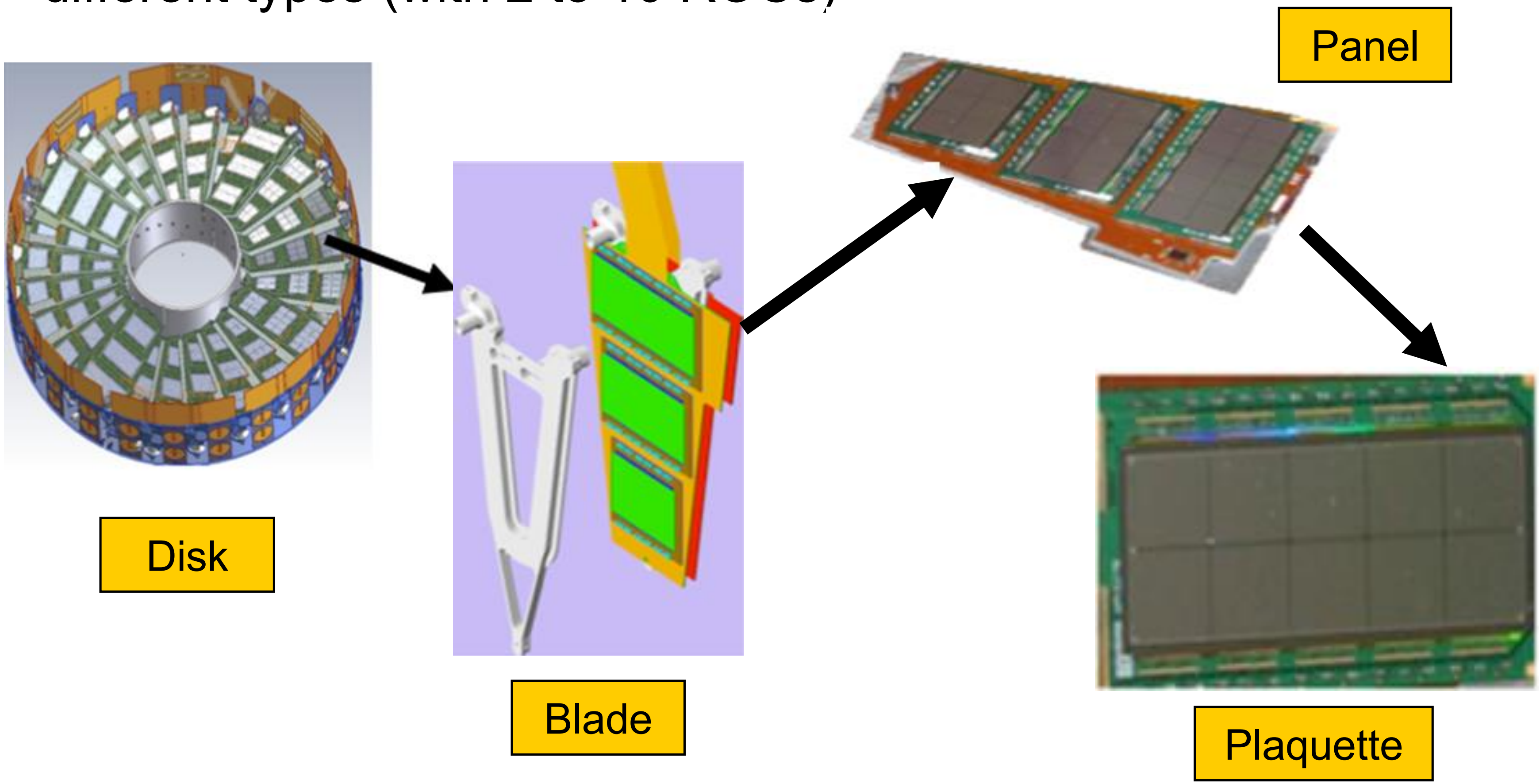
- The pixel detector is the closest detector to the interaction point
- Provides precise track and vertex reconstruction
- Integral part of the Tracker
- Made of silicon with 65 million pixels
- Pixels record the passage of charged particles
- Precise 3D position measurement
  - Each pixel is 100 μm by 150 μm
- Hit resolution of 10 μm
- 40 MHz analog readout



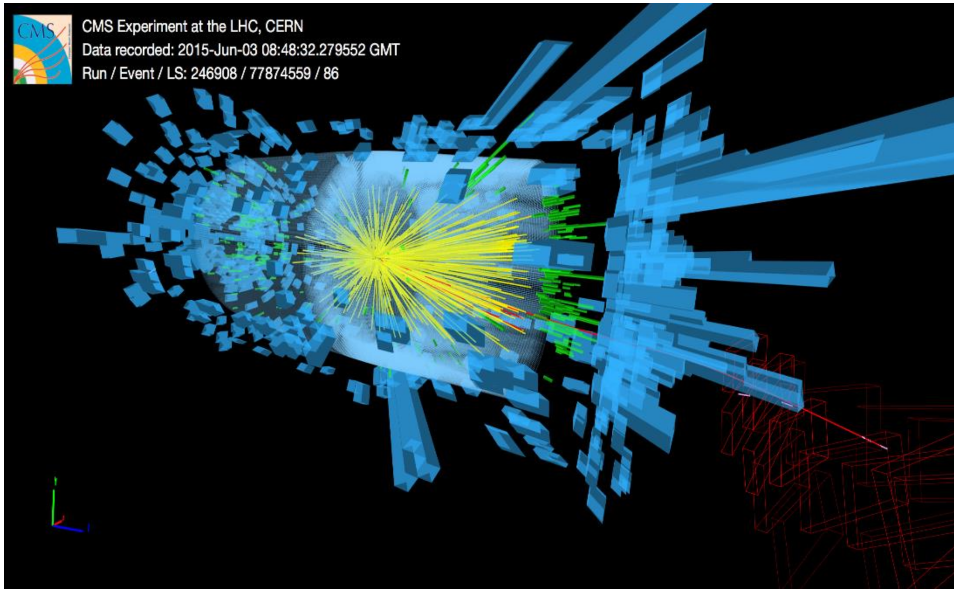


Phase 0 FPIX Detector

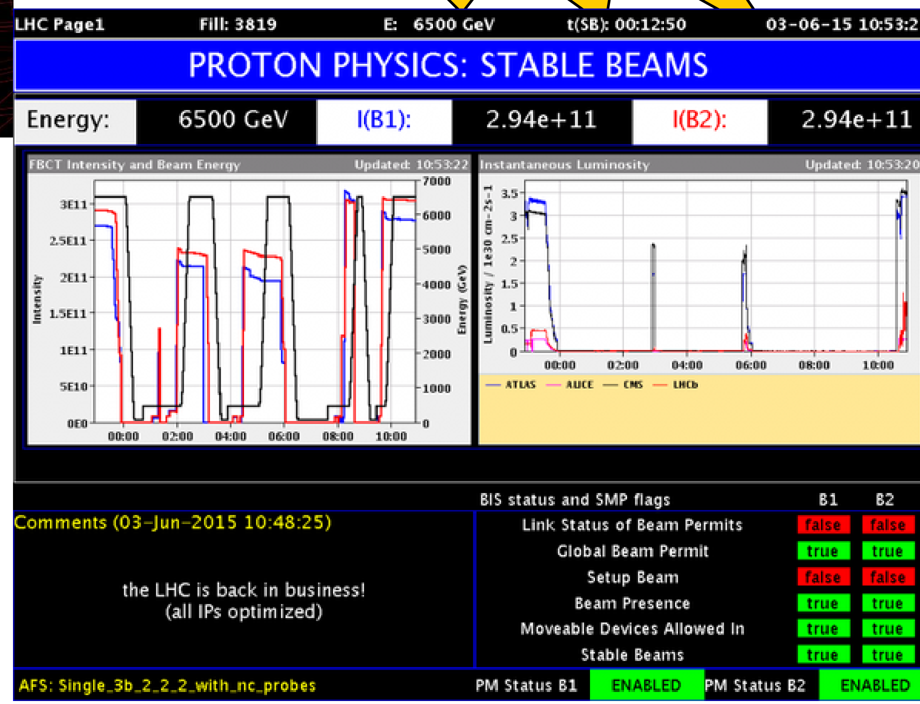
- 4 Forward/Endcap Disks (FPIX)
- Populated with 672 pixel modules (called plaquettes), with five different types (with 2 to 10 ROCs)



The LHC Run II

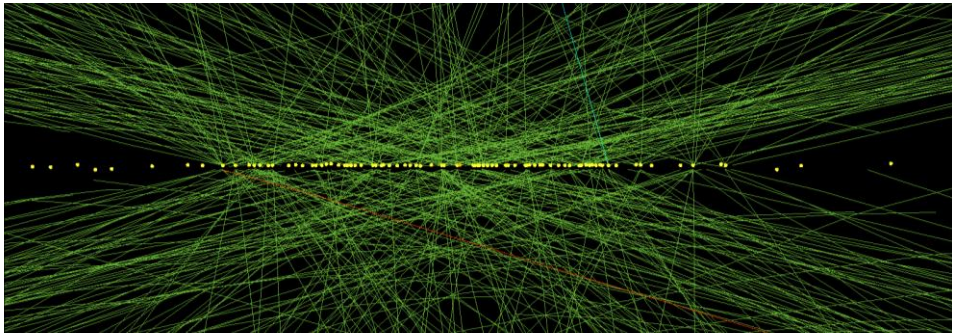


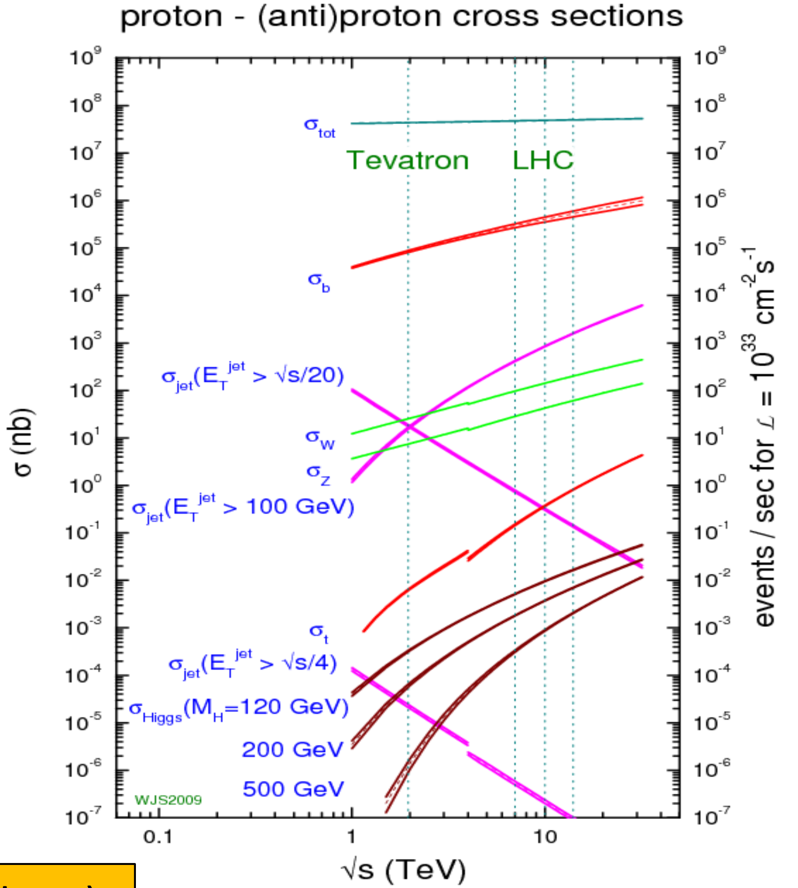
First Collision at 13 TeV!!!



The LHC Run II

- Increased energy and luminosity offer unique potential for historic discoveries
  - Precision Higgs physics
  - Additional Higgs bosons
  - Dark Matter
  - Extra spatial dimensions
  - SuperSymmetry
  - Etc…

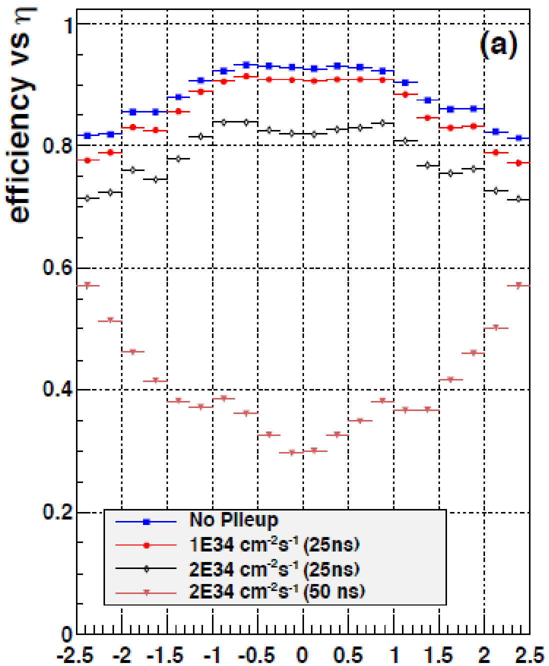


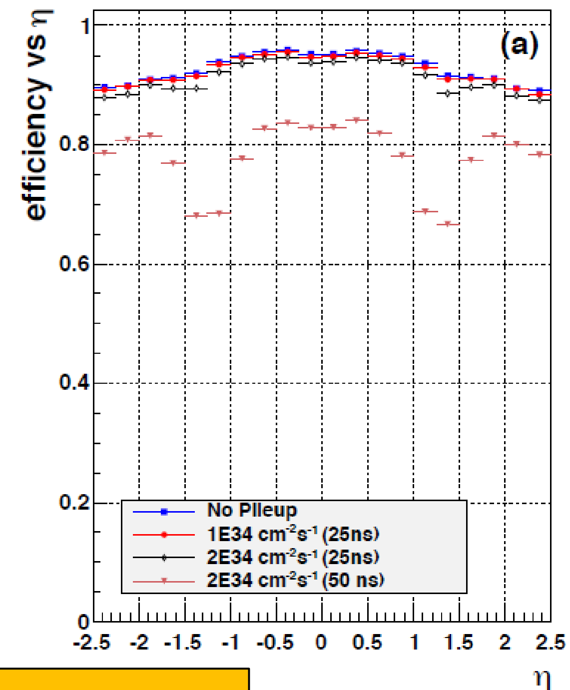


Many Simultaneous overlapping soft interactions (pileup)

Challenges

Current Detector





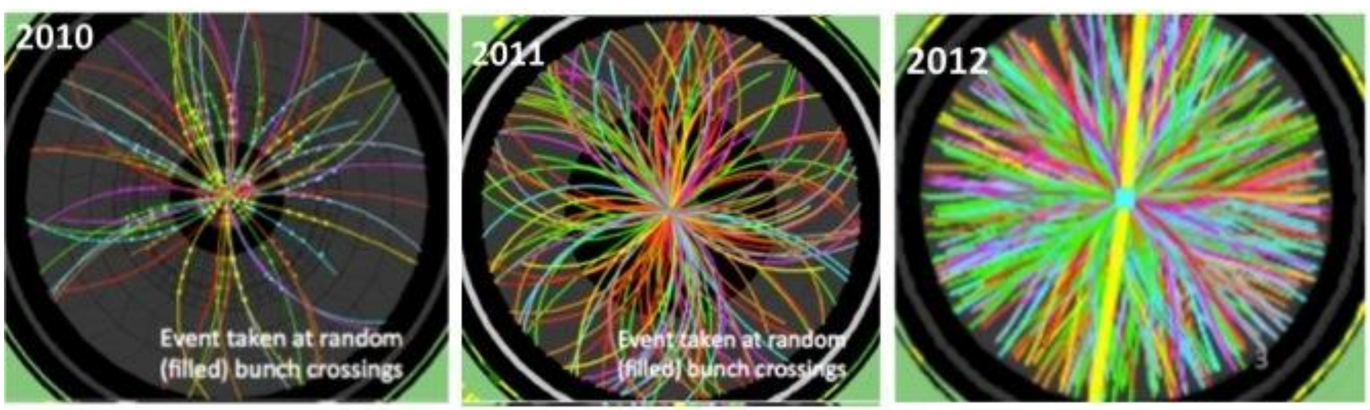
Upgrade Detector

Tracking Efficiency

- **High energy and luminosity brings new challenges**
  - Extreme pile-up conditions
  - High hit rate and data transfer requirements, which the current pixel detector can't satisfy

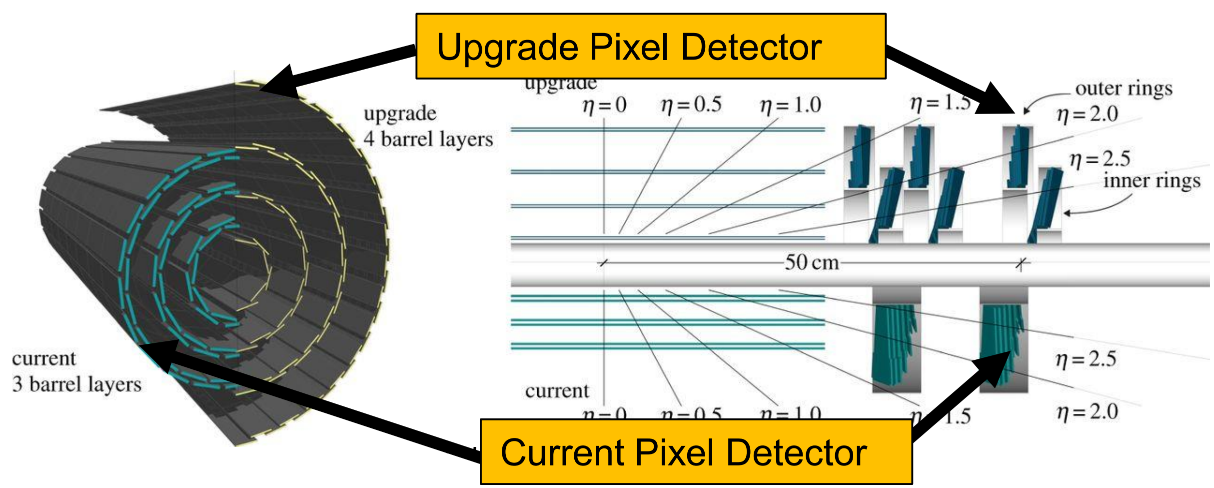
The Pixel Detector – Phase I Upgrade

- Maintain or improve current level of performance under extreme pile-up conditions
  - Sustain the high efficiencies and low fake rates of the current detector
  - Preserve hit resolution of current detector
- Improve radiation hardness
- Minimize data loss due to latencies

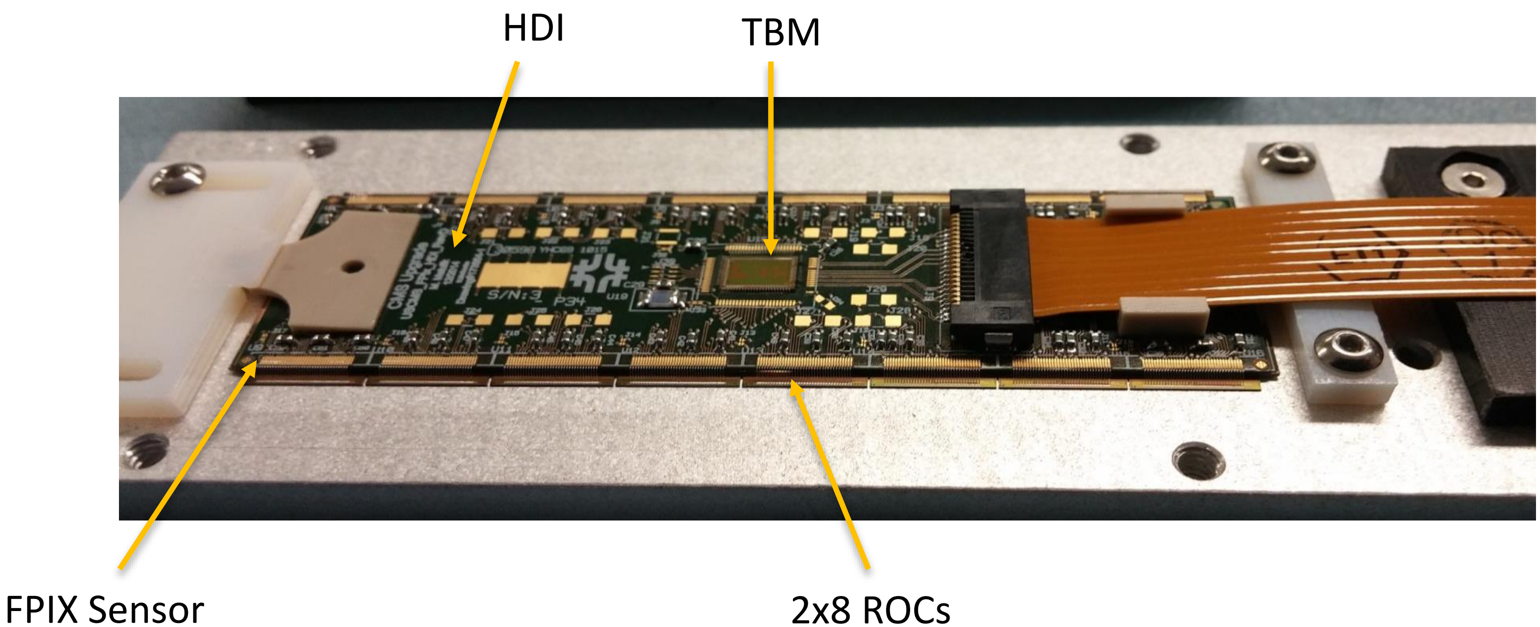


The Pixel Detector – Phase I Upgrade

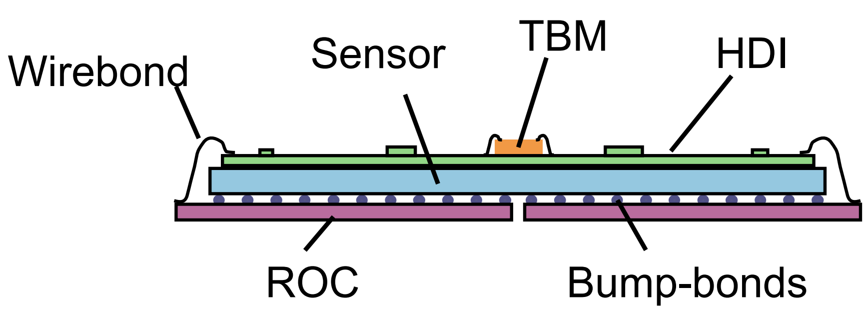
- Optimized detector layout for 4-pixel-hit coverage over the full tracker acceptance
  - Barrel layers from 3 to 4; Forward disks from 4 to 6
- Reduced material budget
  - New cooling system based on two-phase CO_2
- New pixel readout chip (ROC) and token bit manger (TBM), digital readout (160MHz)
- Improved pattern recognition and track reconstruction



FPIX Module

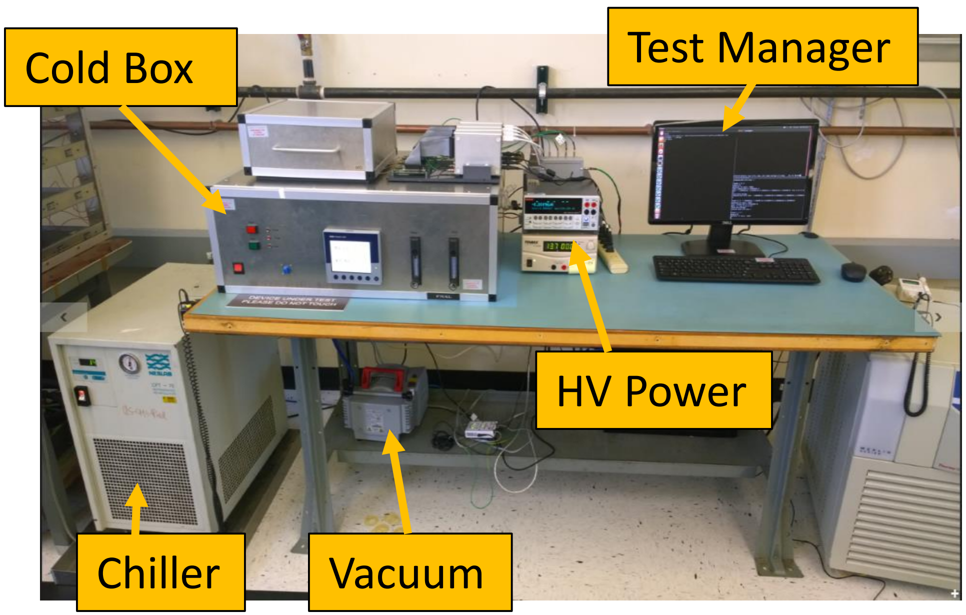


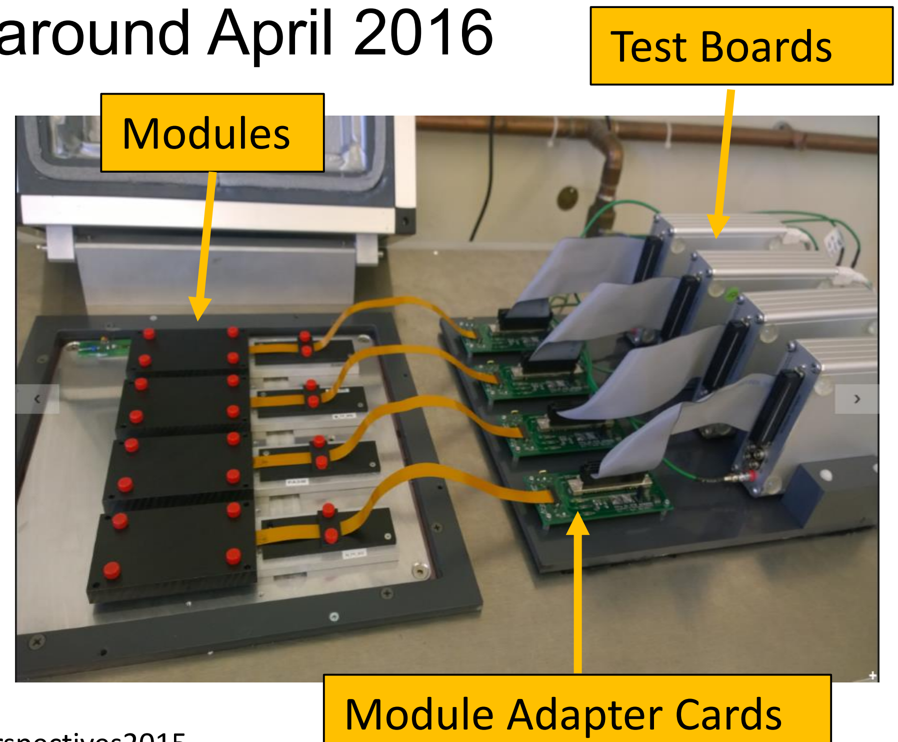
Schematic cross section:



Module Testing & Qualification

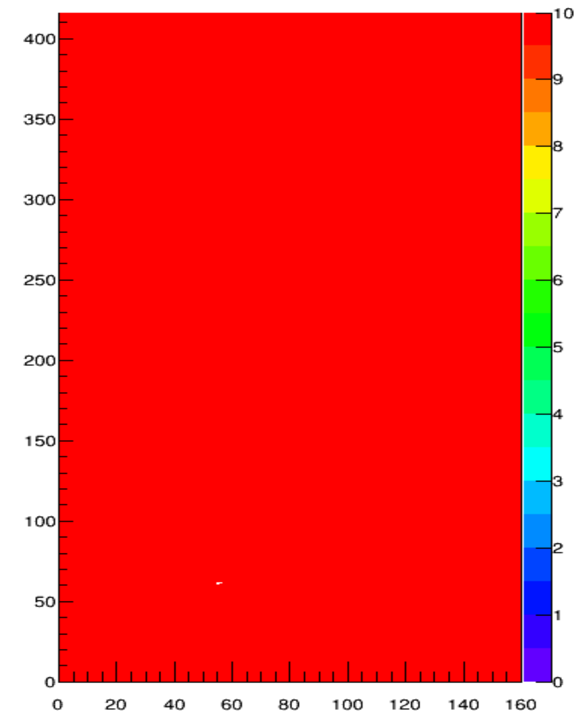
- The bulk of the module testing will be performed at Fermilab
- Two stations with cold boxes
  - Test 4 modules in parallel
- Expect to test 8 modules / day (average)
- Finish testing ~1000 modules around April 2016





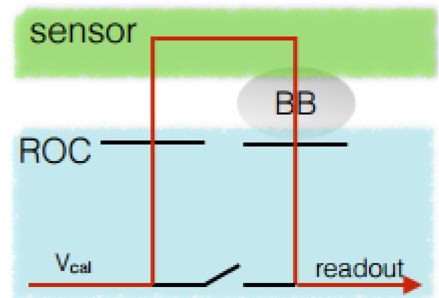
Pixel Alive Test

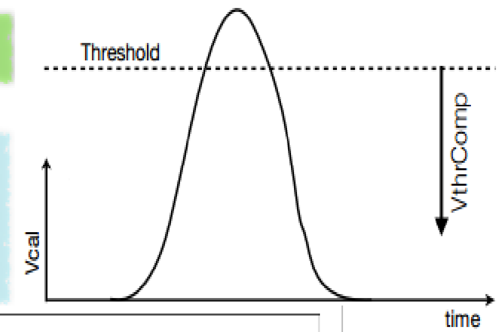
- Pixel alive is a three-fold test that measures the functionality of the pixel unit cell
  - Inject calibration charge 10 times and measures the number of hits
  - Inject calibration charge into each individual pixel and verify that the correct pixel responds
  - Check that pixels can be masked

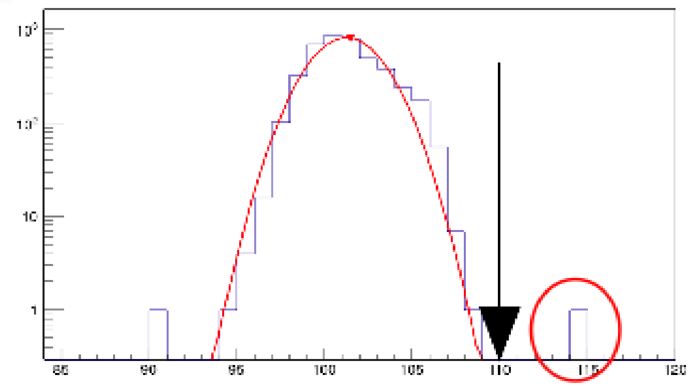


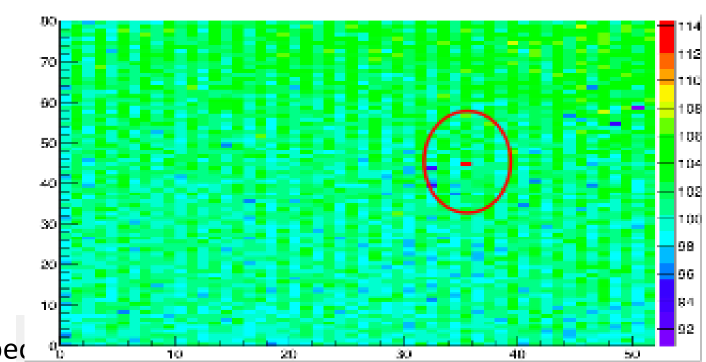
Bump Bonding Test

- Send fixed calibration charge into sensor
- Scan over the comparator threshold
- Generate efficiency curve vs. the comparator threshold
- Fit efficiency to extract turn-on value
- Fit Gaussian to bulk of this distribution, flag pixels with high turn-on as bad









Module Testing Workflow

Assembly Testing

- IV
- Pretest
- ≥5 thermal cycles (-30C to 50C)
- IV
- Pretest
- Pixel alive
- Trim
- Bump bonding

Calibration Testing

- IV
- Pretest
- Pixel alive
- Trim
- Pulse height optimization
- Gain pedestal
- Bump bonding
- S-curves

~10%

~90%

X-Ray Testing

- Fluorescence Test
- High Rate Test

- IV
- Pretest
- Pixel alive
- Trim
- Pulse height optimization
- Gain pedestal
- Bump bonding
- S-curves

Purdue/Nebraska

FNAL

University of Illinois - Chicago/Kansas

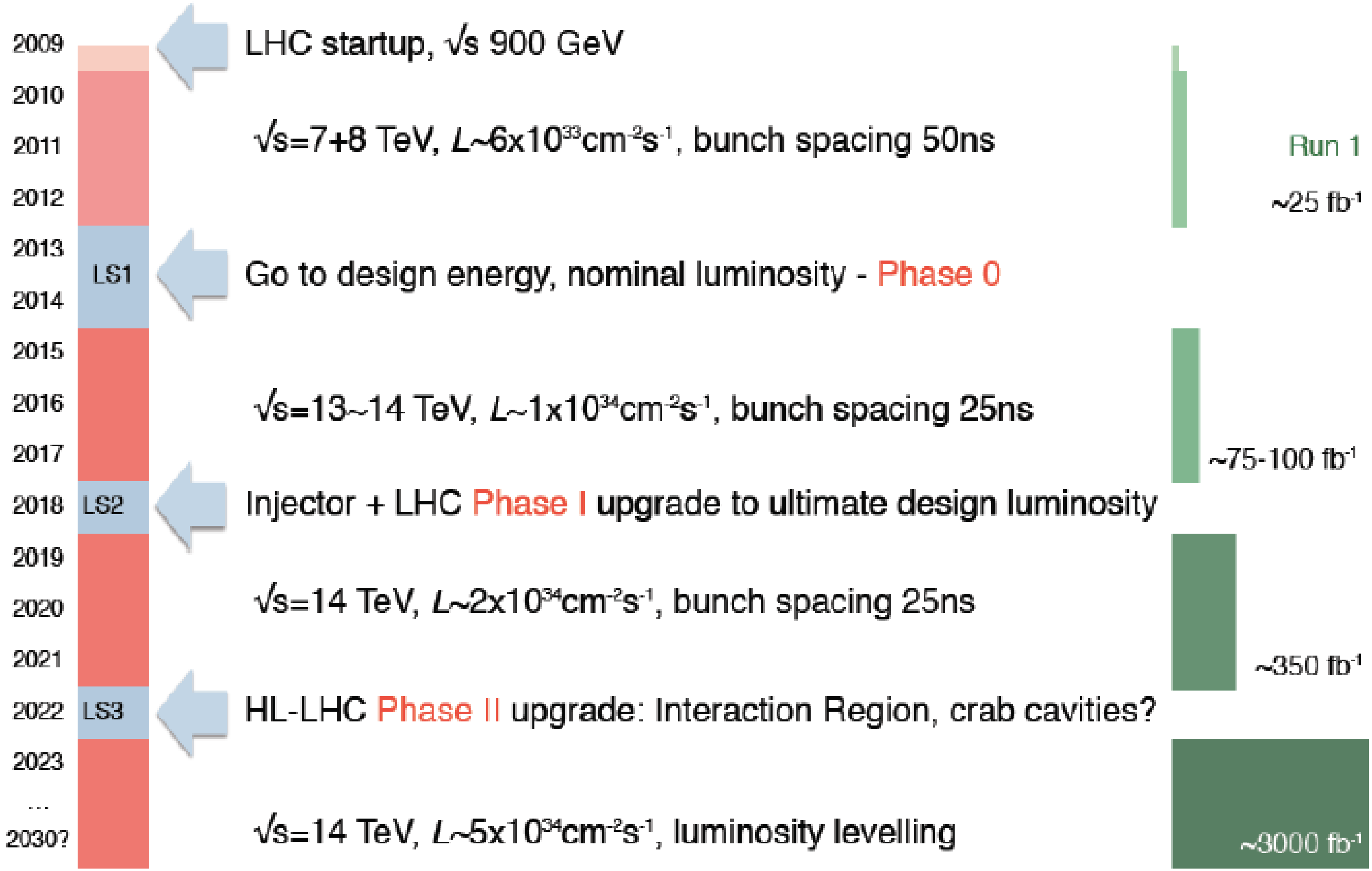
Summary

- The pixel detector is an integral part of the Silicon Tracker
- The current pixel detector performs well under current run conditions
  - Under future run conditions will experience performance degradation
- An upgraded pixel detector is under construction to be installed in the winter of 2016/2017
  - Will maintain the current performance under extreme pileup conditions
- Module testing and qualification procedures established and validated

Thank you!

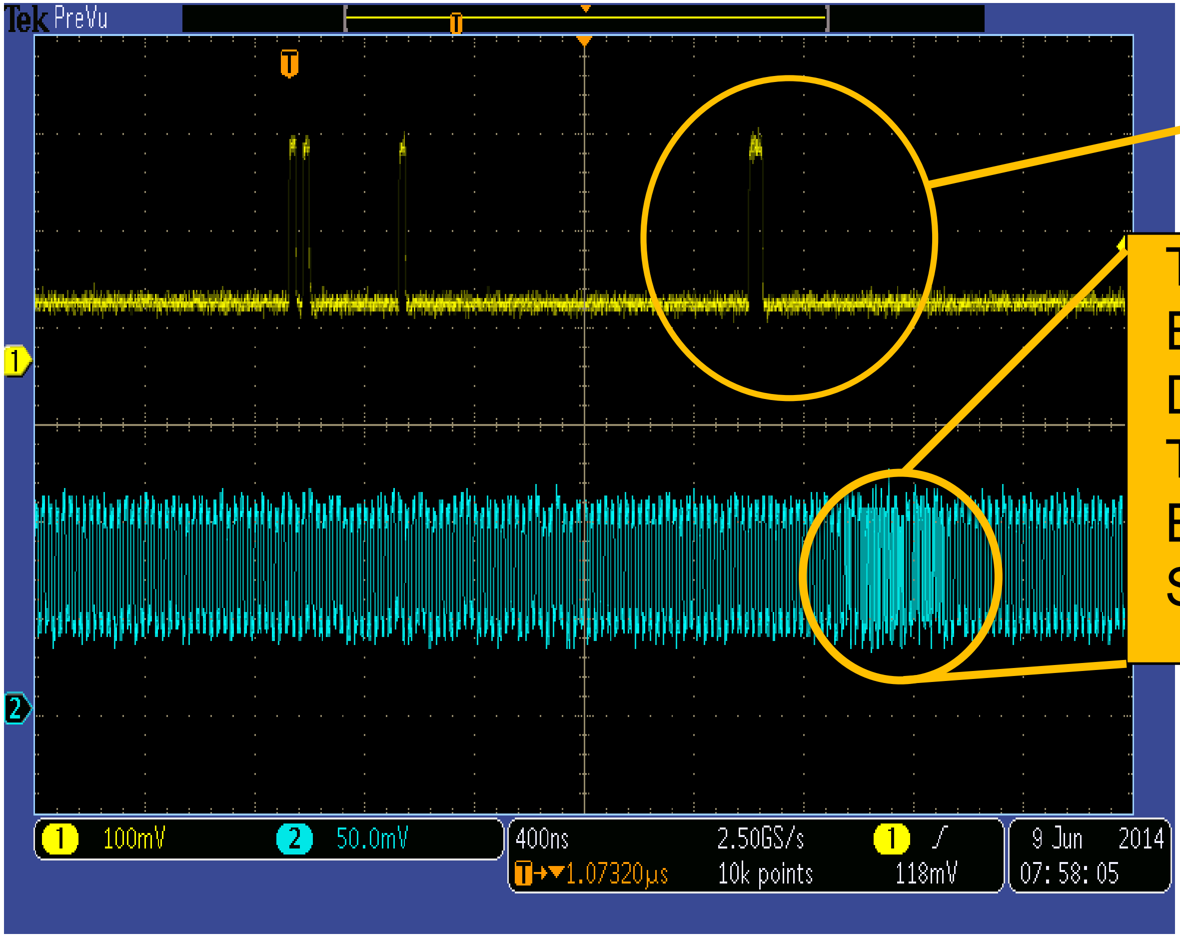
Backup

The LHC Upgrade



TBM Decoding Test

- The TBM decoding test issues a single trigger to the TBM

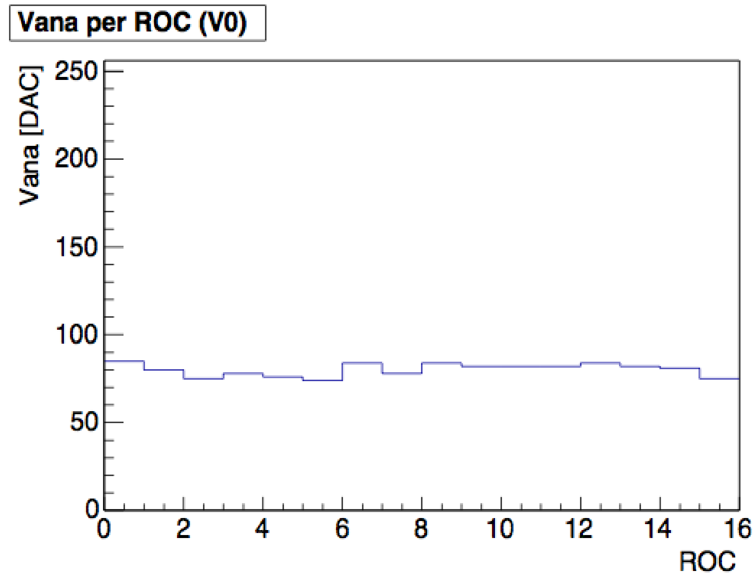


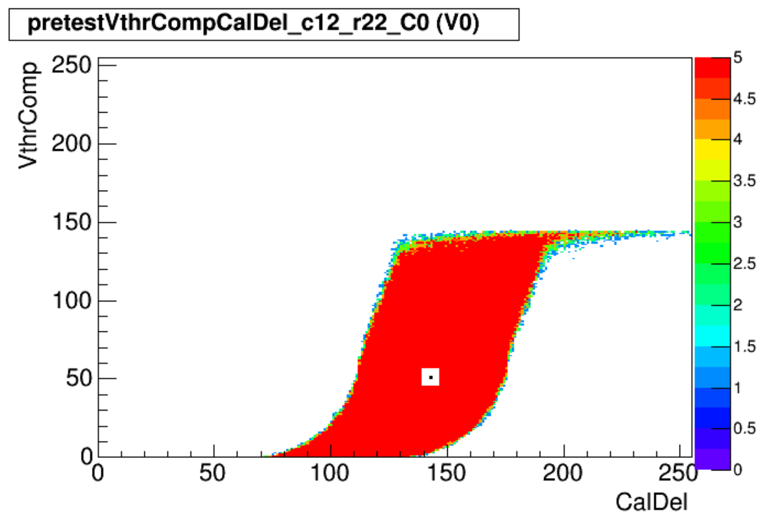
Triggers

TBM Header - 011111111100
Event Number - 00000001
DataID - 10110000
TBM Trailer - 011111111110
Event Info - 0110001000
Stack Count - 000001

Pretest

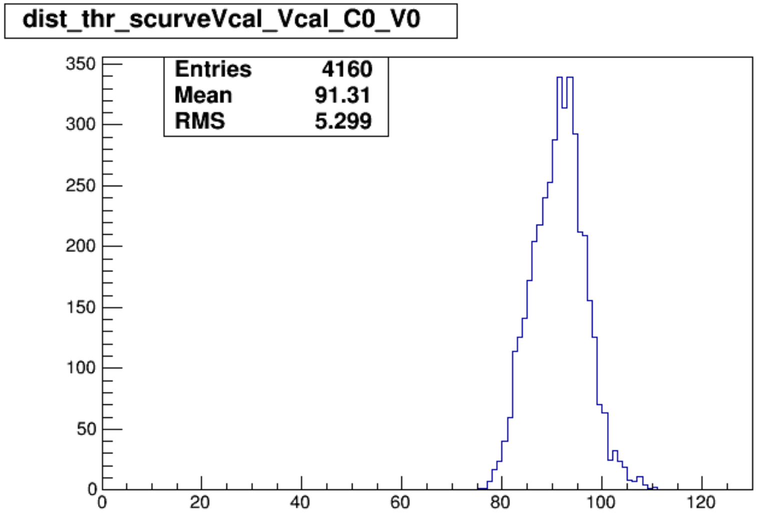
- The pretest establishes the basic functionality of the module and prepares it for further testing
  - Check ROC Programability
  - Tune analog voltage such that each ROC pulls 24mA
  - Verify the TBM and ROC timing
  - Set the comparator threshold and calibration delay for each ROC

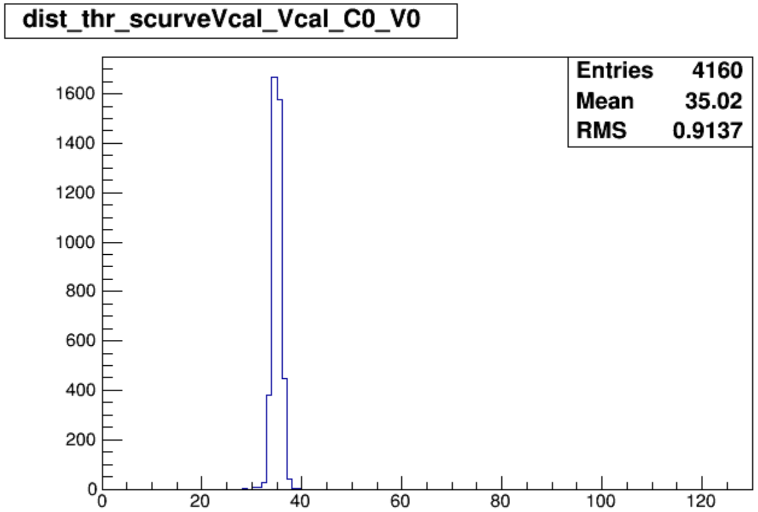




Trim Test

- The trim test consists of two different test that **unify the pixel response across all ROCs**
  - RMS of threshold distribution should not exceed 400 e^-
- The trim test sets the VThrComp and VTrim of each ROC
- The trim bit test sets 4 trim bits for each pixel.
- The goal of this process is to provide the narrowest turn on for a target VCal.

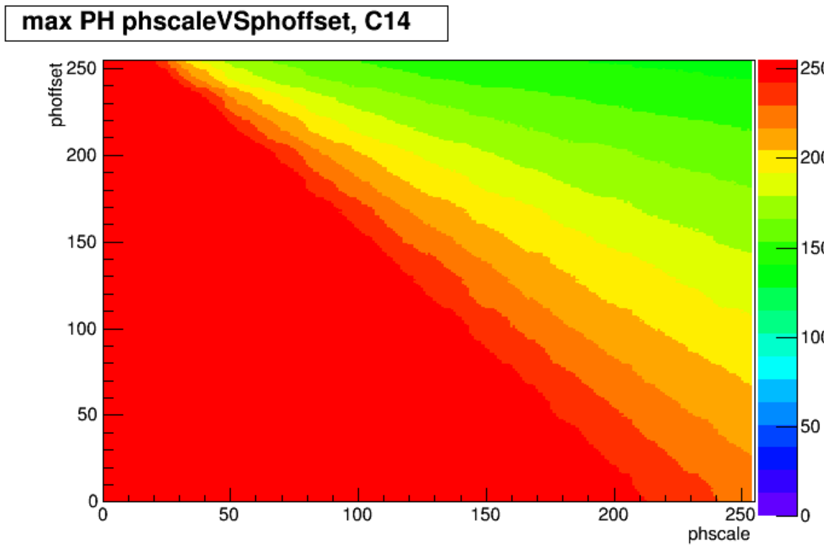


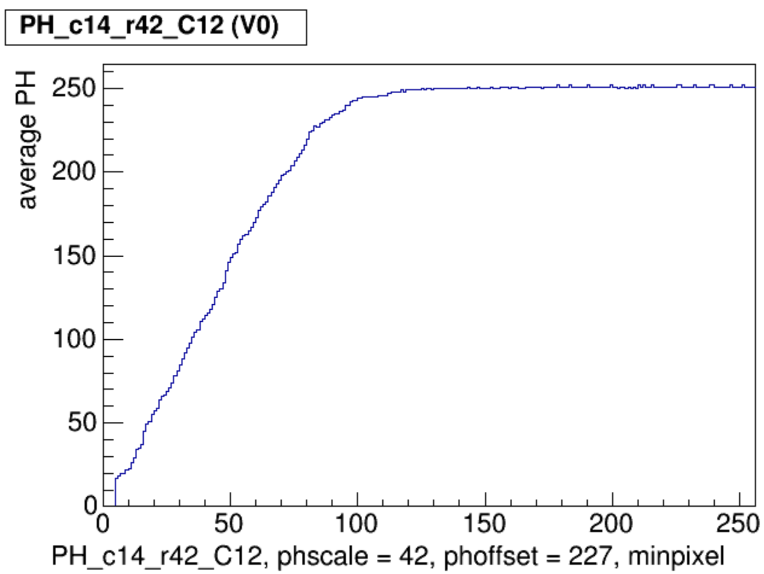


Pulse Height Optimization

- **Establish the dependency of the pulse height on the injected charge**

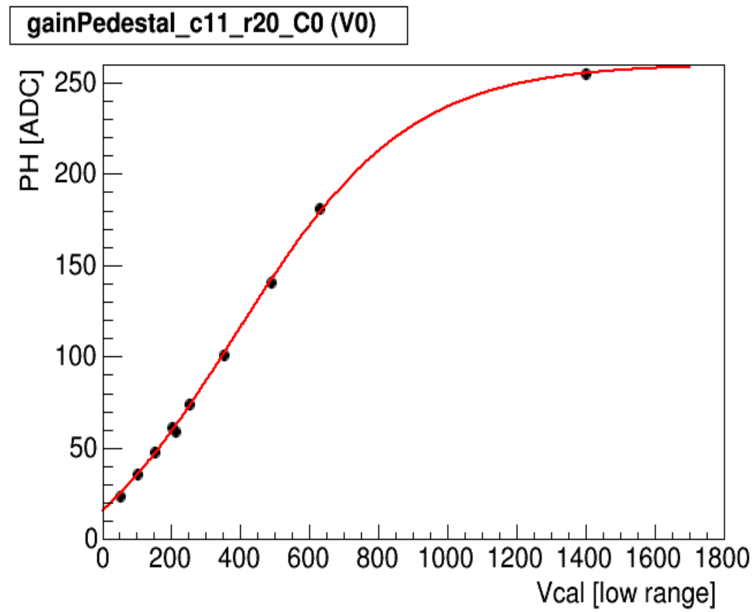
- Phscale and Phoffset are scanned, and the point where the pixel amplifier saturates at the target Vcal is selected





Gain Pedestal Test

- The gain pedestal test measures the response of each pixel
  - Ensure linearity
  - Tolerate up to 20% variation of the gains
  - Pedestal RMS is required to be less than 5000 e^-
- This is done by measuring the pulse height vs. injected VCal and fitting the response curve
- Once the gain pedestal test is finished, the module is fully calibrated and ready for X-ray tests



$$P_3 + P_2 \tanh(P_0 x - P_1)$$

S-curves Test

- The S-curves test measures the performance of a module as a function of a single dac parameter
- Once a module is fully calibrated, a VCal S-curve will measure the performance of the trim and the **pixel noise**
  - Noise should not exceed 1000 e^-