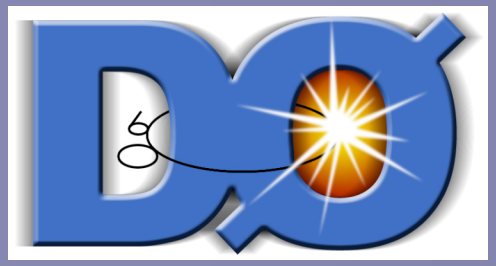
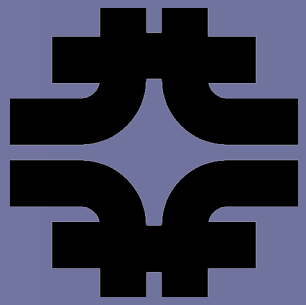




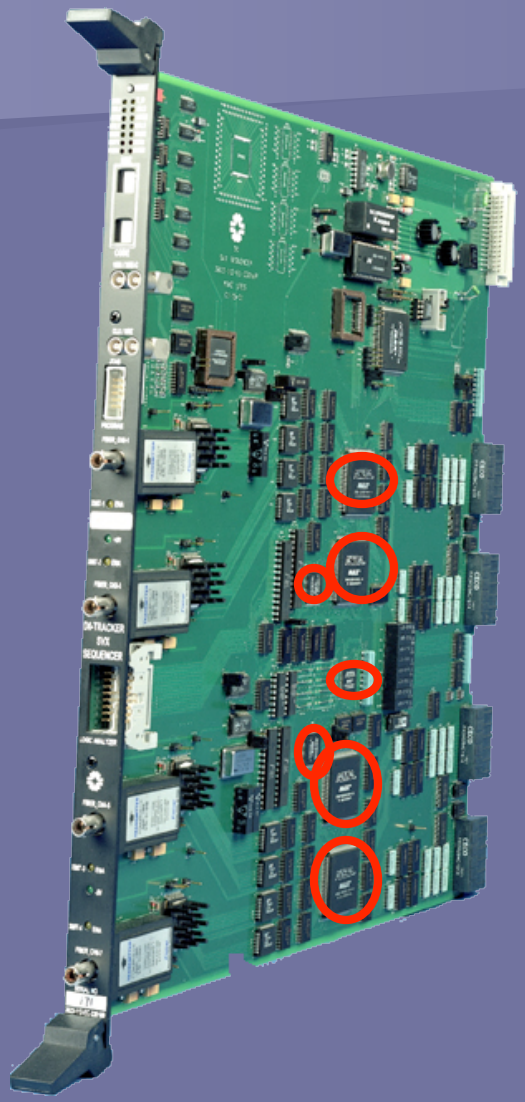
SIST PROGRAM
D-ZERO EXPERIMENT

By Jefferson OKRAKU

Supervised By Geoff SAVAGE

Control Systems Group

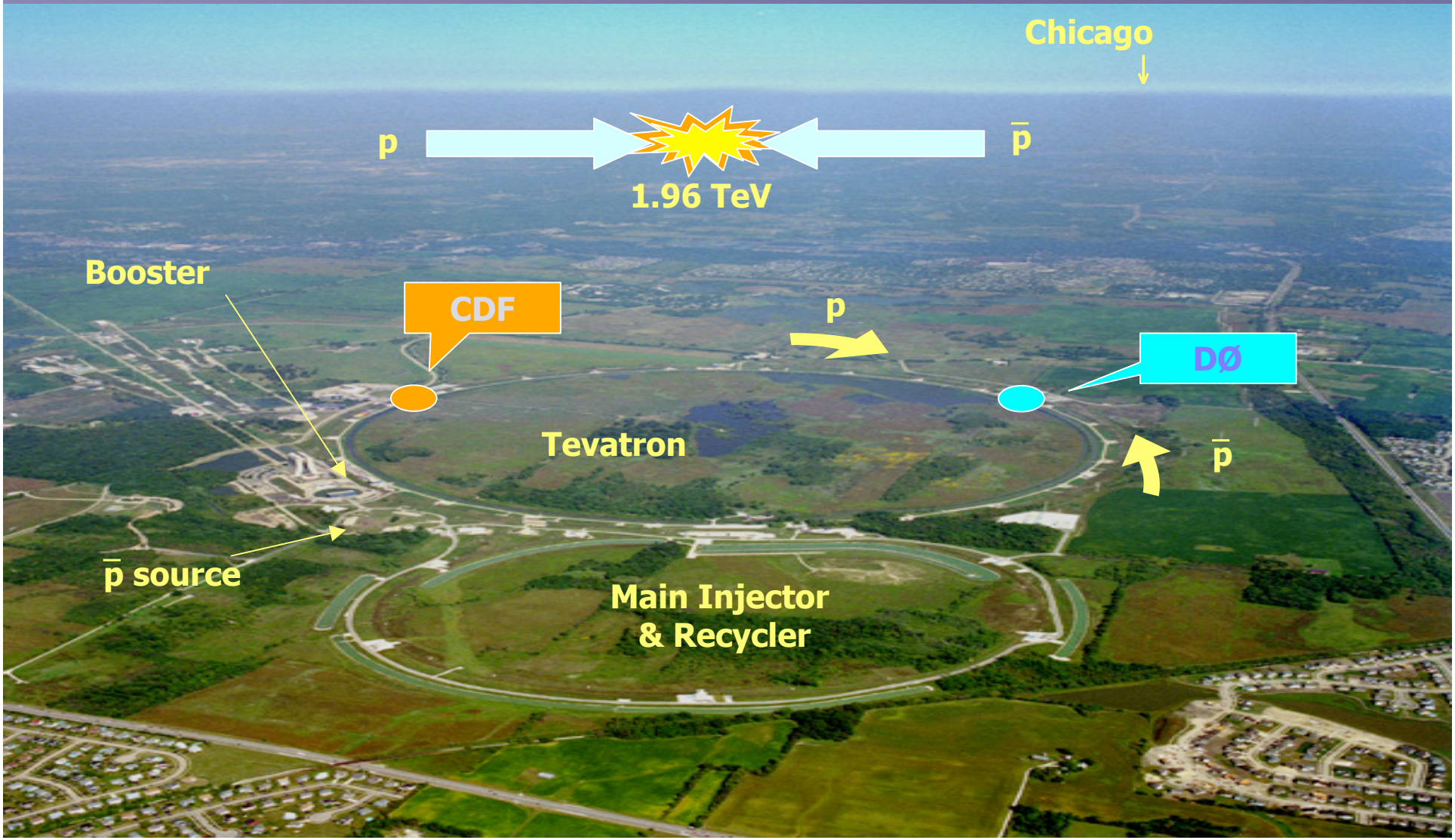
Summer Project



- Objective:
- To send data to the chips on this board from a far off location

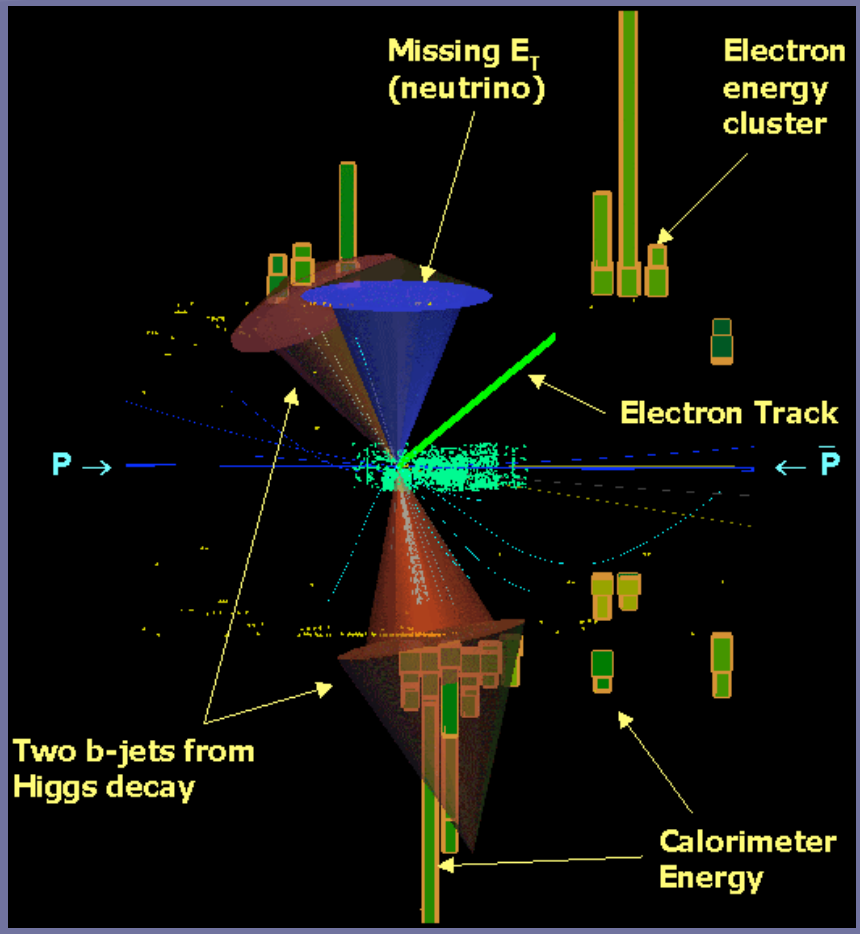
…..and that is exactly what happened….

Fermilab and its Accelerators

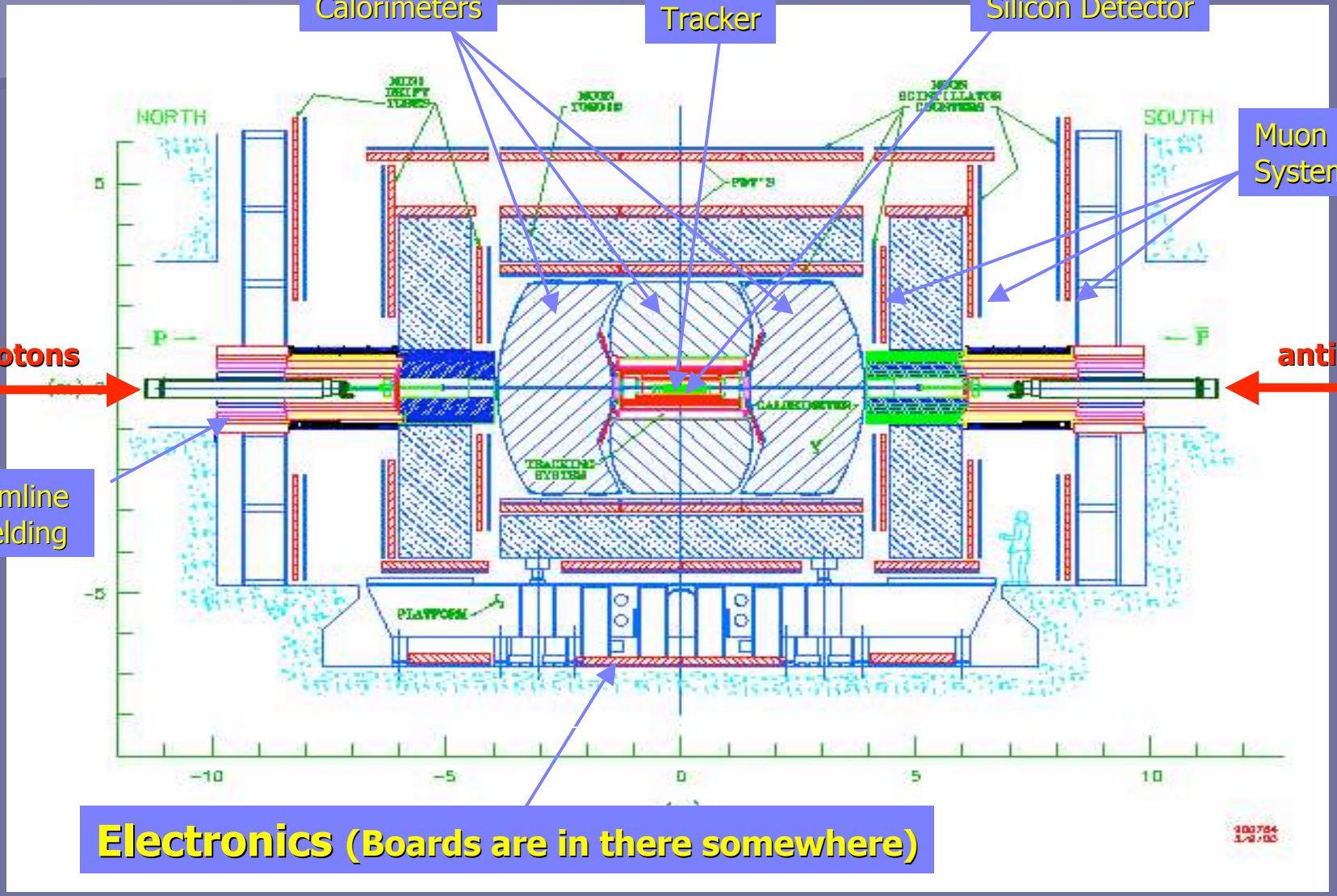


DØ Experiment

- The DØ experiment is focused on precise studies of interactions of protons and antiprotons at the highest available energies.
- DØ detector is one of two large particle detectors here at Fermilab.
- It's basically a camera.
- Can inspect Zillions of collisions but records just a few

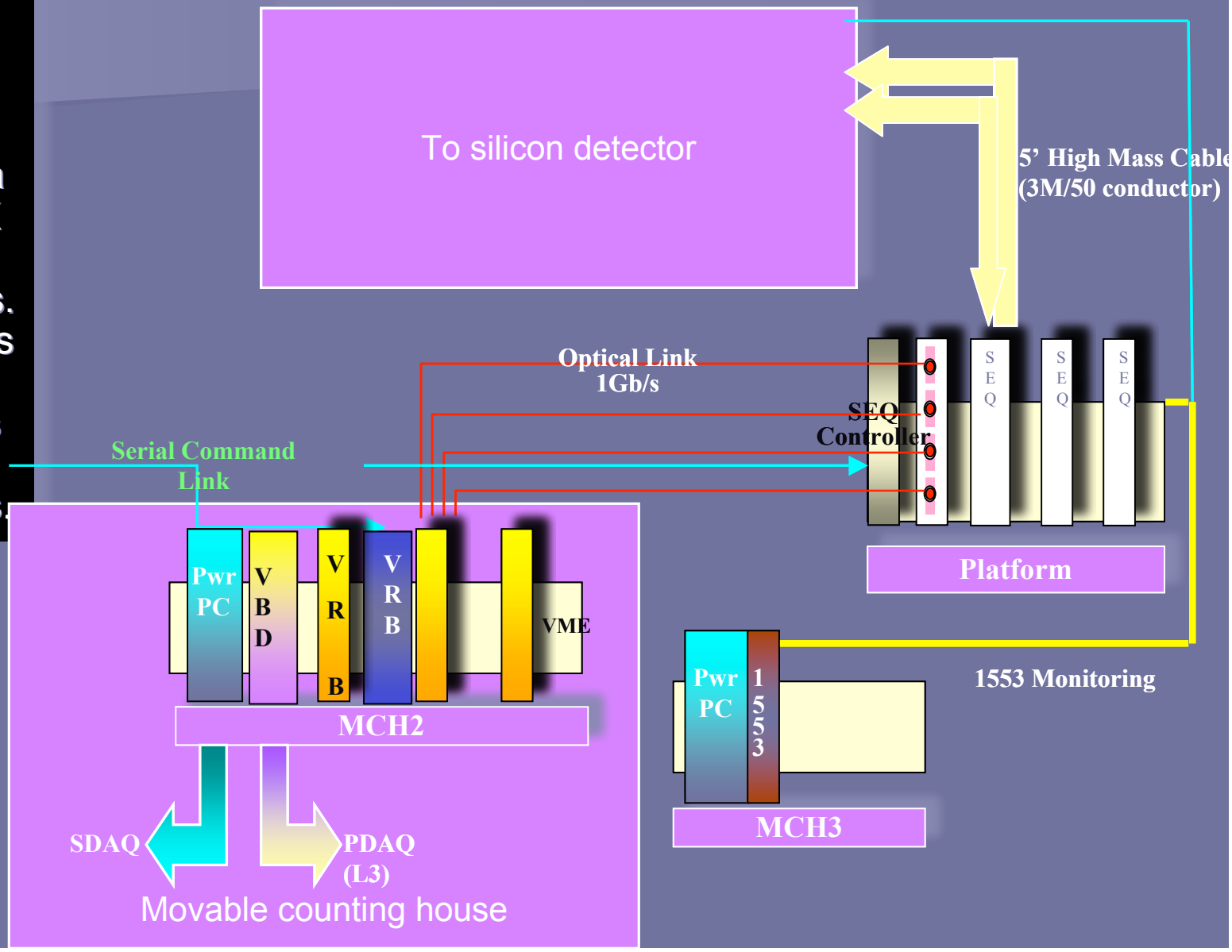


DØ Detector


Calorimeters
Tracker
Silicon Detector
Muon System
protons
antiprotons
Beamline Shielding
Electronics (Boards are in there somewhere)
NORTH
SOUTH

Silicon Readout Data Flow

The SVX sequencer controls SVX chips and transfers data from the SVX chips to the readout crates. The SVX chips digitize 128 analog inputs from silicon strip detectors.

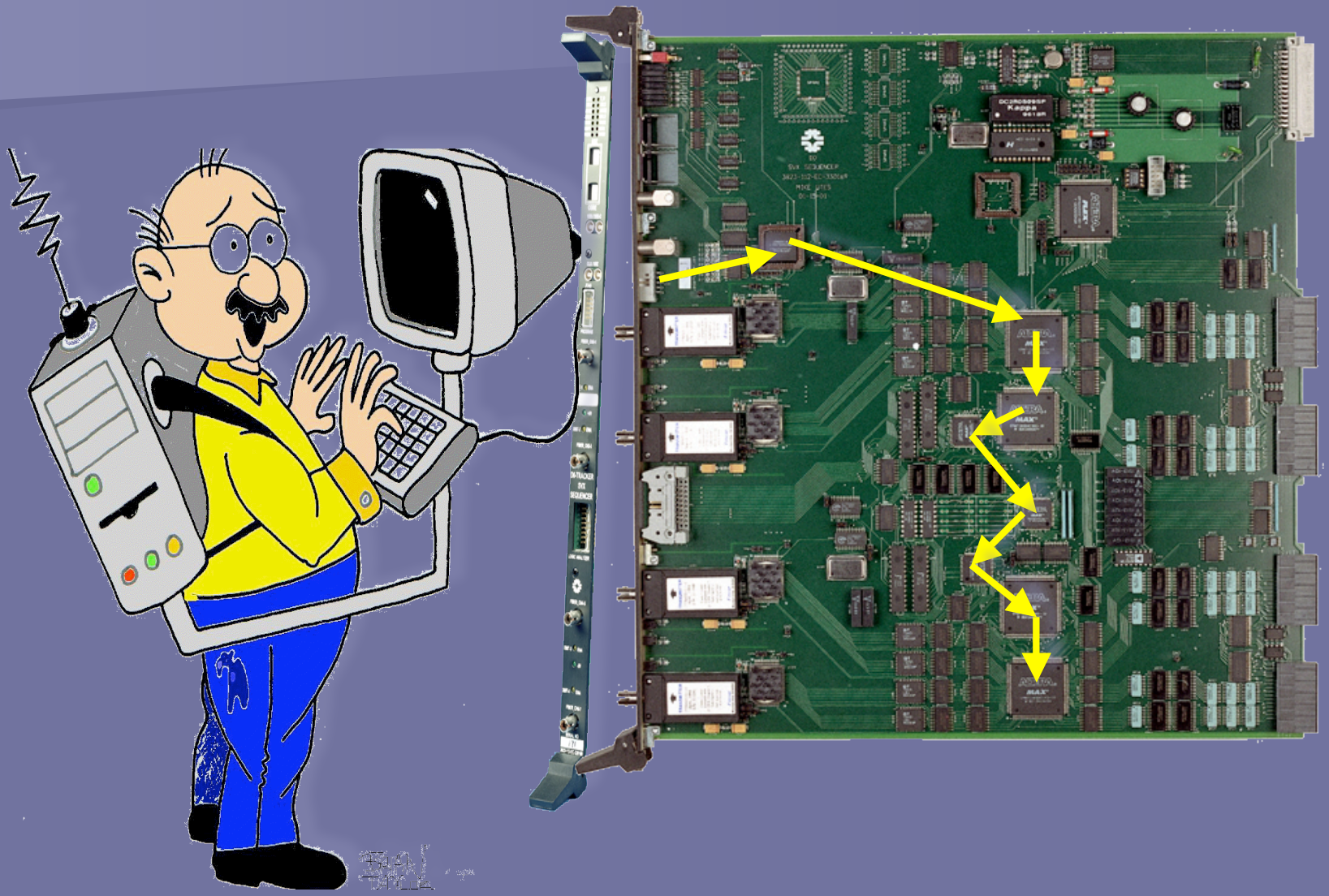


Problem

- SVX Sequencers are at an obscure location on the detector.
- In order to change the firmware on any of the chips, for testing or otherwise, someone has to go down to the detector.
- To do this, they need permission (You can't just walk onto the platform).

If only we can reprogram the boards without going to them physically?

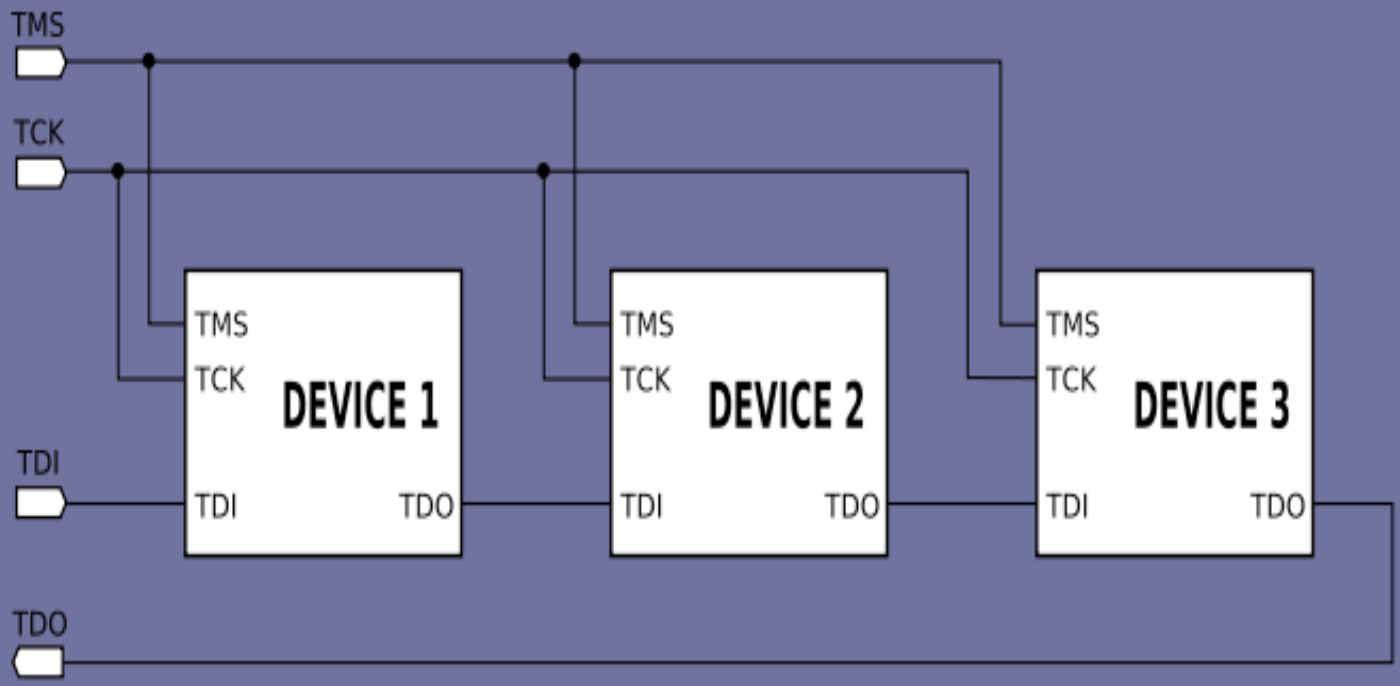
Programming FPGA Chips



FPGA and Firmware

- Field Programmable Gate Array.
- They are semiconductor devices containing programmable logic components called "logic blocks", and programmable interconnects.
- Firmware is a set of instructions programmed on an FPGA.
- Unlike software, it is not loaded from a disk and unlike hardware, it can be modified once installed.

How the chips are connected on the board

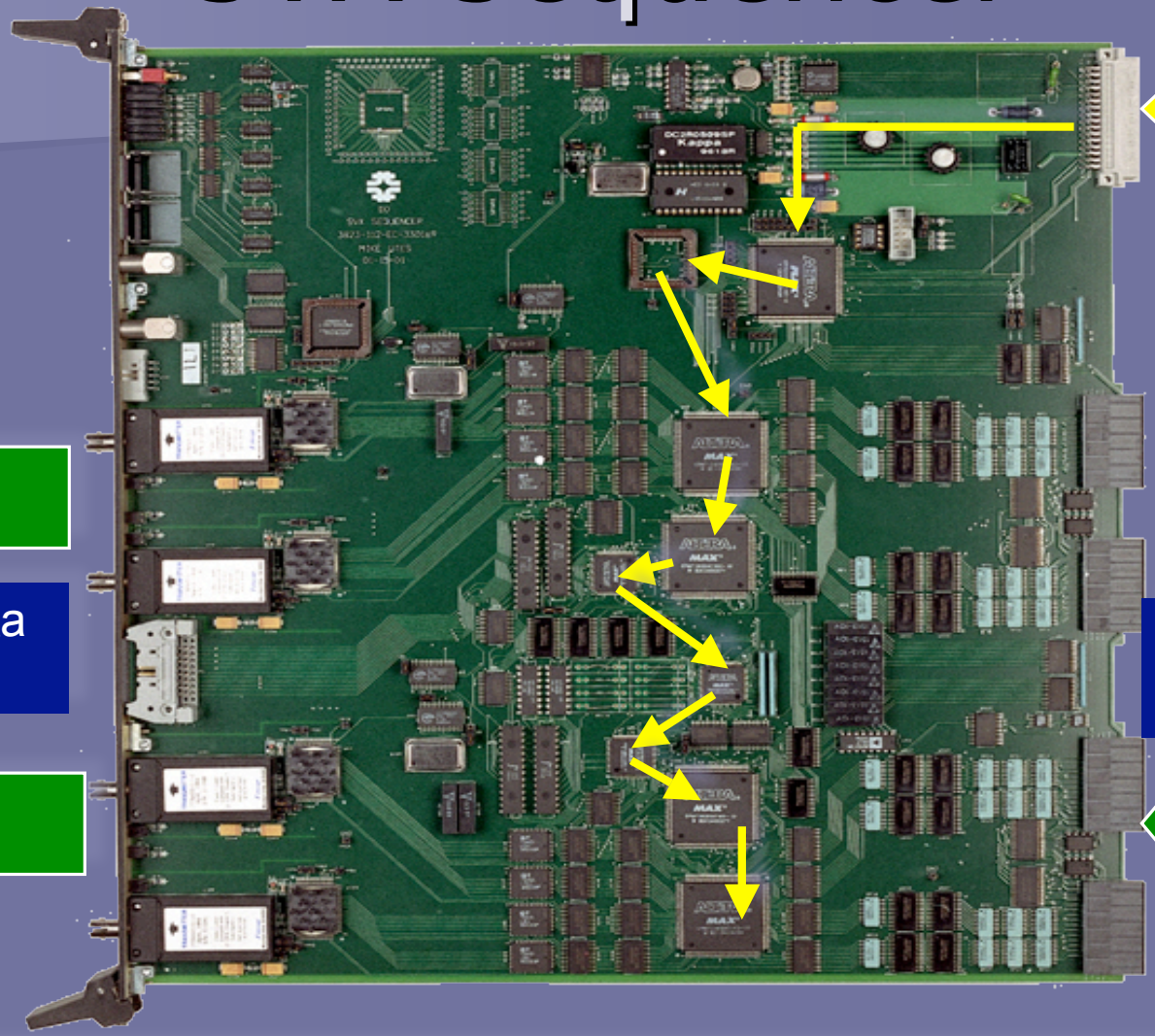


JTAG (Joint Test Action Group) Chain

The JTAG chain is a group of FPGAs daisy-chained together via a JTAG interface.

A JTAG interface is a special four/five-pin interface added to a chip

SVX Sequencer



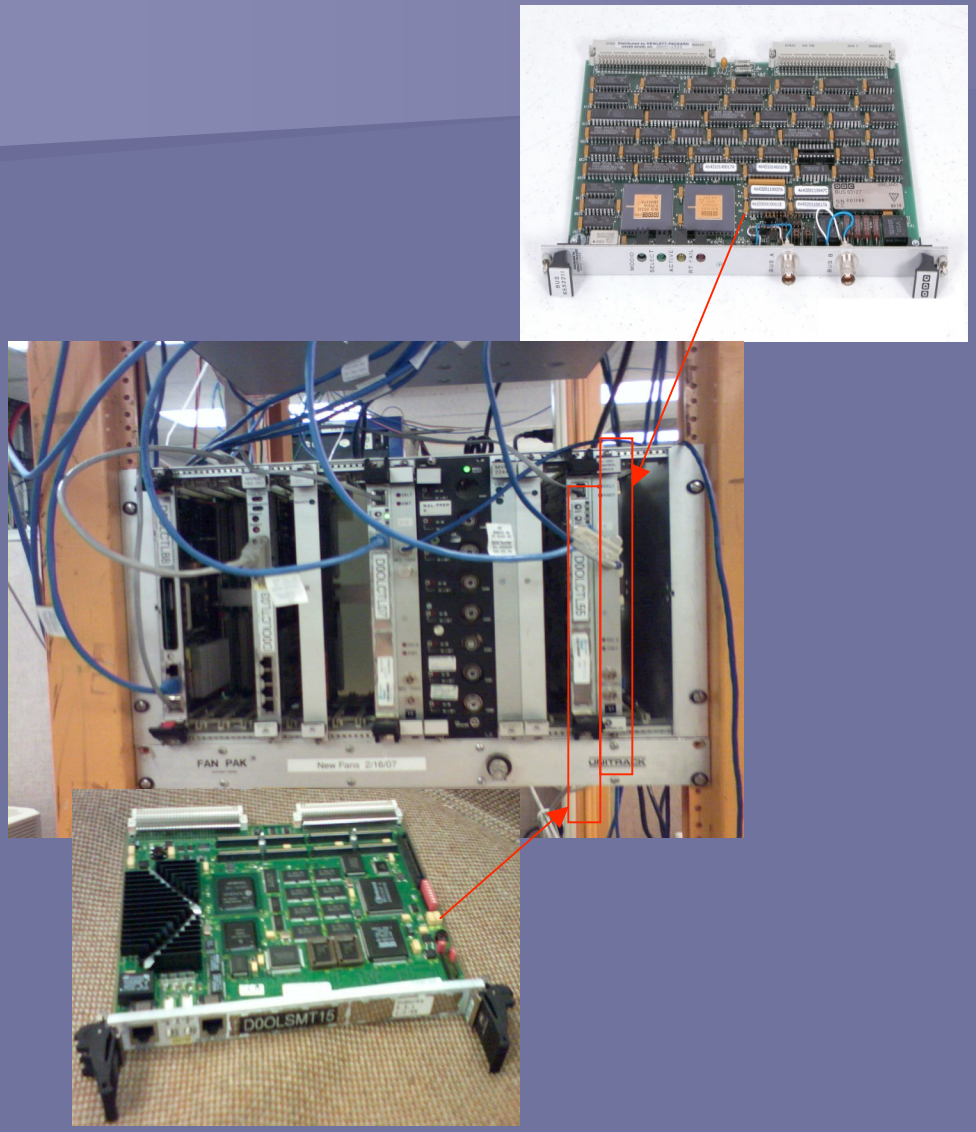
From 1553 bus

Physics Data OUT

Physics Data IN

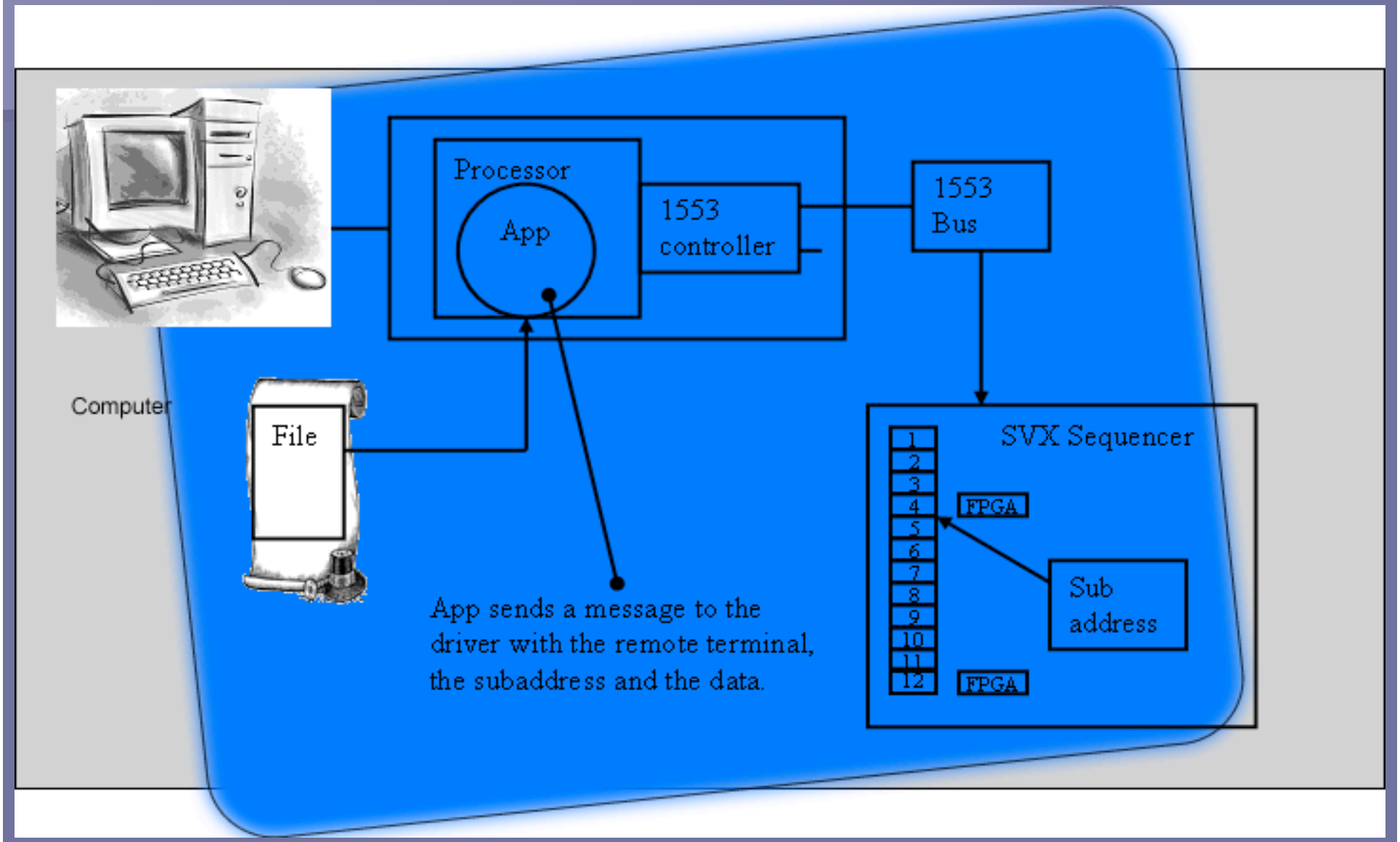
The SVX Sequencer boards are 9U by 280mm circuit boards that reside in slots 2 through 21 of each of eight Eurocard crates

1553 Bus and Controller



- The 1553 bus is a device which consists of a wire pair that transfers data or power between computer components inside a computer or between computers .
- The controller operates according to a command list stored in its local memory to direct the bus
- To accommodate the my program the 1553 driver, the program is tailored to talk to the bus bit at a time.

Diagram of Process

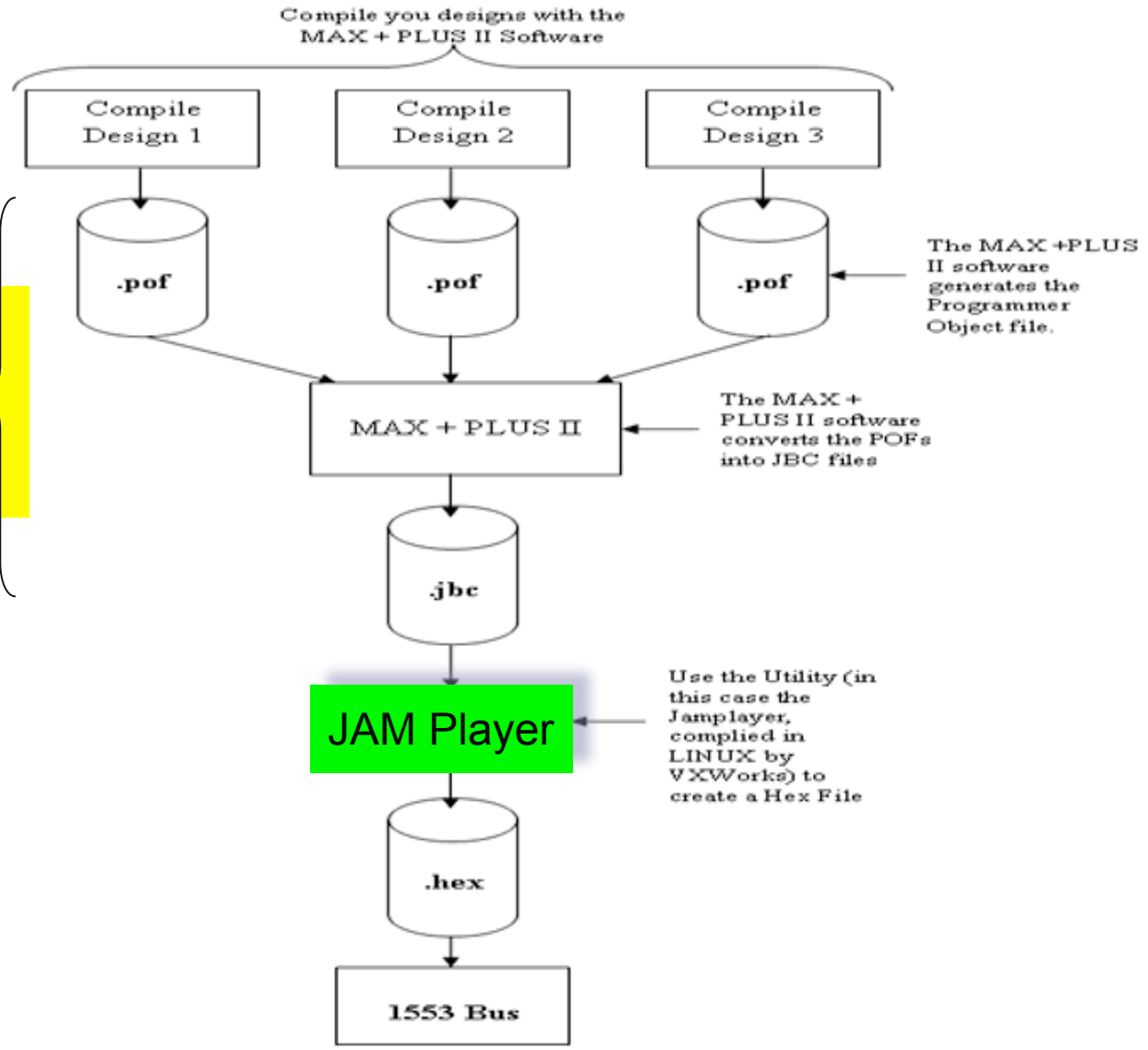


Firmware

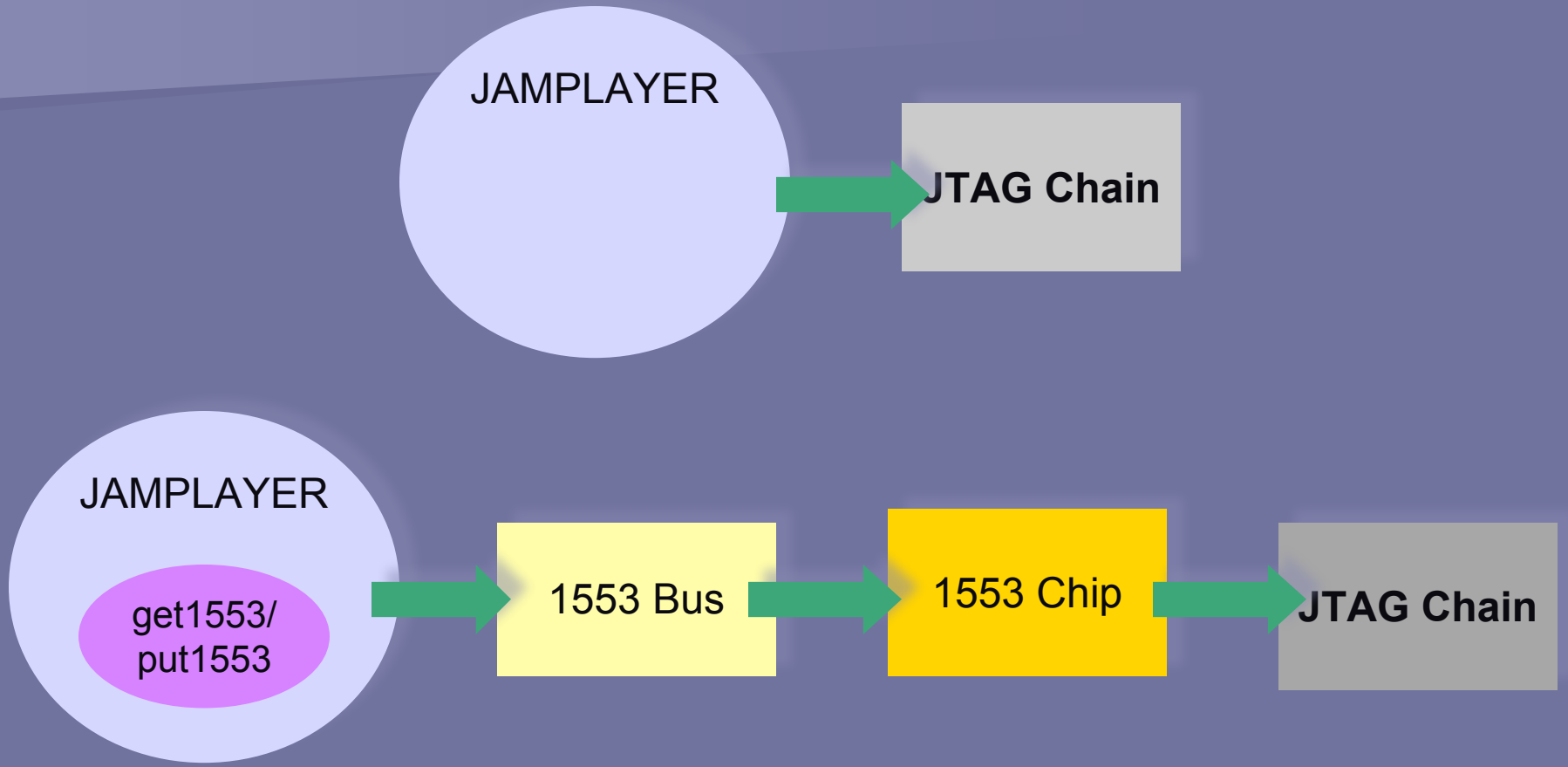
Mike Utes

Engineer @ D0

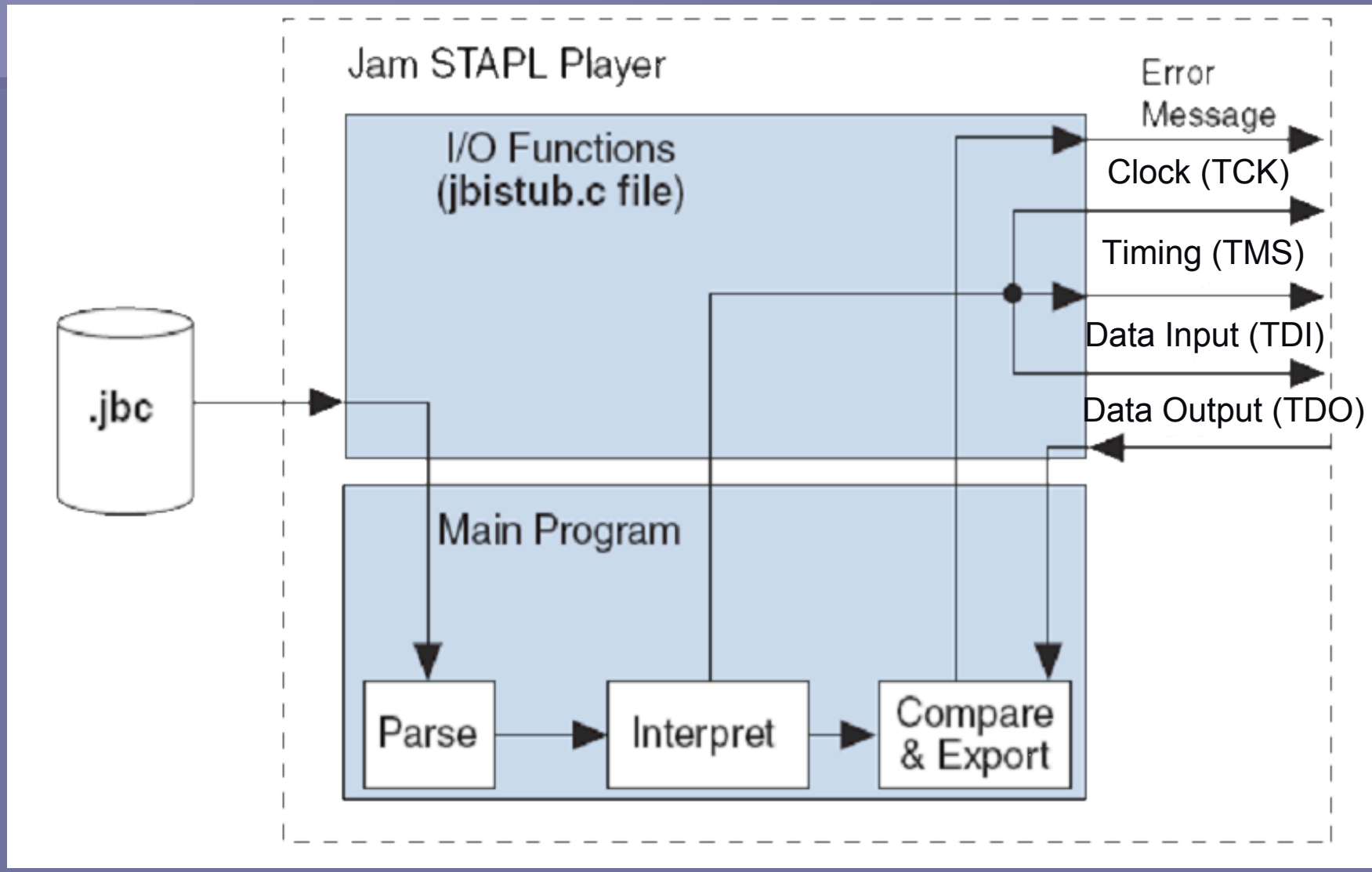
Board Designer



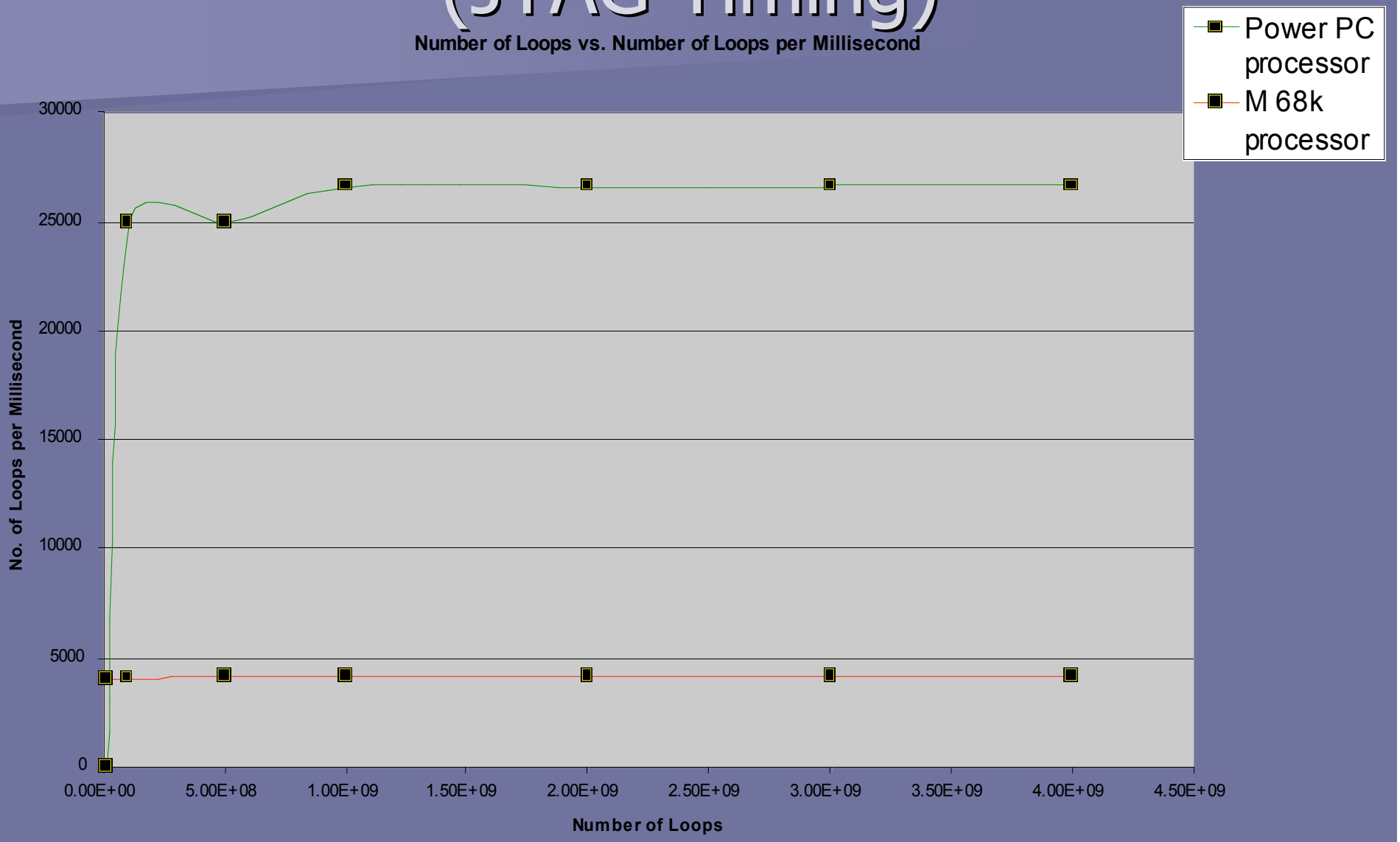
The old and the new



Software:
How the JAM PLAYER WORKS



How long is a millisecond ? (JTAG Timing)



Action	Size of File	Time Taken by Processor (Minutes: Seconds)	
		M 68k	Power PC
program 1st chip	43KB	22:07	7:47
verify 1st chip	43KB	12:09	4:24
verify whole chain	72KB	55:23	21:18
Verify 1st and 7th chip	48KB		7:01
Verify 2nd and 6th chip	59KB		9:47
Verify 3rd and 5th chip	43KB		7:00
Verify 4th chip	43KB		3:06
get1553		300 µs	123 µs
put1553		300 µs	120 µs

Things I learned

- How to use Unix, VXworks, Python
- How a 1553 bus and controller works
- How the D0 Experiment works

Acknowledgment

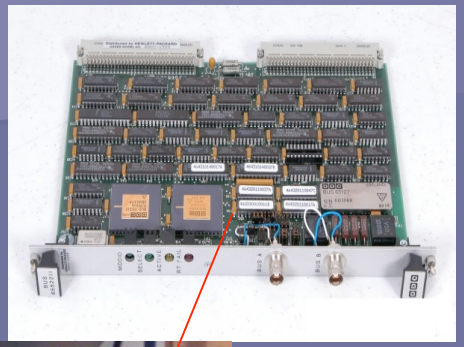
- Geoff Savage
- Mike Utes
- Taka Yasuda
- Jamieson Olsen
- Mayling Wong-Squires
- Bill Lee and Fritz Barlett
- Elliot McCrory
- Dianne Engram
- Me

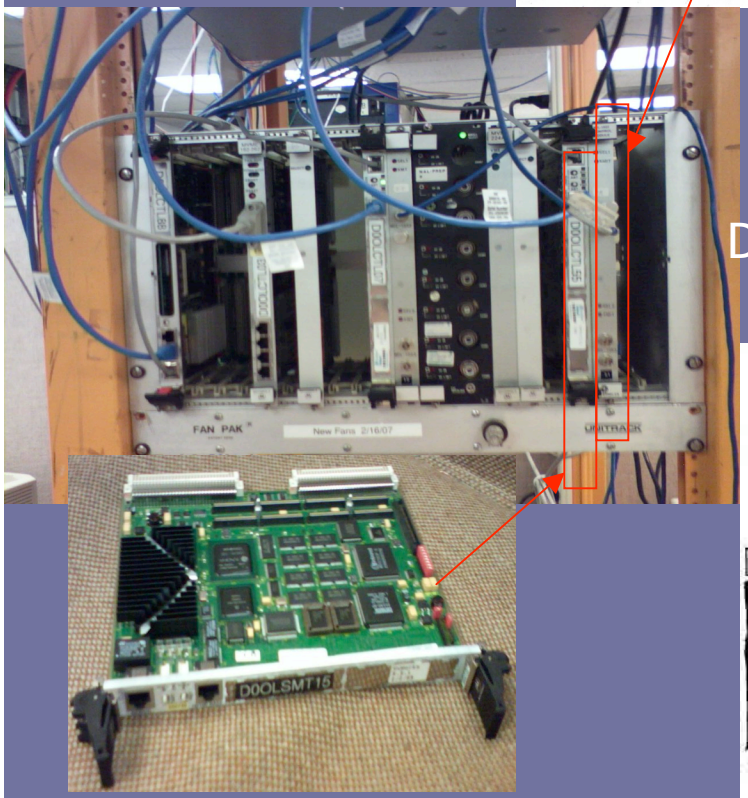
THE END

No questions?
NICE!!!

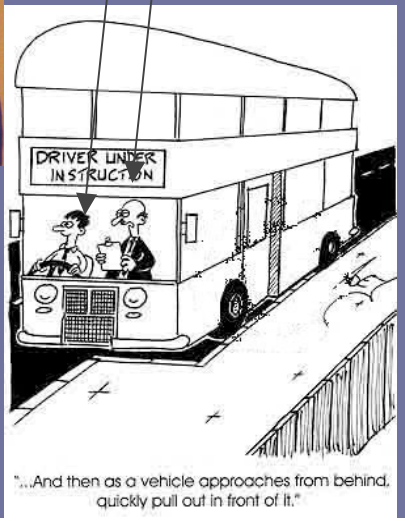
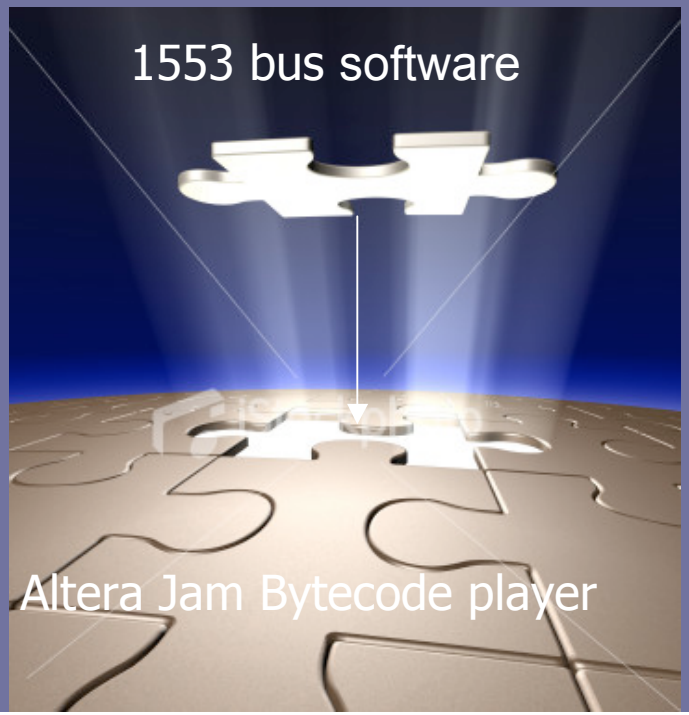
Thank you.

1553 Bus Driver and Controller





- To accommodate the a program the 1553 driver, a program to talks to the driver bit at a time, had to be merged with the Jam Player Software.

Driver

Controller