CMOS Image Sensors and Prospects for High-Speed Applications

Eric R. Fossum

September 14, 2018

ULITIMA 2018

Argonne National Laboratory
Where is Dartmouth College?

Pasadena & Los Angeles, California

Hanover, New Hampshire
CMOS IMAGE SENSORS
CMOS Image Sensors Enable Billions of Cameras Each Year

About 5 Billion Cameras Made Each Year (More than 150 per second)

CMOS Image Sensor Sales March Higher into Next Decade

2012-2017 CAGRs
Sales = 11.9% Units = 17.9%

2017-2022F CAGRs
Sales = 8.8% Units = 11.7%

Source: IC Insights

Many Kinds Of Digital Cameras
MOS “Photomatrices”
0th Generation Image Sensor

~June 1966

First self-scanned \( \rightarrow \)
Sensor 10x10 1966/67

Mid-late 1960’s
MOS arrays at Plessey
with startup Integrated Photomatrix Ltd. (IPL)

The 64 by 64 array
and a 1024 linear array

And Fairchild with startup Reticon
Charge-Coupled Device (CCD)  
1st Generation Image Sensor

- CCD invented at Bell Labs 1969, then CCD image sensor in 1970.
- Perfected with mass production in Japan.
- Mainstay of digital cameras and camcorders in 1980’s and 1990’s.
CCD Cameras
1970’s - 1990’s

Early 70’s Bell Labs CCD camera by Mike Tompsett et al.

Steve Sasson with first Kodak self-contained digital camera (1975)

RCA Camcorder

DALSA industrial CCD camera late ’80s

NASA Galileo Spacecraft CCD camera (with optics) early ’80s (800x800)

Sony Camcorder early 90’s
2009 Nobel Prize in Physics

"for the invention of an imaging semiconductor circuit – the CCD sensor"

CCD image sensor inventor:
Michael F. Tompsett
US patent no. 4,085,456

Figure 4. Original notes from the Boyle and Smith’s brainstorm meeting on September 8 1969, when they made the first sketch of a CCD.
1990’s Need: Smaller cameras for smaller spacecraft at JPL/Caltech
Some Problems with CCDs

- Charge must be perfectly transferred thousands of times to get to output amplifier.
  - Requires high voltages
  - Requires special device structures
  - Very susceptible to radiation damage and traps
  - Requires power to drive huge whole-chip capacitance
- Requires many support chips
- Difficult to make it work right
- Serial readout gives slow frame rate
- High bandwidth (noisy) output amplifier
Active Pixels with Intra-Pixel Charge Transfer

- Complete charge transfer to suppress lag
- Correlated double-sampling to suppress kTC noise
- Double-delta sampling to suppress fixed pattern noise
- On-chip ADC, timing and control, etc.

One pixel

electrons in silicon

light
correlated double sampling (CDS)

amplifier
“Camera-on-a-Chip” Enables Much Smaller Cameras
Most of the JPL Team circa 1995

Advanced Imager Technology Group, Jet Propulsion Laboratory, California Institute of Technology 1995
Back row: Roger Panicacci, Barmak Mansoorian, Craig Staller, Russell Gee, Peter Jones, John Koehler
Front row: Robert Nixon, Quisp Kim, Eric Fossum, Bedabrata Pain, Zhimin Zhou, Orly Yadid-Pecht

Missing: Sabrina Kemeny, Junichi Nakamura, Sunetra Mendis
Entrenched industry moves slowly in adopting new technologies so in February 1995 we founded **Photobit Corporation** to commercialize the CMOS image sensor technology ourselves.

*S. Kemeny, N. Doudoumopoulos, E. Fossum, R. Nixon*
The Photobit Corporation Team (early 2000)
1995-2001 Photobit grows to about 135 persons
- Self funded with custom-design contracts from private industry
- Important support from SBIR programs (NASA/DoD)
- Later, investment from strategic business partners to develop catalog products
- Over 100 new patent applications filed
- Nov 2001 Photobit acquired by Micron Technology
The Technology Develops a Life of its Own

DARTMOUTH

• Today, over 5 billion cameras are manufactured each year that use the CMOS image sensor technology we invented at JPL, or more than 150 cameras per second, 24/365.
• Semiconductor sales of CMOS image sensors are over $13B/yr in 2018.
• Thousands of engineers working on this around the globe.
• Caltech has successfully enforced its patents against all the major players.
• NASA is now just adopting the technology for use in space (e.g. Mars 2020).

16Mpix camera modules
From Sony ~2012

Endoscopy Camera
From Awaiba ~2012
~$14B Semiconductor Sales in 2018
~5 Billion Cameras in 2018
2017 Queen Elizabeth Prize for Engineering

DARTMOUTH

Eric Fossum
Nobukazu Teranishi
Mike Tompsett

CMOS image sensor
Pinned photodiode
CCD image sensor
+ George Smith CCD

Buckingham Palace Reception
December 2017

For the creation of digital imaging sensors
QUANTA IMAGE SENSOR
Group at Dartmouth

L-R: Song Chen, Saleh Masoodian, Rachel Zizza, Zhaoyang Yin, Donald Hondongwa, Wei Deng, Dakota Starkey, Eric Fossum, Jiaju Ma, Leo Anzagira
Photon-Counting Image Sensor Concept

Image reconstruction
X-Y-t Bit Density ➔ Gray Scale

Vision: A billion jots readout at 1000 fps with single photon-counting capability (1Tb/s) and consuming less than a watt.
1. How to make a tiny sub-diffraction-limit (SDL) pixel (< 500nm) with deep sub-electron read noise in a mainstream process?

2. How to readout a very large array of binary pixels or jots at 1000 fps with less than 1Watt power?

3. How do you process the jot data to create pixels?
Photoresponse as Bit Density

Bit Density $D \triangleq \frac{M_1}{M} = 1 - e^{-H}$
Issues with Single Photon Avalanche Detectors (SPADs) for QIS Application

SPADs use avalanche multiplication for gain

- High internal electric fields
- Higher operating voltages (15-20V)
- Larger pixels (8-25um)
- High dark count rates (100-1000Hz)
- Dead time
- Low fill factor (low PDE <50%)
- Low manufacturing yield
- Small array sizes (below 0.1M jots)
Our Approach

Use very low capacitance sense node

$$\Delta V = \Delta Q / C$$

$$1\text{mV} = 1.6\times10^{-19} / 0.16\text{fF}$$

One pixel
Voltage Output with No Electronics Noise

Poisson probability mass function

\[ P[k] = \frac{e^{-H} H^k}{k!}, \quad k = 0, 1, 2, 3 \ldots \]

CG = conversion gain = \( \frac{q}{C} \) \([\text{V/e-}]\)
Broadened by 0.12e- rms read noise

\[ U_n = \frac{V_n}{CG} \quad [e-\text{rms}] \]
Broadened by $0.25e^{-}$ rms read noise

![Graph showing probability density against voltage/charge gain (electron number).]
Quantized Values Broadened by Readout Noise

![Graph showing Poisson distribution with various RMS values](image)

**Single-bit QIS**

- **“0”**
- **“1”**

**Diagram Details**

- Voltage/CG = Electron Number
- Probability Density
- Poisson Distribution
  - 0.12e rms
  - 0.15e rms
  - 0.25e rms
  - 0.35e rms
  - 1.0e rms
Pump-Gate Jot: Minimize TG-FD Overlap Capacitance

Highest possible CG (Lowest possible cap.)
Experimental Data
Photon Counting Histograms

20k reads of same jot, 0.175e- rms read noise ~21DN/e- (61.2uV rms 350uV/e- or 0.45fF)
Room temperature, no avalanche, 20 CMS cycles, jot: TPG PTR BC
Experimental Data
Photon Counting Histograms

20k reads of same jot, 0.2e- rms read noise ~21DN/e-
Room temperature, no avalanche, 20 CMS cycles, jot:TPG PTR BC
Read Noise and Photon-Counting Error

![Graph showing bit density vs. quanta exposure with different theoretical and experimental data points.](image)

- **Read Noise 0.26e- Theory**
- **Read Noise 0.24e- Theory**
- **Read Noise 0.22e- Theory**
- **Read Noise 0.17e- Theory**
- **Read Noise 0.15e- Theory**
- **Experimental Data 16k Jots**
- **Experimental Data Single Jot**
Dark Current

Room Temp: $\sim 0.16 \text{e-}/s \text{ avg.} (\sim 2 \text{pA/cm}^2)$
Previously measured $\sim 2 \times$ every 10C

Storage well isolated from surface

Ma, Masoodian, Wang, Fossum 2017
Ma, Anzagira and Fossum IEEE JEDS 4(2) 2016
Quantum Efficiency

QE data courtesy of Gigajot
Stacked BSI CIS Using Wafer Bonding

Detector Layer

Wafer Bonding Connection

Circuit Layer

Sony IMX260 dual pixel AF sensor from Samsung S7 teardown

Newly developed Stacked BI-CIS

Pixels

DRAM

Logic process substrate (Si)

Sony 2017 ISSCC
Two or more stacked layers
- A group of jots form a cluster
- Readout circuits of a cluster of jots are located underneath cluster
- Clusters function in parallel
- Column line length is reduced, parasitics are reduced
Prototype 1Mjot 1040fps QIS (1b Digital Output)

- Process technology: CMOS BSI 45nm/65nm 2-layer Stacking
- Cluster-Parallel Architecture
- Readout Variation:
  - Analog
  - Single-bit Digital
- Resolution: 1024x1024
- Jot pitch size: 1.1µm
- Jot types:
  - Tapered-reset Pump-Gate (TPG)
  - Punch-Through Reset (PTR)
  - JFET SF

16x16=256 clusters
4096 jots in each cluster
8 CDS units and a 1b-ADC in each readout cluster
Digital and Analog Readout Organization

(a) DIGITAL High speed

(b) ANALOG Low speed
1Mjot Prototype QIS Experimental Results

1Mpixel QIS photon-counting binary image sensor operating at 1040fps
## Summary of Measured Results

<table>
<thead>
<tr>
<th>Process</th>
<th>45nm (jot layer), 65nm (ASIC layer)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>1.8V &amp; 2.5V (Analog, digital and array), 3V &amp; 2.2V (I/O pads)</td>
</tr>
<tr>
<td>Jot type</td>
<td>BSI Tapered Pump Gate 2-Way Shared RO</td>
</tr>
<tr>
<td>Jot pitch</td>
<td>1.1µm</td>
</tr>
<tr>
<td>BSI Fill Factor</td>
<td>~100%</td>
</tr>
<tr>
<td>Quantum Efficiency</td>
<td>79% @ 550nm</td>
</tr>
<tr>
<td>Conversion gain on column</td>
<td>345µV/e-</td>
</tr>
<tr>
<td>Input Referred Noise</td>
<td>0.22e- r.m.s.</td>
</tr>
<tr>
<td>Corresponding BER</td>
<td>~1%</td>
</tr>
<tr>
<td>Avg. Dark current (RT)</td>
<td>0.16e-/s</td>
</tr>
<tr>
<td>Equiv. Dark Count Rate (RT)</td>
<td>0.16Hz/jot</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Equiv. PD Dead Time</th>
<th>&lt;0.1%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array</td>
<td>1024 (H) x 1024 (V)</td>
</tr>
<tr>
<td>Field rate</td>
<td>1040fps</td>
</tr>
<tr>
<td>ADC sampling rate</td>
<td>4MSa/s</td>
</tr>
<tr>
<td>ADC resolution</td>
<td>1 bit</td>
</tr>
<tr>
<td>Output data rate</td>
<td>32 (output pins) x 34Mb/s = 1090Mb/s</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Package</th>
<th>PGA with 224 pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td></td>
</tr>
<tr>
<td>Array</td>
<td>2.3mW</td>
</tr>
<tr>
<td>256 ADCs</td>
<td>7.5mW</td>
</tr>
<tr>
<td>Addressing</td>
<td>4.1mW</td>
</tr>
<tr>
<td>I/O pads</td>
<td>3.7mW</td>
</tr>
<tr>
<td>Total</td>
<td>17.6mW</td>
</tr>
<tr>
<td>FOM ADC</td>
<td>6.9pJ/b</td>
</tr>
</tbody>
</table>

\[
FOM = \frac{\text{Power Consumption}}{\# \text{ of pixels} \times \text{frame rate}} \left[ \frac{pJ}{b} \right]
\]
Gigajot spinoff (2017)

Dr. Saleh Masoodian

Dr. Jiaju Ma

Dr. Eric R. Fossum
1Mpixel 3b QIS Image
Exposure of 0.87e-/pixel average

Raw image and Histogram

2x2x2 cubicle sum only

2x2x2 cubicle denoise
Comments on
VERY HIGH SPEED IMAGE SENSORS
What is High Speed?

• Old Target circa 1995
  • 1Mpix @ 1Kfps
  • Continuous Readout
  • 1Gpix/s @10b

• New Target 2019 (?)
  • 1Mpix @ 100K+fps
  • Continuous Readout
  • 100Gpix/s @ 10+b
Issues

- **Pixel Size, QE, and Charge Transport**
  - Higher frame rate, fewer photons per frame
  - Thicker material, better QE, worse charge transport
  - Larger pixel, larger aperture, more photons
  - Larger pixel, longer charge transport distance
    - $T \sim L^2$ or at best $L$
  - Global Shutter vs. Rolling Shutter
Issues

• On-chip Analog-to-Digital Conversion (ADC)
  • Chip area per ADC v. pixel pitch
  • 3D Stacking for Pixel-Parallel or Cluster-Parallel
  • How many bits? 1,2,3….16b
  • Conversion cycles – SA if resolution <= 6b
  • Power dissipation limits
    • 1Mpixel @ 1uW/pix = 1W
    • Energy/conversion related to ADC resolution
Issues

- On-chip data reduction and off-chip readout
  - Mostly pertains to continuous mode readout
  - Power dissipation is critical, pad count is limited.
  - $1\text{Mpixel} @ 100\text{Kframe/s} = 0.1 \text{Tpixel/sec} = 1 \text{Tb/sec}$ for $10\text{b} \text{ADC}$
  - For sparse illumination can reduce number of pixels read out.
  - Compressive sensing might help but not if data spans full space of values.

- Image data must be received, and stored at same data rate – also a problem.
Issues

• Architecture
  • Continuous mode
    • 1Mpixel @ 100Kframe/s = 0.1Tpixel/s data rate (!)
  • Burst mode
    • 1Mpixel @ 1Gframes/s x m frames on-chip storage (ok)
In-pixel transport

**Figure 3:** Photodetector construction and operation.

**Figure 4:** Charge decay in photodetector.
Pixel data buffer storage

Off-chip readout architecture

Figure 1: Architecture of 2x2 pixels.

Figure 2: Imager block diagram.

- Number of pixels: 4x180x180
- Pixel size: 50x50μm²
- Fill factor: 13.5%
- CCD elements per pixel: 30
- Saturation signal, Qmax: 11,000e/p
- Responsivity: 2.2μV/e
- Readout noise: 9rms e/p
- Dynamic range: 1200:1
- Maximum frame rate: 8.33x10⁶ frames/s
Burst Mode
Work led by Etoh at Kinki Univ
Continuous Readout circa 1998

PB1024 HIGH SPEED SENSOR

- 1024x1024 elements
- 10 μm x 10 μm pixel pitch
- 0.5 μm CMOS
- 1024 on-chip 8b ADCs
- 8 digital output ports (64 pins)
- Open architecture
- Power: 95 mW @ 60 fps
- Power: 270 mW @ 574 fps
- By far, world’s pixel rate record of ALL image sensors (CCDs and CMOS)

Krymski, Van Blerkom, Bock, Anderson 1998

Behind Every Great Digital Image

© 2000 E.R.Fossum, Photobit Corporation
Continuous Readout circa 2000

4Mpixel, 200 fps SENSOR

Technology 0.35um 2P3M CMOS
Format 2368x1728 (4.1Meg)
Frame rate 200 F/s @50 MHz mscik
Number of outputs 16x10bit
Data throughput 8.2 Gbit/s (820 Mpix/s)
Number of pins 273 (280PGA package)
Pixel pitch 7um
Shutter type rolling
Conversion gain >10 uV/e
Quantum Efficiency 30%
ADC, 2368 x1 10bit (9 bit accuracy)
Dark FPN, rms 2 mV
PRNU at 1/2 Sat <2%
Temporal Noise <100e
Power supply 3.3V
Power consumption <800mW

Behind Every Great Digital Image
<table>
<thead>
<tr>
<th>Model</th>
<th>Resolution</th>
<th>Pixel Size</th>
<th>Format</th>
<th>Frame Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>LUX2100</td>
<td>2.1 Megapixel</td>
<td>10.0µm</td>
<td>4/3&quot;</td>
<td>1920 x 1080 @ 1,000 FPS</td>
</tr>
<tr>
<td></td>
<td>1952 x 1096</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LUX1310</td>
<td>1.3 Megapixel</td>
<td>6.6µm</td>
<td>2/3&quot;</td>
<td>1280 x 1024 @ 1,070 FPS</td>
</tr>
<tr>
<td></td>
<td>1280 X 1024</td>
<td></td>
<td></td>
<td>640 x 512 @ 4,168 FPS</td>
</tr>
<tr>
<td>LUX1310S</td>
<td>1.3 Megapixel</td>
<td>6.6µm</td>
<td>2/3&quot;</td>
<td>1280 x 1024 @ 267 FPS</td>
</tr>
<tr>
<td></td>
<td>1280 X 1024</td>
<td></td>
<td></td>
<td>640 x 512 @ 1,045 FPS</td>
</tr>
</tbody>
</table>

**2000Mpix/s**

**3600Mpix/s**

See also, CMOSIS (AMS)
A 5 Megapixel, 1000fps CMOS Image Sensor with High Dynamic Range and 14-bit A/D Converters

Table 1: key specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel array</td>
<td>2240 x 2240</td>
<td></td>
</tr>
<tr>
<td>Interface</td>
<td>Serial LVDS</td>
<td></td>
</tr>
<tr>
<td>Frame Rate</td>
<td>1000fps</td>
<td></td>
</tr>
<tr>
<td>Data Rate</td>
<td>70Gbps</td>
<td></td>
</tr>
<tr>
<td>Main power supply</td>
<td>1.8 &amp; 3.3 V</td>
<td></td>
</tr>
<tr>
<td>Full well</td>
<td>20 ke-</td>
<td></td>
</tr>
<tr>
<td>Temporal noise</td>
<td>5 e-</td>
<td></td>
</tr>
<tr>
<td>QE</td>
<td>&gt;50%</td>
<td>@633nm</td>
</tr>
<tr>
<td>MTF</td>
<td>63%</td>
<td>@633nm</td>
</tr>
<tr>
<td>DR</td>
<td>72dB</td>
<td>Intra-scene</td>
</tr>
<tr>
<td>ADC resolution</td>
<td>14-bit</td>
<td>12-bit ENOB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>after rescaling</td>
</tr>
</tbody>
</table>

5000Mpix/s

Vision Research
Phantom Camera

v2512

The Phantom v2512 is the maximum speed available with 25 Gpx of throughput. Our highly sensitive, proprietary CMOS sensor combines with easy data management to produce clear images when speed is critical.

- 25,700 fps at 1280 x 800
- Exposure Index Range:
  - Mono 32,000 – 160,000
  - Color 6,400 – 32,000
- 72, 144, or 288GB RAM
- 10Gb Ethernet and up to 8TB CineMag

~26,000Mpix/s 12b according to website

https://www.phantomhighspeed.com/products/cameras/ultrahighspeed/v2512
ISSCC 2018 / SESSION 5 / IMAGE SENSORS / 5.1

5.1 A Back-Illuminated Global-Shutter CMOS Image Sensor with Pixel-Parallel 14b Subthreshold ADC

Sony

Process

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CIS wafer: 90nm 1 Poly 4 Metal Layer</td>
<td></td>
</tr>
<tr>
<td>Logic wafer: 65nm 1 Poly 7 Metal Layer</td>
<td></td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>2.9 [V] / 1.1 [V]</td>
</tr>
<tr>
<td>Num. of pixels</td>
<td>1632^H x 896^V</td>
</tr>
<tr>
<td>Pixel size</td>
<td>6.9 [μm] x 6.9 [μm]</td>
</tr>
<tr>
<td>Output interface</td>
<td>16ch x 4.752 [Gbps/ch] SLVS-EC</td>
</tr>
<tr>
<td>Max frame rate</td>
<td>660 [fps]</td>
</tr>
<tr>
<td>Saturation signal</td>
<td>16.6k [e-]</td>
</tr>
</tbody>
</table>

~1000 Mpix/s, ~750mW, 14b
Acknowledgments for QIS Part

• Dartmouth graduate students
  • Ma, Masoodian, Starkey, Deng, Zizza, Anzagira, Hondongwa, Song
• Faculty colleagues
  • Odame, Liu, Chan
• Rambus
  • Endsley, Stark, Guidash
• TSMC
  • Wei, Yamashita, Wang
• DARPA DETECT (a little bit)

The END