Trends in ultra fast silicon trackers

A. Rivetti - INFN Torino

Thanks to contribution by:
N. Cartiglia, L. Demaria, M. Mandurrino, E. Monteil, J. Olave, L. Pacher, L. Pancheri, M. Rolo
Future accelerators under study - energy frontier

Lepton colliders

- ILC
- CLIC
- FCC/e+e-
- CEPC

- Vertex/tracking detectors require:
  - Very good spatial resolution \( \mathcal{O}(\mu m) \)
  - Very low material budget (0.15% \( X_0/\text{layer} \))
  - Moderate time resolution
  - Moderate radiation hardness (1 Mrad TID, \( 10^{12} \) eq. neutrons)
- Vertex detector: silicon
- Main tracker: silicon or TPC

  • Very precise

Hadron colliders

- HE-LHC
- FCC/pp
- SppC

- Vertex/tracking detectors require:
  - Very good spatial resolution \( \mathcal{O}(\mu m) \)
  - low material budget
  - Very good time resolution
  - Extreme radiation hardness
- Vertex detector: silicon
- Main tracker: silicon

• Very fast
Smaller and shorter term facilities can provide an ideal playground to test advanced detector concepts.
Relevant trends in sensors/electronics

- Fast data transmission
- Better time resolution
- Smaller pixels, more functionality
- CMOS sensors with even larger Q/C and charge collected by drift: DMAPS
- Stitching
- 3D/high density interconnect

Looking ahead – scaling!

- With the 65 nm process we cannot increase I/O speed beyond 10 Gbps
- 65 nm ok for HL-LHC, might be ok for HE-LHC, definitely not ok for FCC-hh (if any…)
- Industry has scaled down 6 times more…
- We cannot stand still, but going forward requires significant resources.

- Next promising technology is 28 nm.
- CMOS 28 nm is already being explored in back-end electronics (like FTK-Atlas-Phase2 project).
- INFN started since few years R&D projects exploring the 28nm node for front-end electronics (Scaltech28, then the Call TimeSpot) and CERN interest is growing. Preliminary results show that radiation hardness of 28 nm seems even higher than for 65nm.
- Also cost and access to the technology is improving.

- Below 28 nm, FINFET becomes the workhorse ⇒ FINFET16-V2.
Fast data transmission

Y. Frans et al.  
Better time resolution

**Single sample timing**

- Timing pulse provided by a discriminator
- Leading edge or zero crossing (CFD)
- Simple and compact electronics
- Suitable for highly pixellated detectors
- Can be used to measure also charge

**Multiple sample timing**

- Waveform sampling
- Many opportunities for DSP
- Data throughput is an issue
- Higher power/lower density
H. Wang, F. F. Dai

A 14-Bit, 1-ps resolution, two-step ring and 2D Vernier TDC in 130nm CMOS technology

ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference

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**Many possible topologies**

- TDCs now hitting the ps barrier
- Much progress thanks to ADPLL

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**TDCs not the limiting component** in high resolution timing systems

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**TABLE I.**

<table>
<thead>
<tr>
<th></th>
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<tr>
<td>Process</td>
<td>Cyclic</td>
<td>Stochastic</td>
<td>SS-ADC</td>
<td>2D Vernier</td>
<td>SAR-ADC</td>
<td>Ring+2D Vernier</td>
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<tr>
<td>NoB</td>
<td>28nm</td>
<td>14nm</td>
<td>65nm</td>
<td>45nm</td>
<td>14nm</td>
<td>130nm</td>
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<td>ENoB (1)</td>
<td>12</td>
<td>10</td>
<td>6.1</td>
<td>8</td>
<td>7</td>
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<tr>
<td>ER (2)</td>
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<td>3.85ps</td>
<td>7.60ps</td>
<td>1.67ps</td>
<td>2ps (4)</td>
<td>1.74ps</td>
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<td>Speed [MHz]</td>
<td>10</td>
<td>100</td>
<td>40</td>
<td>80</td>
<td>26</td>
<td>10</td>
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<tr>
<td>DNL [LSB]/[ps]</td>
<td>0.5/0.32</td>
<td>0.8/0.94</td>
<td>---/---</td>
<td>0.25/0.31</td>
<td>---/---</td>
<td>0.41/0.41</td>
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<tr>
<td>INL [LSB]/[ps]</td>
<td>3.8/2.39</td>
<td>2.3/2.7</td>
<td>0.27/1.6</td>
<td>0.34/0.4</td>
<td>9/1.8</td>
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<tr>
<td>Power [mW]</td>
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<td>0.78</td>
<td>0.36</td>
<td>0.33</td>
<td>---</td>
<td>2.4</td>
</tr>
<tr>
<td>FoM (3)</td>
<td>0.02</td>
<td>0.01</td>
<td>0.13</td>
<td>0.02</td>
<td>---</td>
<td>0.02</td>
</tr>
</tbody>
</table>

1. ENoB = NoB – log2(INL+1).
2. Effective Resolution (ER) = Resolution × 2^((NOB – ENOB).
3. FoM = Power / (2^NOB × F_s) [pJ / conv-step].
4. calculated based on in-band phase noise. PN = 10log(2π²f²τ_m^2/12fₚ).
Timing uncertainties

Timing jitter

\[ \sigma_t = \frac{\sigma_n}{dV/dt} \approx \frac{v_n}{\sqrt{2}t_a} \frac{C_d}{Q_{in}} \sqrt{t_a^2 + t_d^2} = \frac{v_n C_d}{Q_{in}} \sqrt{t_d} \]

Eg: \( g_m = 30 \mu S, C_d = 100 \text{ fF}, Q_{in} = 1 \text{ fC}, t_d = 5 \text{ ns} \)
\( \sigma_t = 117 \text{ ps} \)

- \( Q/C \) very important also for good timing!

Time walk

- See also C. de la Taille lecture
- Eg: \( g_m = 30 \mu S, C_d = 100 \text{ fF}, Q_{in} = 1 \text{ fC}, t_d = 5 \text{ ns} \)
\( \sigma_t = 117 \text{ ps} \)
Shape related effects

- Pulse shape variations affect timing
- Detector and front-end co-design to predict reasonably timing performance
Constant fraction?

The input signal is both delayed and attenuated. The delayed and attenuated signals are combined to yield a bipolar waveform. The zero crossing of the bipolar waveform is used for timing.

**Jitter optimization:**

\[ t_{zc} = \frac{t_d}{1 - f} \]

\[ t_{zc} = \frac{t_d e^{\frac{t_d}{\tau}}}{e^{\frac{t_d}{\tau}} - f} \]
A 64-Gb/s 1.4-pJ/b NRZ Optical Receiver Data-Path in 14-nm CMOS FinFET
Front-end with 25 ps peaking time

\[ \frac{C_{i1}}{C_{i2}} = \frac{g_{m_p}}{g_{m_n}} = \frac{C_{o1}}{C_{o2}}. \]

A 64-Gb/s 1.4-pJ/b NRZ Optical Receiver Data-Path in 14-nm CMOS FinFET
In this design, the input node of the TIA is used as the negative output ($V_{outn}$) to serve as a different signal to the output node of the TIA ($V_{outp}$), rather than placing a replica TIA to generate a reference voltage [14], as shown in Fig. 10(b). As a result, the transimpedance gain becomes $R_{fb}$ instead of $R_{fb} \left[ A_{eq} / (A_{eq} + 1) \right]$, where $A_{eq}$ is equal to $g_m \left( R_{fb} \parallel R_{out} \right)$. This improvement is shown in Fig. 12. Both single-ended outputs and the differential voltage ($V_{outp} - V_{outn}$) are given in Fig. 12. Note that ($V_{outp} - V_{outn}$) is shifted to the right in order to match the sampling points for better comparison of the two cases. The main cursor [$V_{Tap}(0)$] of $V_{outp} - V_{outn}$ is larger than the main cursor of the single-ended output ($V_{outp}$), whereas $V_{Tap}(-1)$ and $V_{Tap}(2)$ are the same. Since $V_{Tap}(1)$ will be equalized by DFE, the increase in this ISI term does not degrade signal integrity.

Another advantage of using the self-referenced TIA is that it generates less noise compared with the replica design. In Fig. 13, three noise spectral densities (NSDs) are given. The red solid line is the NSD of the TIA with a replica with no filtering capacitor ($C_{FLT}$) at its output. Adding a 600 fF of $C_{FLT}$ shapes the NSD as indicated by the blue dotted curve. The green dashed curve is the NSD of the proposed self-referenced TIA. There are two main reasons for the reduction in noise. First one is that there is no replica to generate noise. Note that the replica generates as much noise as the TIA itself increasing the integrated noise by a factor of $\sqrt{2}$. High-frequency noise of the replica TIA can be filtered out by using a large capacitance at the output node. However, this would prevent the replica TIA from tracking the main TIA behavior for high-frequency supply disturbances compromising power supply rejection ratio (PSRR). The second reason for noise reduction is that in self-referenced TIA, the low-frequency noise components of the transistors are converted into common-mode noise. This explains why no flicker noise is observed in the NSD of the self-referenced TIA illustrated in Fig. 13.

To investigate the PSRR of the self-reference TIA, it is critical to separate the input and output capacitances connected.

- Power $O(10 \text{ mW})$ for 100 fF input capacitance
Again on LGAD

- No gain zone between pixel

- Homogeneous gain layer
- Small pixels

RSD ingredients:
1. Resistive cathode: freeze the signal
2. Cap oxide: couple the signal with pads
An example of timing chip

- Timing front-end ASIC: 1024 channels, 4096 TDC, 20 Gbit/s output bandwidth
- Technology 110 nm CMOS
- Pixel size $400 \mu m \times 400 \mu m$
- TDC binning $20 \div 100$ ps, DNL %
- Overall system jitter $\approx 30$ ps r.m.s.
System level issues

- Best achievable performance often compromised by system-level issues
- Verification, verification, verification
A 12-bit 150-MS/s Sub-Radix-3 SAR ADC With Switching Miller Capacitance Reduction

Kwuang-Han Chang, Member, IEEE, and Chih-Cheng Hsieh, Member, IEEE

<table>
<thead>
<tr>
<th>Comparison Table of the State-of-the-Art ADCs</th>
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<tbody>
<tr>
<td>Architecture</td>
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<tr>
<td>Technology</td>
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<tr>
<td>Supply Voltage</td>
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<tr>
<td>Resolution</td>
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<tr>
<td>Sampling Rate</td>
</tr>
<tr>
<td>SNDR @ peak (dB)</td>
</tr>
<tr>
<td>SFDR @ peak (dB)</td>
</tr>
<tr>
<td>SNDR @ Nyq (dB)</td>
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<tr>
<td>SFDR @ Nyq (dB)</td>
</tr>
<tr>
<td>DNL (LSB)</td>
</tr>
<tr>
<td>INL (LSB)</td>
</tr>
<tr>
<td>Power (mW)</td>
</tr>
<tr>
<td>FoMw @ peak (fJ/conv-step)</td>
</tr>
<tr>
<td>FoMw @ Nyq (fJ/conv-step)</td>
</tr>
<tr>
<td>Core Area (mm²)</td>
</tr>
</tbody>
</table>

*: ADC+Ref+Buf  **: ADC-only
ADCs in front-end electronics

K. Swientek
The SALT, a 128-Channel Readout ASIC for Upstream Tracker in the Upgraded LHCb Experiment
https://indico.cern.ch/event/608587/contributions/2614090/

- 6 bit ADC
- designed for LHCb upgrade
- 128 channels
Compact electronics

- Part of a pixel front-end demonstrator chip
- INFN project CHIPiX65, funded by INFN R&D committee
- Fully compatible with HL-LHC specifications (50 um x 50 um pixels)
- Full regional logic, two different front-ends (synch and asynch)
- Synchronous front-end with:
  - Dynamic offset compensation (no calibration DACs)
  - Fast charge digitisation with ToT
- Front-end size: 35 um x 35 um
Compact front-end electronics

- First front-end electronics for radiation detectors based on **switched-capacitor** circuits
- Maximum charge stored in a transistor in 65 nm about 5% of that of a 350 nm
- Charge injection greatly **reduced**
- Advanced **isolation** features
Positive feedback latch

- When the 40 MHz strobe signal moves high, this stage is able to compare the two inputs in a very short time (~200 ps).
- The power consumption is limited to transitions thanks to the XNOR gate.
- This kind of latch can be used only in a synchronous design.

Some circuit details:

- Differential Amplifier schematics
- VFE_1 version
- VFE_2 version
- Synchronous front-end architecture
- Torino INFN design group [JINST 11(2016), C03013]
- Telescopic-cascode CSA with Krummenacher feedback for linear Time-over-Threshold (ToT) charge encoding
- Synchronous hit discriminator with track-and-latch voltage comparator
- Threshold trimming by means of autozeroing using capacitors
- 40 MHz 4-bit ToT or 5-bit fast ToT counting with latch turned into a local oscillator (100-900 MHz)
- Efficient self-calibrations can be performed according to online machine operations
- Successfully tested (also after irradiation) using dedicated mini@sic small-prototypes

pacher@to.infn.it
ToT linearity

- Oscillation frequency: 320 MHz, but could be significantly higher (>> 1 GHz)
- Power primarily depends on number of cycles
- Number of bits primarily depends on data storage
- Mostly digital, good for scaling
Radiation performance

ToT frequency vs radiation

- Some degradation, but still functional after 600 Mrad
Test on larger system

- One of three front-end concepts tested in the RD53A chip
Some performance

- **Sr90 - self-triggered**

- **Occupancy** ($\Sigma = 556778$)

  - S-curves for 24576 pixel(s)
  - Threshold distribution
  - Noise distribution

- **Cluster size**

  - Mean noise $\sim 77$ e-
  - Noise dispersion $\sim 6$ e-
  - Thr dispersion $\sim 76$ e-

- **Cluster size**

  - Mean noise $\sim 77$ e-

A. Rivetti
• Fast TDC/oscillators can also be shared among pixels (e.g. Timepix3, Timepix4)
Fully depleted MAPS

Sensors with Embedded Electronics Design (SEED)

Supported by INFN R&D Committee

A. Rivetti

ULITIMA 2018 -Argonne National Lab
The in-pixel electronics

- **Analog gain = 1/C_f**
- Analog buffer based on a switched OP amp amplifier → high dynamic range
- The calibration system: test pulse injection and baseline regulation

**Analog electronics**

**Analog in-pixel electronics**

- **Calibration**
- **CSA**
- **Analog buffer**
Test structures
Some results

- Several test structures with different guard-ring design
- Inversion layer may compromise guard-rings
- Can be partially cured with irradiation
- Cause understood and fixed in the next release just delivered by the foundry
Non-depleted matrix

At 100 V the leakage current injected to all the channels generates the saturation of the whole matrix.

At 110 V the depletion region reaches the topside. First, the pixels in the middle see the effect of depletion. External pixels still receive a high leakage current.
Fully depleted matrix

- At 100 V the leakage current injected to all the channels generates the saturation of the whole matrix.
- At 110 V the depletion region reaches the topside. First, the pixels in the middle see the effect of depletion. External pixels still receive a high leakage current.
- For voltages higher than 140 V, the channels do not see any leakage current at the input transistor.
- Parasitic currents along the chip edge have been observed. They are collected by the guard ring built around the matrix array.
C-V and I-V curve

- In full depletion, total matrix capacitance is 2.7 pF
- I-V curve: few nA up to 180 V
- Maximum voltage before breakdown 240 V
Uniformity and noise

CMIV distribution

<table>
<thead>
<tr>
<th>CMIV FIT</th>
<th></th>
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<tbody>
<tr>
<td>Entries</td>
<td>600</td>
</tr>
<tr>
<td>Mean</td>
<td>824.8</td>
</tr>
<tr>
<td>RMS</td>
<td>5.766</td>
</tr>
<tr>
<td>$\chi^2$/ndf</td>
<td>11.36/8</td>
</tr>
<tr>
<td>Constant</td>
<td>146.8 ± 7.6</td>
</tr>
<tr>
<td>Mean</td>
<td>824.7 ± 0.2</td>
</tr>
<tr>
<td>Sigma</td>
<td>5.627 ± 0.179</td>
</tr>
</tbody>
</table>

Common mode input voltage

• Depletion and punch through voltage correlated with the common mode input voltage (CMIV)
• Expected from simulations 820 mV.
• Measured (824 ± 6) mV
• FWHM depends on the input transistor size (mismatch). Good agreement with simulations (4 mV)

2D maps shows a good uniformity among the pixel matrix

Electrical tests (II): Noise

• Noise is measured as the standard deviation of the baseline distribution
• All the sectors have similar noise performances
• Noise = 420 ADC (50 electrons)
• Whenever are observed problems with the sensor, noise is higher (sample 2)

All sectors

More samples
Digitally induced noise

- Good separation between analog and digital circuits

![Graph showing analog noise vs frequency](image)

- Fast digital signal injected to the digital logic of the pixel with frequencies up to 1.6 MHz
- Noise at the output of the analog chain is measured to identify any kind of noise injection
- Measurements show a negligible effect of the digital part in the analog performance
- The analog circuitry is well isolated by the digital circuitry built on the pixel cell
With lasers and X-rays

**Unfocused pulse**

- Laser measurements
  - The metal fillers of the channel have been designed so that the pixel centre is left free for optical measurements.
  - A laser of wavelength 1060 nm has been used for the measurements.
  - Good noise suppression in those pixels where there is no signal.

**Laser measurements**

- Measurements with 55 Fe
  - The four sectors exhibit very similar analog gain.
  - The measurement has been used to calibrate the analog gain to 116 mV/fC.
  - FWHM is 1300 eV, which is not enough to see the secondary peak. More statistics are required.

**X-rays measurements**

- Calibration made by means of the facility for total dose RP-149 Semiconductor Irradiation System.
- A monochromator has been used to get a monochrome spectrum.
- Two energies selected: 7 KeV and 8.7 KeV.
- Measured with Amptek XR-100CR and MATISSE.
5.1 A Back-Illuminated Global-Shutter CMOS Image Sensor with Pixel-Parallel 14b Subthreshold ADC

Masaki Sakakibara¹, Koji Ogawa¹, Shin Sakai¹, Yasuhisa Tochigi¹, Katsumi Honda¹, Hidekazu Kikuchi¹, Takuya Wada¹, Yasunobu Kamikubo¹, Tsukasa Miura¹, Masahiko Nakamizo¹, Naoki Jyo¹, Ryo Hayashibara¹, Yohei Furukawa¹, Shinya Miyata⁵, Satoshi Yamamoto¹, Yoshiyuki Ota¹, Hirotsugu Takahashi¹, Tadayuki Taura¹, Yusuke Ōike¹, Keiji Tatsani¹, Takashi Nagano¹, Takayuki Ezaki¹, Teruo Hirayama¹

¹Sony Semiconductor Solutions, Atsugi, Japan
²Sony Semiconductor Manufacturing, Kumamoto, Japan
³Sony LSI Design, Fukuoka, Japan

Figure 5.1.1: Simplified block diagram of pixel-parallel ADC.

digital signal to and from an IC. The signal level is converted into a voltage at the A/D converter, and is stored in SRAM as a digital signal. The digital signal is then read from SRAM through the repeater.

Figure 5.1.2 shows the timing waveform for the pixel operation. The timing waveform is shown for each stage of the ADC. The initial value of the ADC is set to 0, and the value is updated during the reading period. The reading period is divided into 15 periods, and the value is updated during each period. The value is then stored in SRAM as a digital signal.

Figure 5.1.3 shows the micrograph of the chip. The chip is composed of a 1.46-Mpixel 14b subthreshold ADC, which is connected to the IC via a bonding interface. The chip is composed of 128 ADCs, which are connected in parallel. The ADCs are connected to the IC via a bonding interface.

Figure 5.1.4 shows the captured image, demonstrating that the pixel-parallel ADC is working correctly. The captured image is composed of 896 pixels, which are connected in series. The image is captured by the pixel-parallel ADC, and is stored in SRAM as a digital signal.

Figure 5.1.5 summarizes the performance of the pixel-parallel ADC. The performance is evaluated using the following figure-of-merits (FOMs):

- FOM1: Power consumption of the ADC
- FOM2: Time average of the operation current of 7.74nA

The best performance of FOM2 is achieved at a current of the CM can be turned off, thus reducing the average power consumption. As a result, the time average of the operation current of 7.74nA is achieved.

Figure 5.1.6 shows the performance comparison of the pixel-parallel ADC with other ADCs.

Figure 5.1.7: Die micrograph and the part of cross-section.
CMOS sensors for tracking are making very good progress

- 2-layer devices for high-density, high-speed environments
- 1-layer sensor for outer layers
- Power likely to be limited by data transfer
- Very good perspective for timing trackers...but devil is the details