A new front end electronics interfacing in the ATLAS experiment

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May 17, 2016
Young Scientist Symposium Series
What is FELIX?

- **FrontEnd LInk eXchange**

- A project name of ATLAS DAQ for the phase 1 & 2 upgrade

- **A router** to interface with various type of frontend readout electronics

- FPGA cards + server PC + network cards + software IOC
ATLAS DAQ

Custom electronic components

Point-to-point S-links

~100 servers

~100 kHz / ~200 GB/s

~1800 links

~1500 servers

FrontEnd

ReadOut Driver

ReadOut System\(^1\) (Data Buffer)

Ethernet

High-Level Trigger Farm

HLTPU

HLTPU

HLTPU

HLTPU

HLTPU

3

PCs (COTS)

\(^1\)Including FPGA PCIe card

Custom server PC

Custom

Run 2

2015

2017

2019

2021

2023

2025
ATLAS DAQ

GBT-links

Infiniband, 40Gb ethernet

HPC Network

ROD

sROD

ROS

HLTPU

Custom server PC

Custom electronic components

PCs (COTS)

*Including FPGA PCIe card
ATLAS DAQ

High-Level Trigger Farm

HPC Network

~10,000 links

~200 system

Less than 10 TB/s

40 MHz

2015
2017
2019
2021
2023
2025
Run 4

Custom
server PC

HLTPU
HLTPU
HLTPU
HLTPU
HLTPU
HLTPU
HLTPU
HLTPU
HLTPU
HLTPU

PCs (COTS)
Requirement for FELIX

- Use more commercial products (Commercial Off The Self)
- High speed link (max: 10Gb/s)
- Forwarding LHC clock and L1 trigger (TTC) to FE data
- Distinguishable for each detector channel
- Various, configurable bandwidth per channel
FELIX : server PC + FPGA card + NIC

- **FELIX Card (FLX)**: TTC FMC, TTC decoder, PCIe Engine, Control/Monitor, GBT Wrapper, Central Router, Housekeeping, Optical Links.
- **Memory**: Large Buffers per group of E-links.
- **PCIe Gen-3**: 64 Gb/s.
- **CPU**: DMA, MSI-X, Custom Device Driver.
- **FELIX Application**.
- **NIC**: 64 Gb/s, 2 – 4 40-Gb/s ports.
- **Optical Links**.

FELIX : server PC + FPGA card + NIC

7
Development: firmware + software

FELIX Card (\(\Gamma\)lx)
- TTC FMC
- TTC decoder
- PCIe Engine
- Control/Monitor
- GBT Wrapper
- Central Router
- Housekeeping

Optical Links

FELIX PC
- NIC
  - 2 – 4 40-Gb/s ports
  - Optical Links
- PCIe Gen-3
  - 64 Gb/s
- CPU
  - DMA
  - MSI-X
  - Custom Device Driver
  - FELIX Application

Memory
- Large Buffers per group of E-links

TTC decoder
- PCIe Gen-3
- 64 Gb/s

Control/Monitor
- Central Router
- Housekeeping

Development: firmware + software
FELIX development cards

FLX-710 (FELIX)
- HiTech Global HTG-710
- Virtex-7 X690T
- PCIe Gen 3 x 8 lanes
- 2x12 bidir CXP connectors
- FMC connector

FLX-709 (MiniFELIX)
- intended for FE development support
- Xilinx VC-709
- Virtex-7 X690T
- PCIe Gen 3 x 8 lanes
- 4 SFP+ connectors
- FMC connector

TTCfx v1, v2 and (v3)
- Custom FMC accepting TTC input
- Outputs TTC clock and CH A-B info
- V1: ADN2814 + CDCE62005
- V2: ADN2814 + Si5338
FELIX firmware block diagram

E-link: a data packet protocol defined by header and tail bytes, could be various in length
Workscope

For FELIX softwares:
Firmware status

- All sub-modules are functioning
  - TTC decoder recovers L1 trigger and TTC data correctly
  - 8 channels of GBT link tested with local loop back
  - PCIe DMA throughput reached maximum performance
  - Central Router with 4 channel configuration works
- Full chain test is complete
- Forwarding TTC clock and L1 trigger to FE is done
- Firmware is available for HTG-710(8ch) and VC-709(4ch)
Software status

- Low level tools and debugging tools
  - Board communication and control
  - Data flow control and check
  - Performance testing
- QT based GUI for various configuration and control
- Documenting software

loopback via GBT links of data from internal generator
To be done

- In general, bug fix

- System level test
  - integration test with FELIX-wares + FE electronics
  - demonstration of TTC busy
  - demonstration of “full mode” (10Gb/s)
Back up slides
FELIX “GBT-FPGA” is based on CERN GBT-FPGA, with some changes:

- Ported to Xilinx Vivado
- Transceiver independent (Xilinx GTH, GTX, etc.)
- Support for quads (4 transceivers + PLLs) and a parametrized number of quads
- Run-time choice of GBT Normal (FEC) mode, GBT Wide mode, “Full mode”
  - “Full mode” is a FELIX addition: 9.6Gb/s byte stream (encoding TBD)
- Lower (fixed) latency (worst cases: Tx 57.1 ns; Rx FEC 63.2ns; Rx Wide 50.7 ns)

- **Input/output Interfaces:** 120-bit registers clocked at 40MHz
Data block and E-link packet

**block header:**
- E-link ID (11 bits)
- sequence number (5 bits)
- Start-Of-Block symbol (16-bits)

**fragment trailer**
- first/last/both/middle/null (3 bits)
- flags: xfer error, trunc, rsrvd, rsrvd (4 bits)
- fragment length in 16-bit words

E-link packet = chunk

1 kB block

* 1 kB blocks of other E-links
Tools for development

- develop and maintain three platforms
- Subversion
- HDL Works Ease for schematic design entry of HDL blocks
- Xilinx Vivado and tcl scripts
- Mentor Graphics Questasim and tcl scripts
- Code Documentation with Latex and Doxygen
- Python scripting and Jinja2 for Register Map to synchronize:
  - HDL register definition (VHDL)
  - Application software (C++) and OKS (xml)
  - Documentation (tex)
- Ecosystem of low level software tools for development and debugging
- QT based GUIs to control and configure hardware