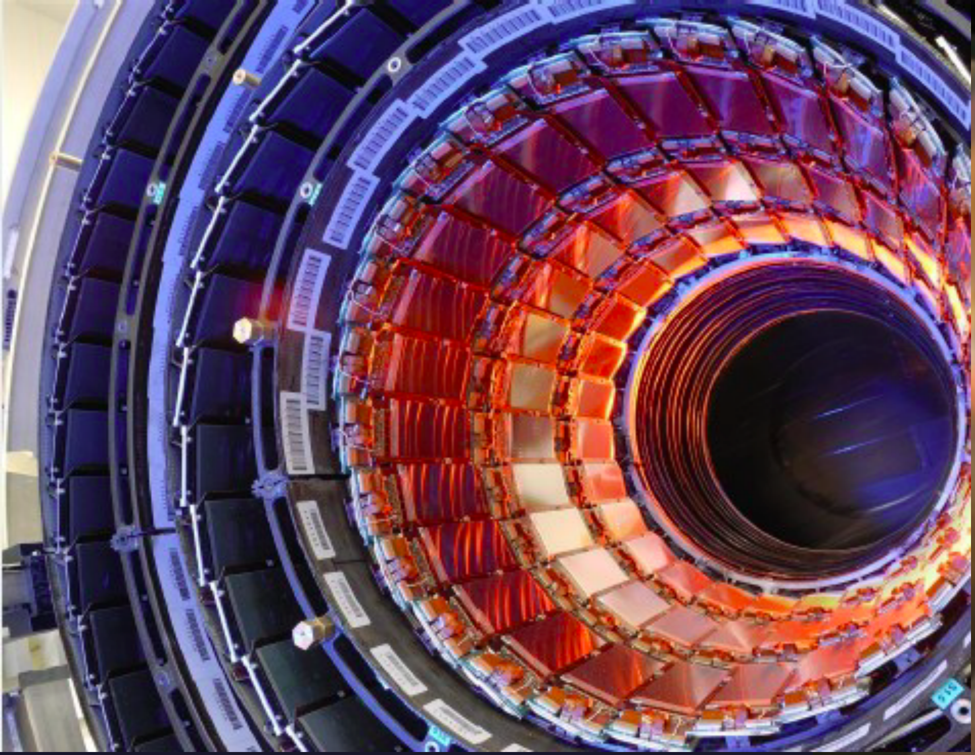


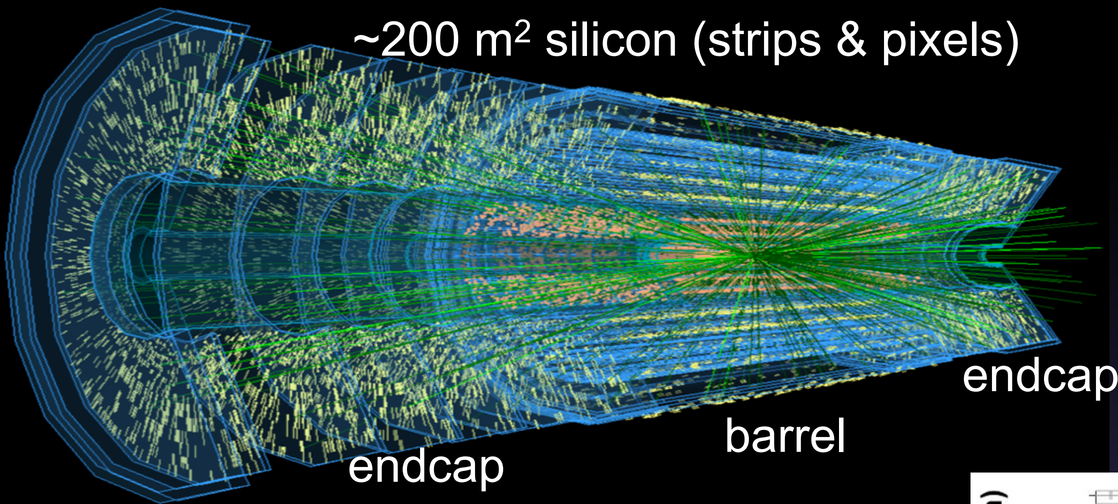
# Tracking

- Fundamental issues in tracking
- Silicon detectors and their applications
- New ideas and developments for the HL-LHC

**D. Bortoletto University of Oxford**

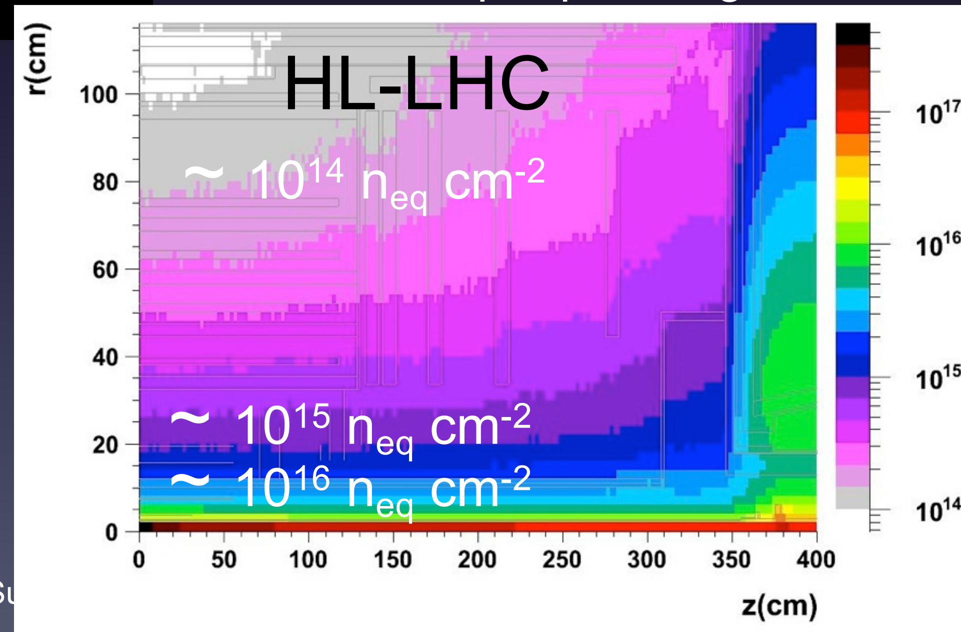
# HL-LHC tracker upgrades

- New all-silicon trackers for ATLAS and CMS



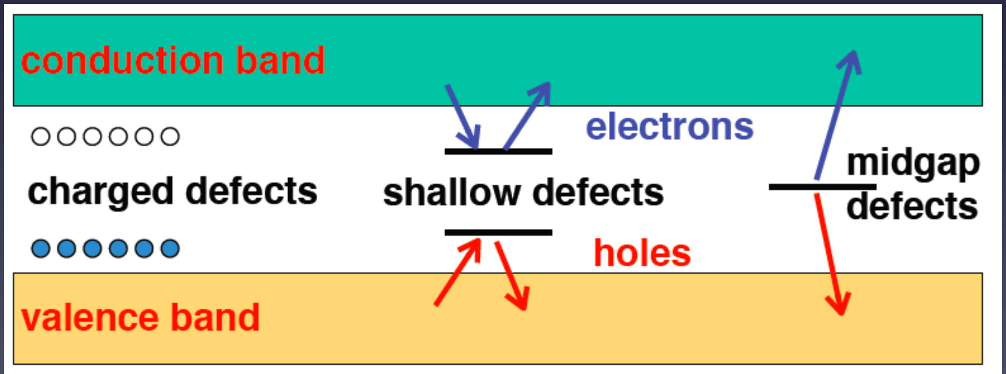

- Increased luminosity and track rate require:
  - Larger area
  - Higher hit-rate capability
  - Increased granularity
  - Higher radiation tolerance
  - Lighter detectors
  - Cheaper price tag !!

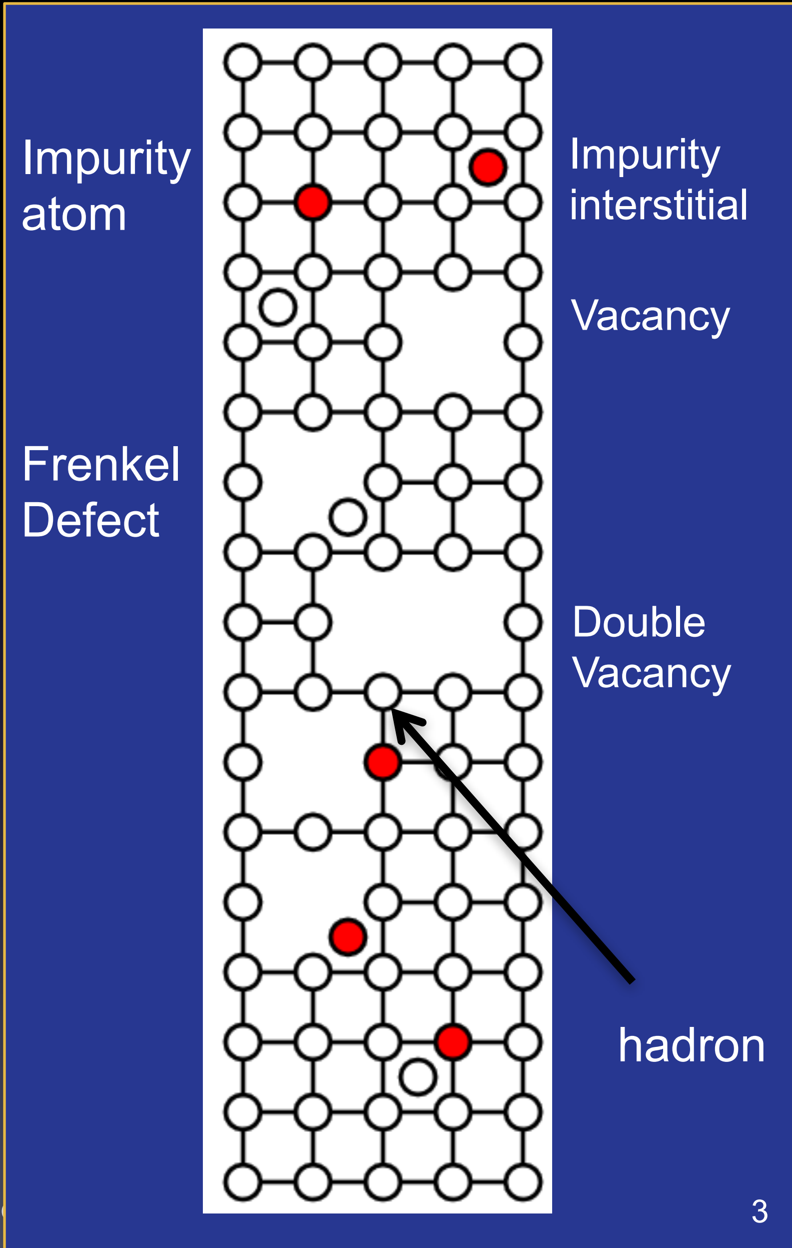
- Radiation hardness and rate performance must increase compared to LHC Run I
  - Run 2 (2015) ≈ x5
  - Run 3 (2018) ≈ x 5-10
  - HL-LHC (>2025) ≈ x 10-30
- In the inner pixel layers:
  - $10^{16}$ $n_{eq}$ $cm^{-2}$ and TID > 1 Grad



# Radiation damage due to NIEL

- Atomic displacement caused by massive particles (p,n,π)
  - Charge defects ➔ change of effective doping concentration ➔ increase $N_{eff}$ (= $N_D - N_A$) and depletion voltage
  - Shallow defect: Trapping centers created ➔ trapping of signal charge
  - Midgap defects: generation/recombination levels in band gap➔ increase of leakage current

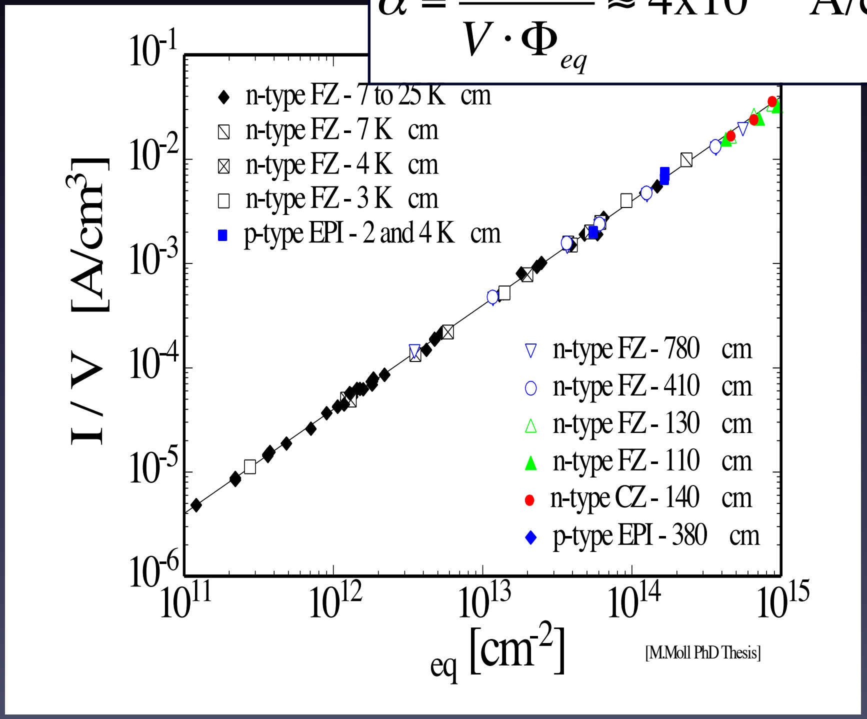


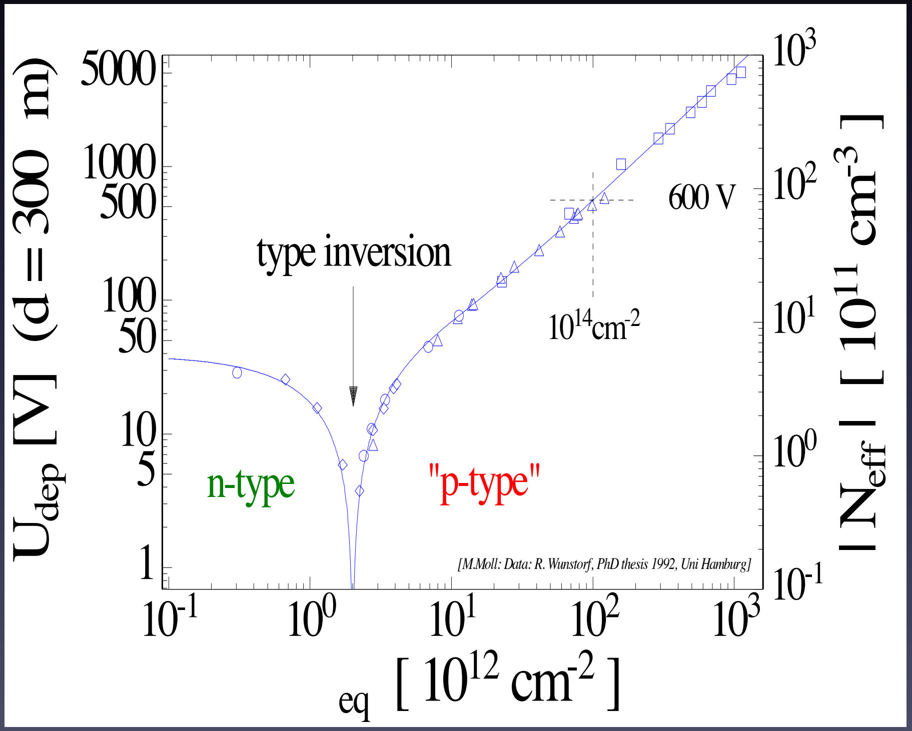



# Radiation damage due to NIEL

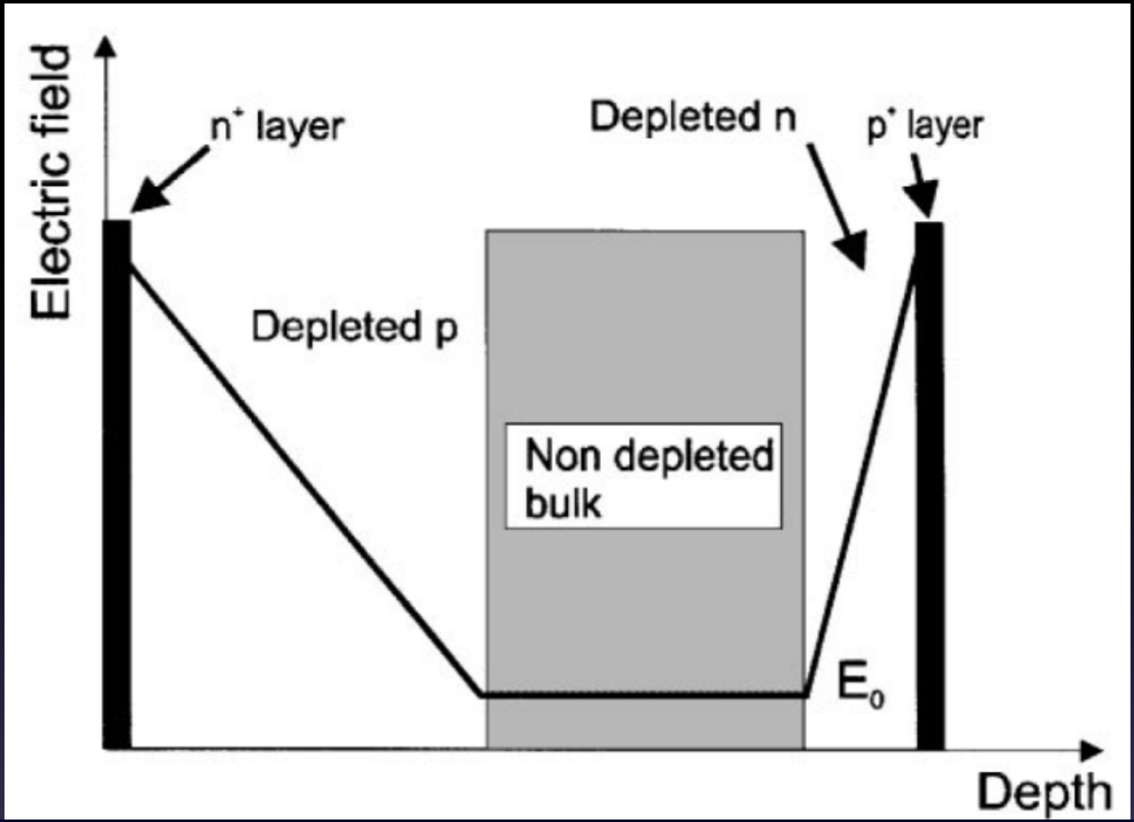
- Change in $I_{leak}$
  - increased noise
  - increased power
  - thermal runaway
  - increased cooling
  - increased material
- change in $N_{eff}$
  - "type inversion"
  - "reverse annealing
  - need higher $V_{bias}$
  - op. in partial depletion

$$\alpha = \frac{\Delta I}{V \cdot \Phi_{eq}} \approx 4x10^{-17}\ \text{A/cm}$$



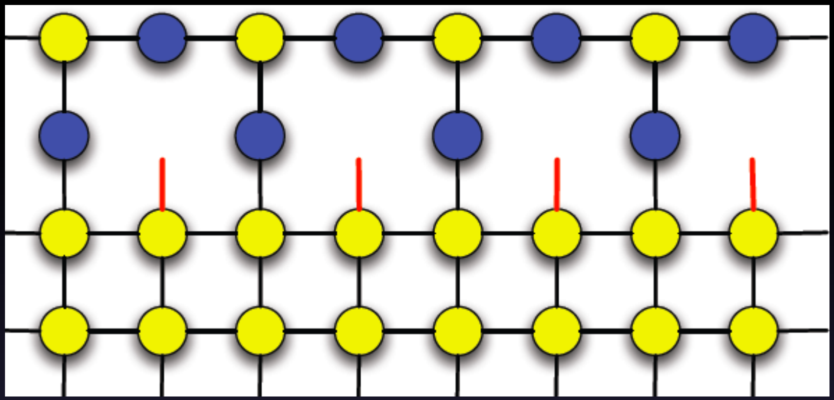
# Effect of radiation in silicon




- Even after heavy irradiation ***both*** p and n sides work at low voltage (under depleted) and sensors act as if there were 2 diode junctions!
- For $\Phi > 10^{15}\ n_{eq}/cm^2$ charge trapping is important: Charge Collection Distance becomes smaller than detector thickness

# Ionizing Dose

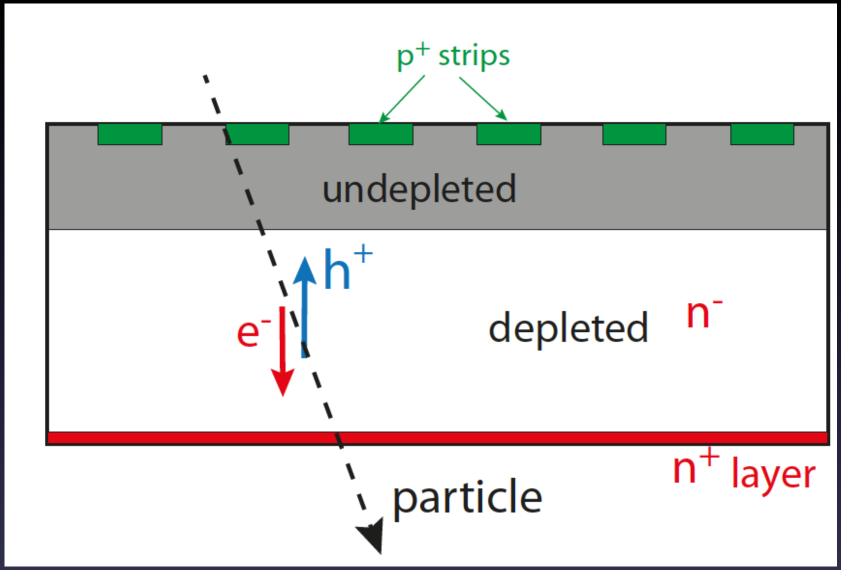
- Damage due to ionizing energy loss
  - Proportional to absorbed radiation dose
  - 1 Gy = 1 J/kg = 100 rad = $10^4$ erg/g (energy loss per unit mass)
  - Trap of ionization induced holes by "dangling bond" at Si-SiO2 interface



- **Affects both detector and electronics**

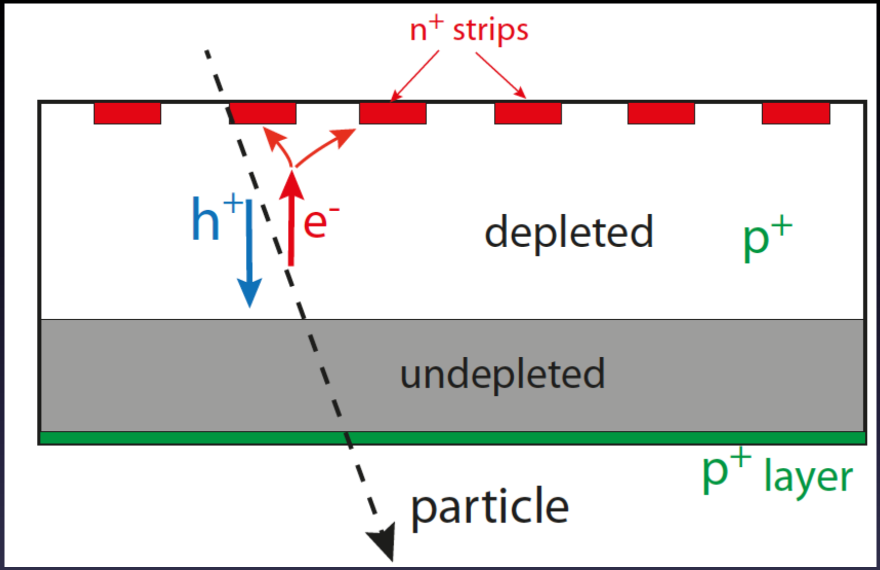
# HL-LHC Strips

- LHC and pre-LHC: $p^+$ in n




- Consequences:
  - signal loss
  - resolution degradation due to charge spreading

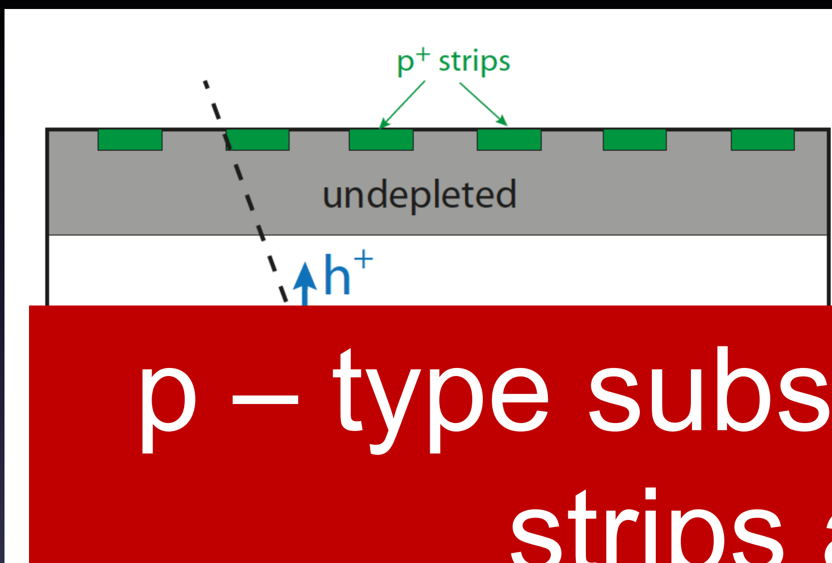
- For HL-LHC upgrade: $n^+$ in p or $n^+$ in n



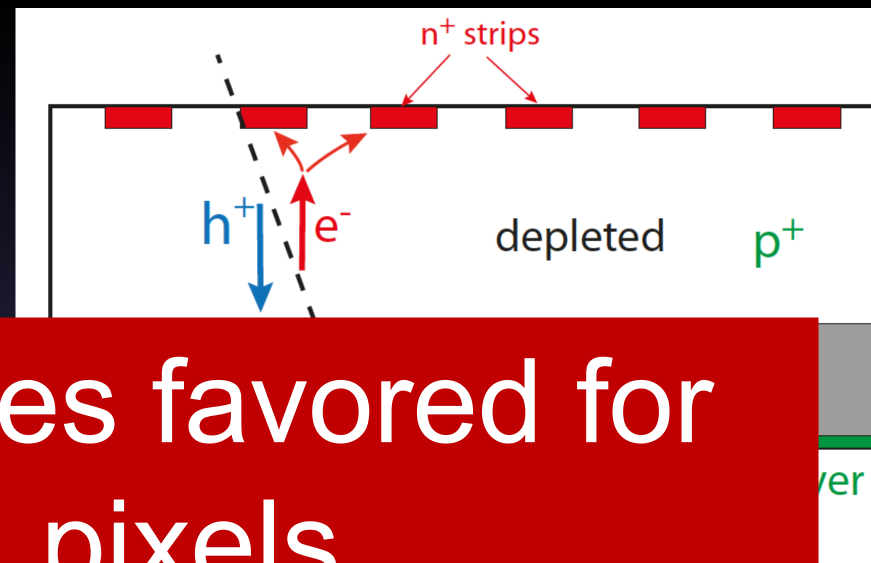

- Advantages:
  - faster charge collection (electrons have higher $v_{drift}$)
  - Less signal and CCE degradation

# HL-LHC Strips

- LHC and pre-LHC: $p^+$ in n




- For HL-LHC upgrade: $n^+$ in p or $n^+$ in n



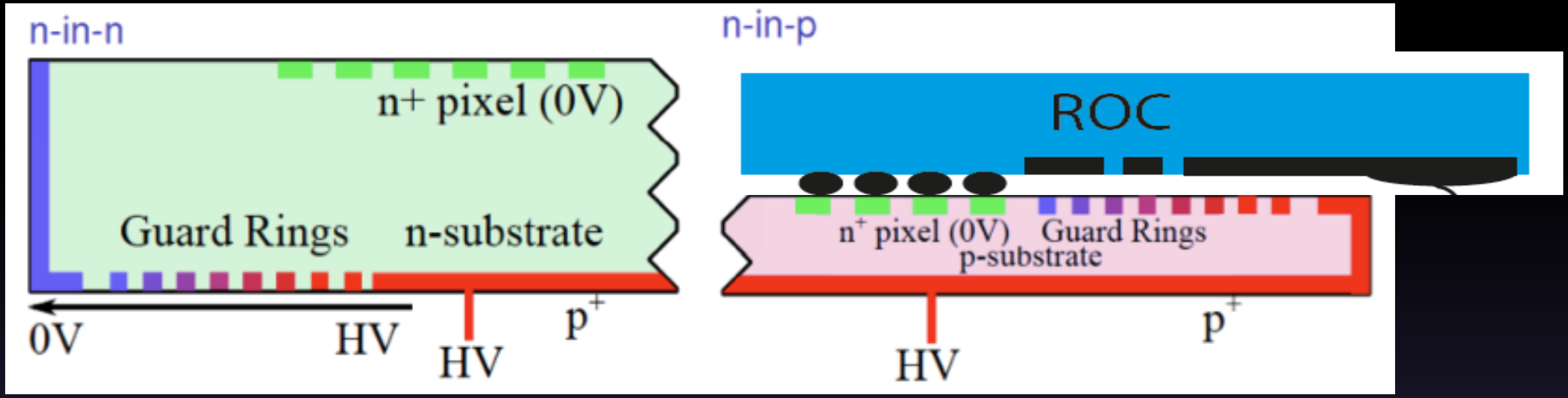

**p – type substrates favored for strips and pixels**

- Consequences:
  - signal loss
  - resolution degradation due to charge spreading

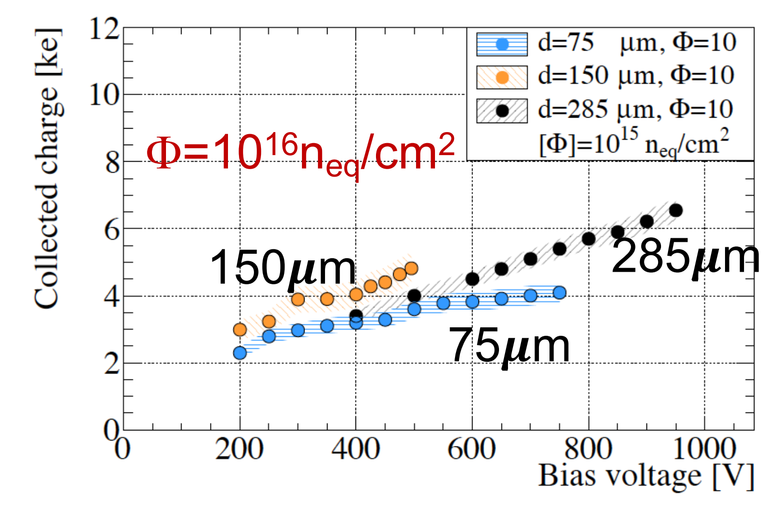
- Advantages:
  - faster charge collection (electrons have higher $v_{drift}$)
  - Less signal and CCE degradation

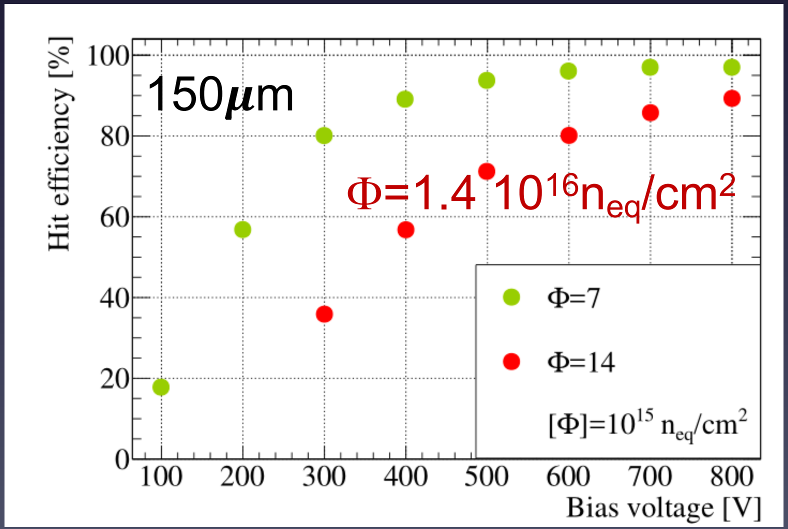
# HL-LHC Pixels

- Thin planar $n^+$ in p sensors sensors



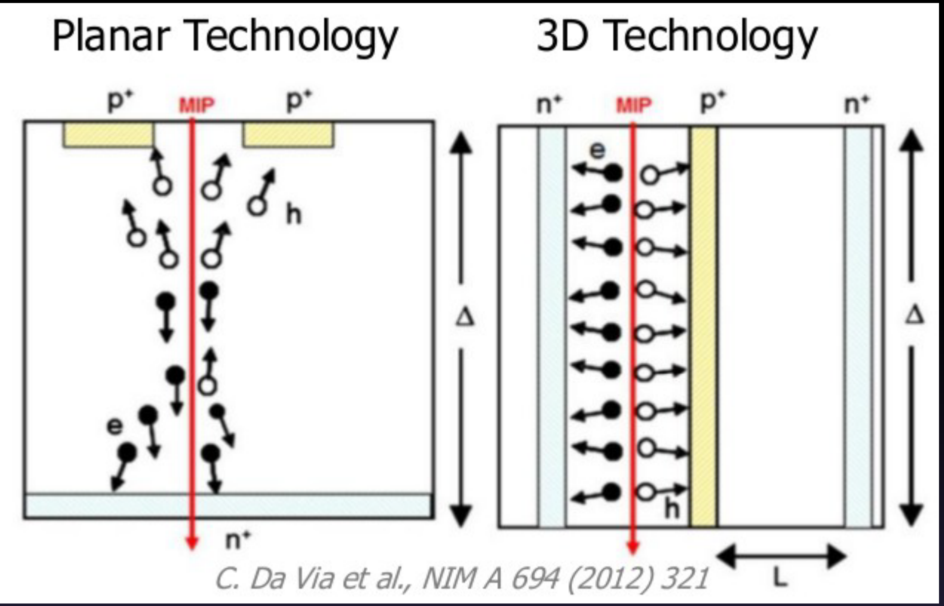

- 5000 $e^-$ in 150 μm thin sensors @ 500 $V_{bias}$
- Hit efficiency > 80% at $\Phi > 10^{16}$



# 3D sensors

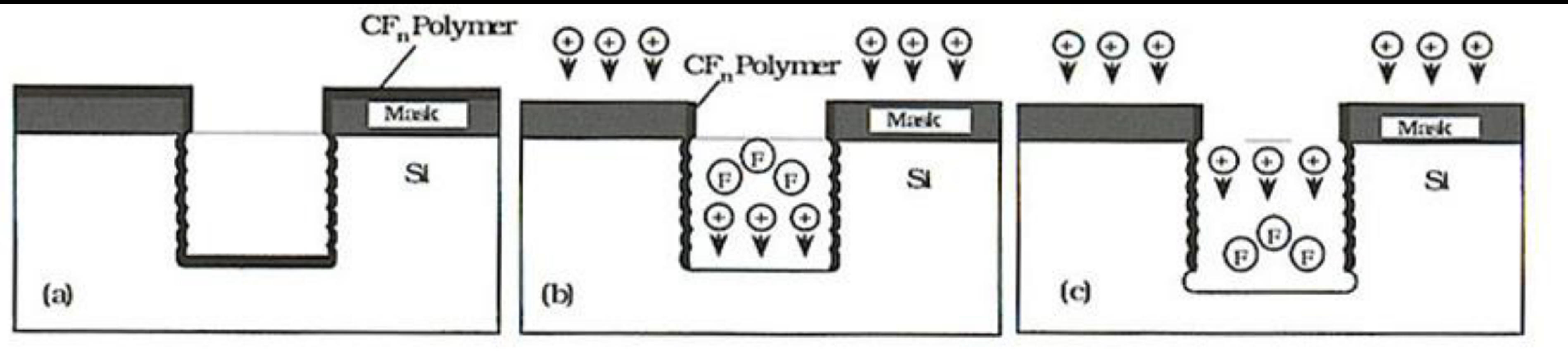
- Advantages
  - Decouple thickness from electrode distance
  - Lower depletion voltage, less power dissipation
  - Smaller drift distance, less trapping
- Disadvantage
  - More complex production process
  - Lower yield, higher costs
  - Higher capacitance (more noise)



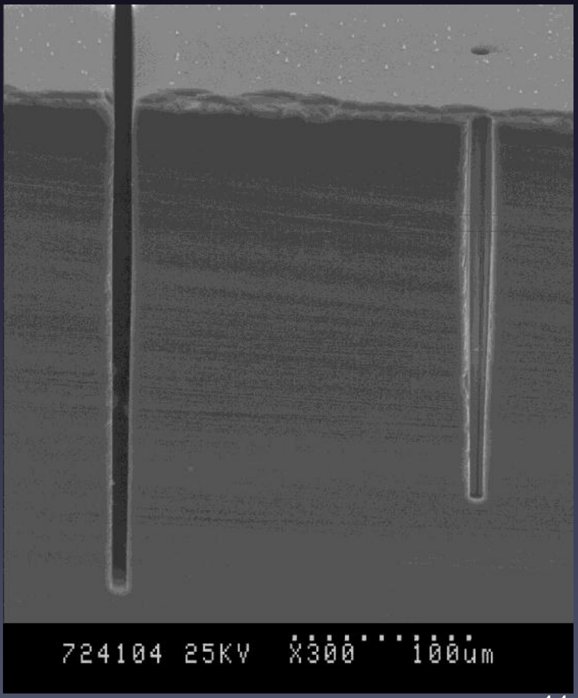

- 3D is the most radiation hard technology to-day
- Similar performance than planar sensors, but less demanding in terms of bias voltage and cooling.
- For the HL-LHC we need :
  - More radiation hard (innermost layer(s), 1-2E16 $n_{eq}/cm^2$)
  - Smaller pixels (compatible with new readout chip, 50 μm – 25 μm)
  - Thinner (reduce cluster size/merging, 200 μm – 100 μm)

S. Parker and C. Kenney

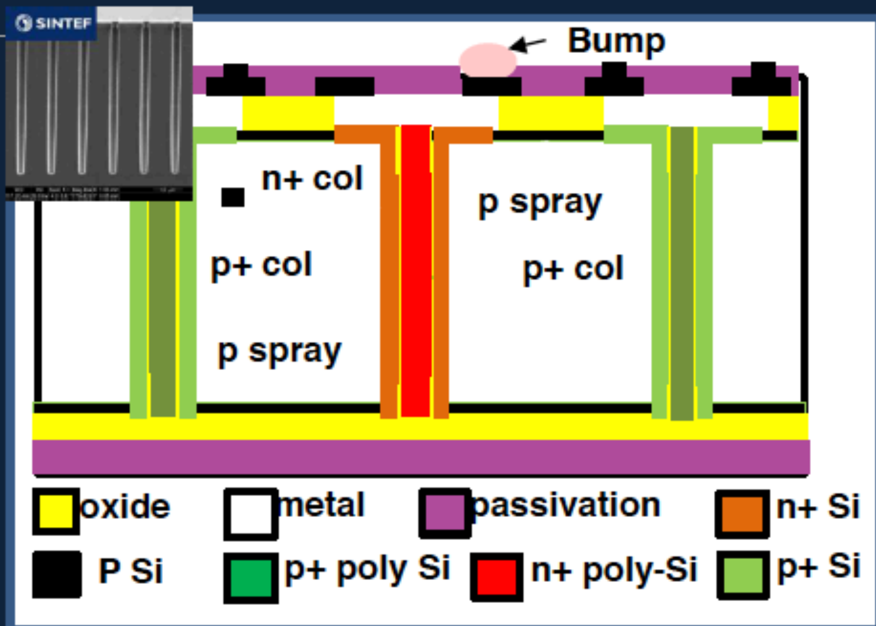
# Key fabrication steps




- **BOSCH PROCESS: alternating passivation (C4F8) and etch cycles (SF6)**
  - Within the plasma an electric field is applied perpendicular to the silicon surface.
  - The etch cycle consists of fluorine based etchants which react with silicon surface, removing silicon. The etch rates are ~1-5μm/minute.
  - To minimize side wall etching, etch cycle is stopped and replaced with a passivation gas which creates a Teflon-like coating homogenously around the cavity. Energetic fluorine ions, accelerated by the e-field, remove the coating from the cavity bottom but NOT the side walls.



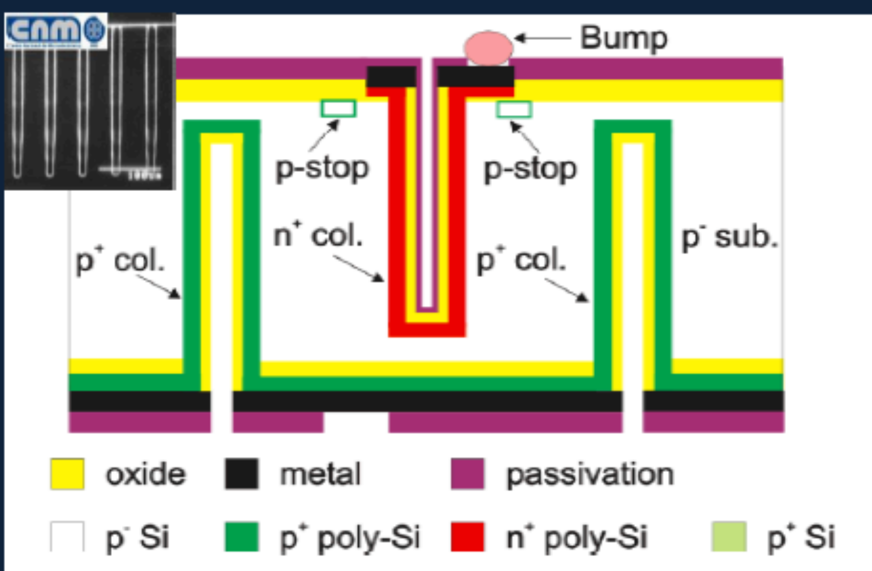
# Existing 3D designs

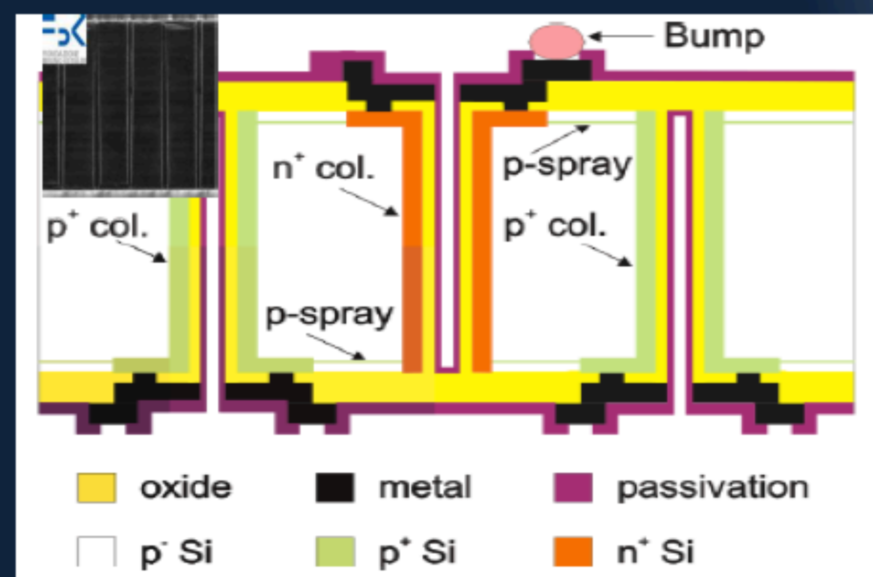




Single side, full 3D with active edges requires a support wafer which is removed later

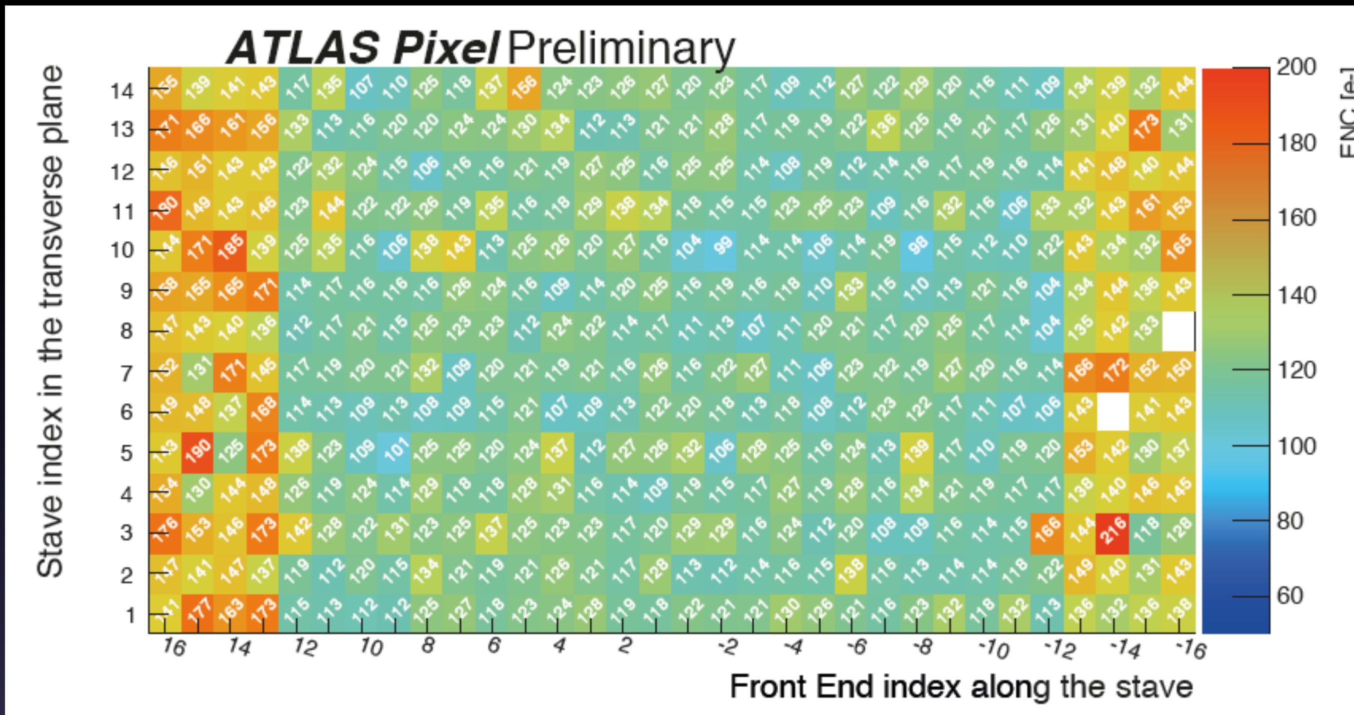

Double sided full or partially through3D with slim-fences (~200um)



# 3D in ATLAS IBL

NOISE MAP

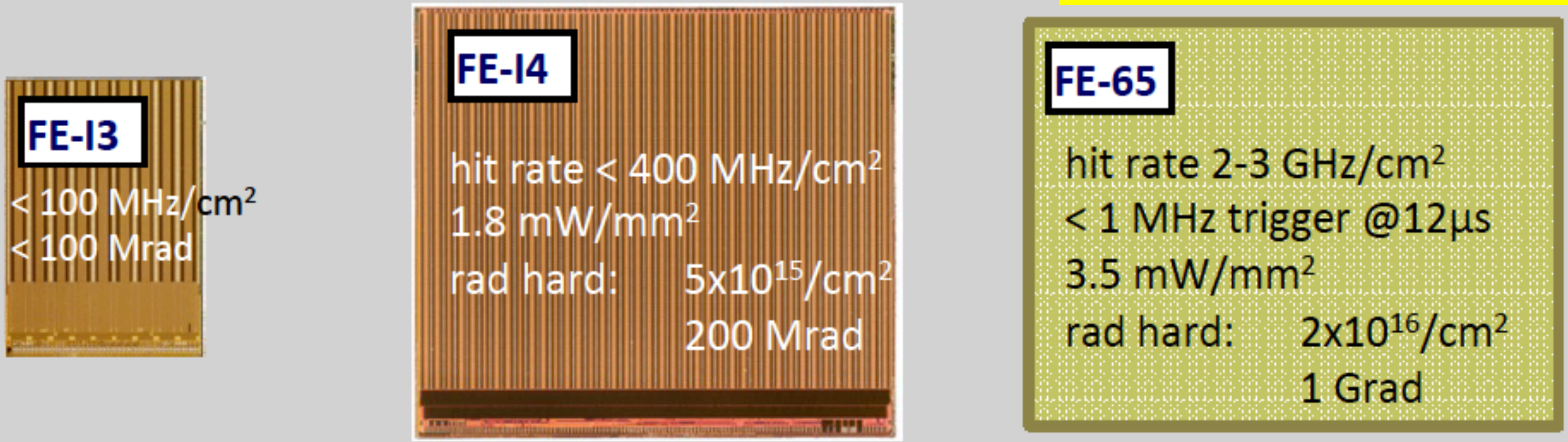



- After 4.3 fb$^{-1}$ corresponding to 1.3 Mrad and $2.5 \times 10^{13}$ $n_{eq}/cm^2$
- Bias voltage
  - IBL 3D: 20 V
  - IBL planar: 80 V
  - B-layer: 250 V

# RD53: 65 nm HL-LHC ROC

- Joint cross experiments effort to:
  - Radiation qualification and characterization of the CMOS 65 nm technology (TSMC)
  - Develop tools to design and characterize circuits and building blocks needed for pixel chips
  - Design and characterize a full scale demonstrator pixel chip
- FE-65 first full-size prototype -> spring 2016

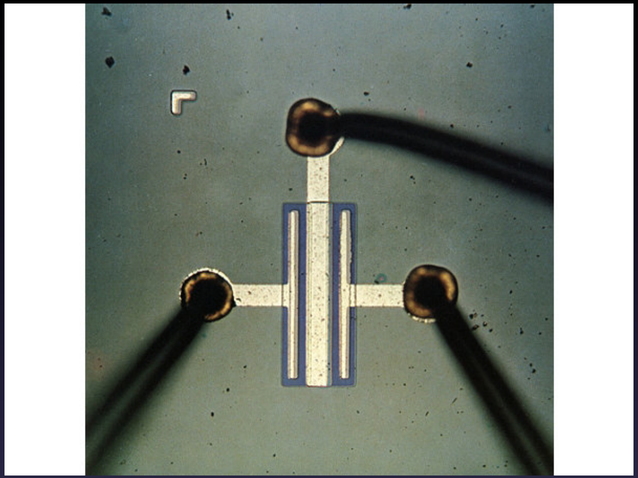
F. Faccio, TWEPP 2015, Proceedings

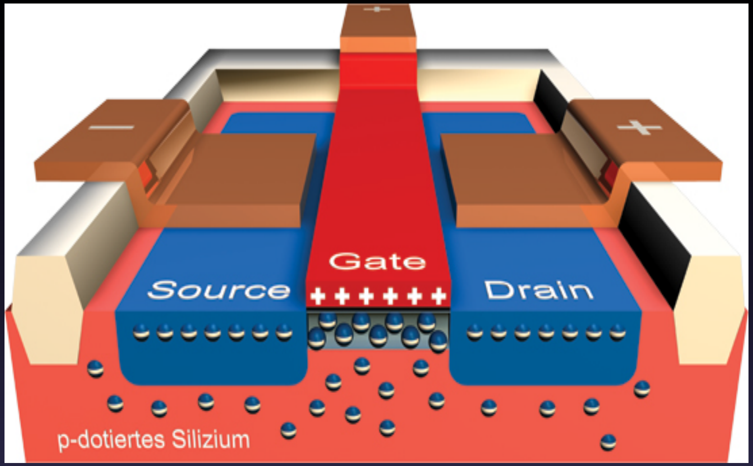


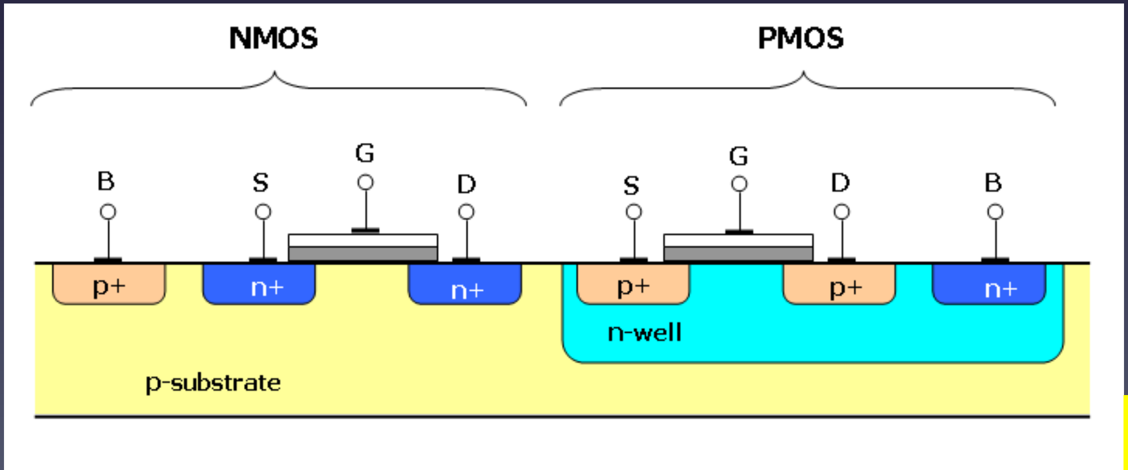

| FE-I3 | FE-I4 | FE-65 |
|---|---|---|
| 250 nm technology | 130 nm technology | 65 nm technology |
| pixel size 400 × 50 $\mu m^2$ | pixel size 250 × 50 $\mu m^2$ | pixel size 50 × 50 $\mu m^2$ |
| 3.5 M. transistors | 70 M transistors | ~ 1000 M transistors |

# CMOS

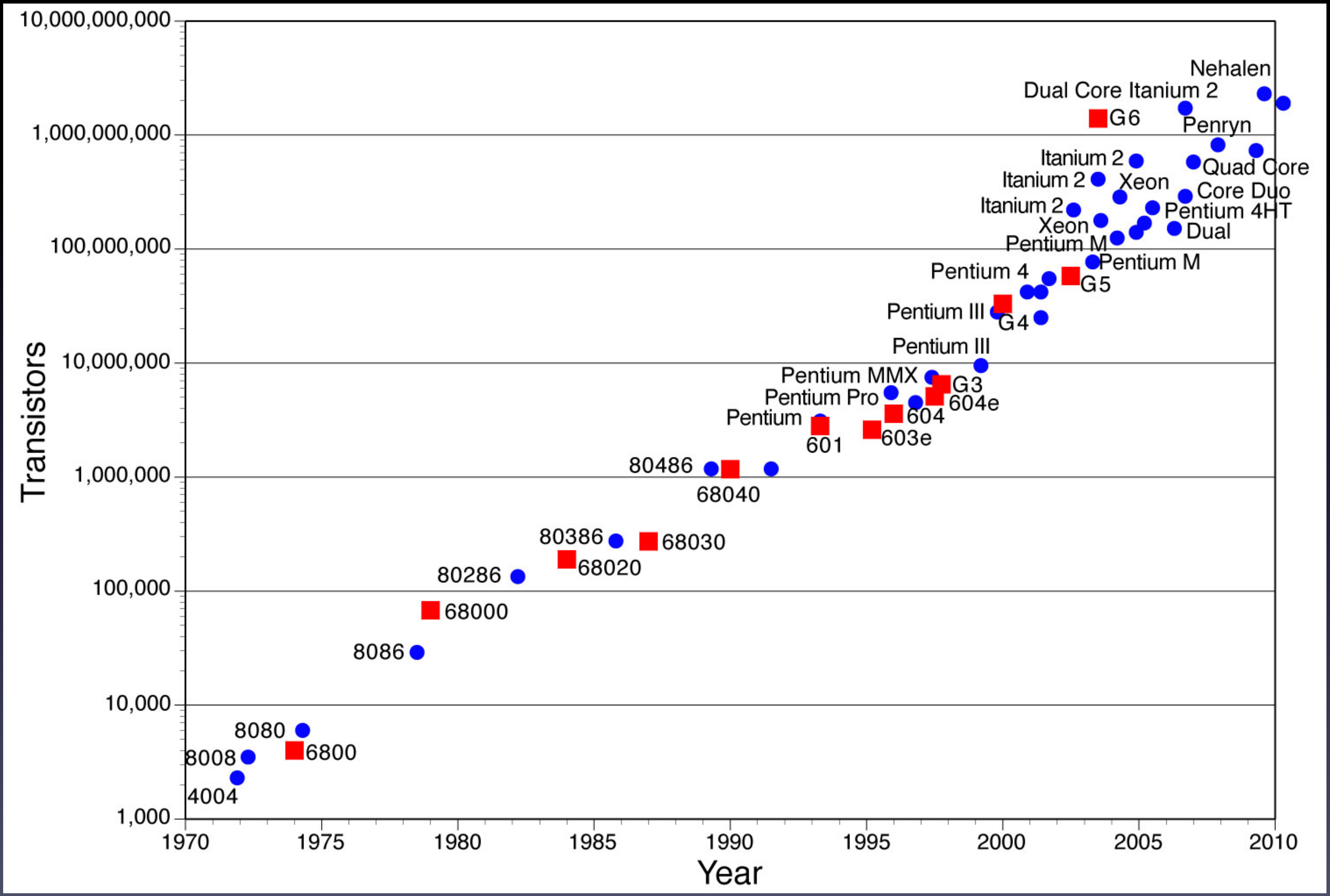
- The CMOS stays for the complementary metal oxide semiconductor transistor (a type of field effect transistor, F. Wanlass 1963)
- First MOSFET was realized in 1959 Dawon Kahng  and Martin M. Atalla.



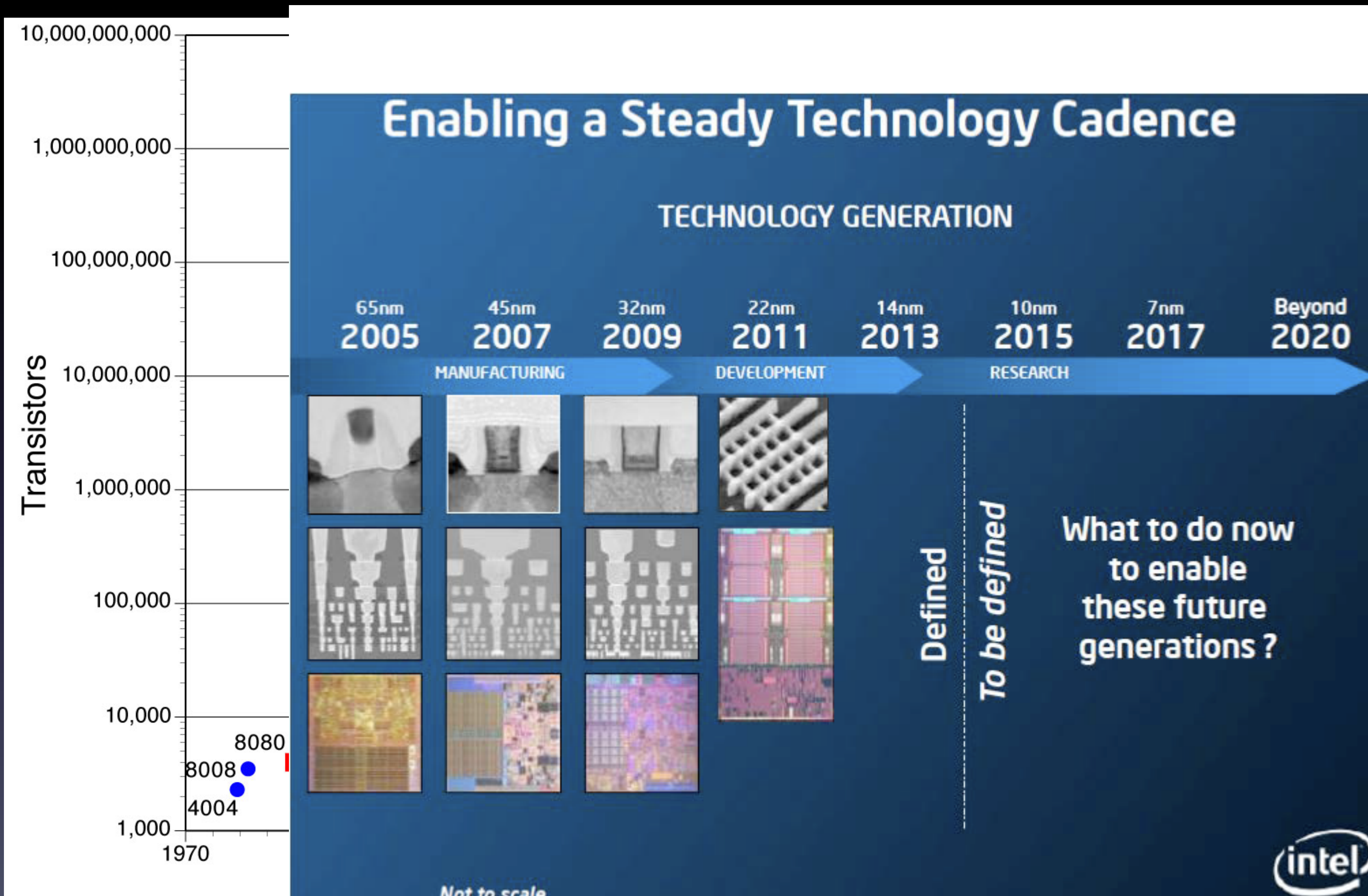


# CMOS


10,000,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
1,000
Transistors
1970
1975
1980
1985
1990
1995
2000
2005
2010
Year
4004
8008
8080
6800
8086
68000
80286
68020
80386
68030
80486
68040
Pentium
601
603e
604
Pentium Pro
Pentium MMX
G3
604e
Pentium III
Pentium III
G4
Pentium 4
G5
Pentium M
Pentium M
Xeon
Itanium 2
Itanium 2
Itanium 2
Xeon
Dual
Pentium 4HT
Core Duo
Quad Core
Penryn
G6
Dual Core Itanium 2
Nehalen

# CMOS


10,000,000,000
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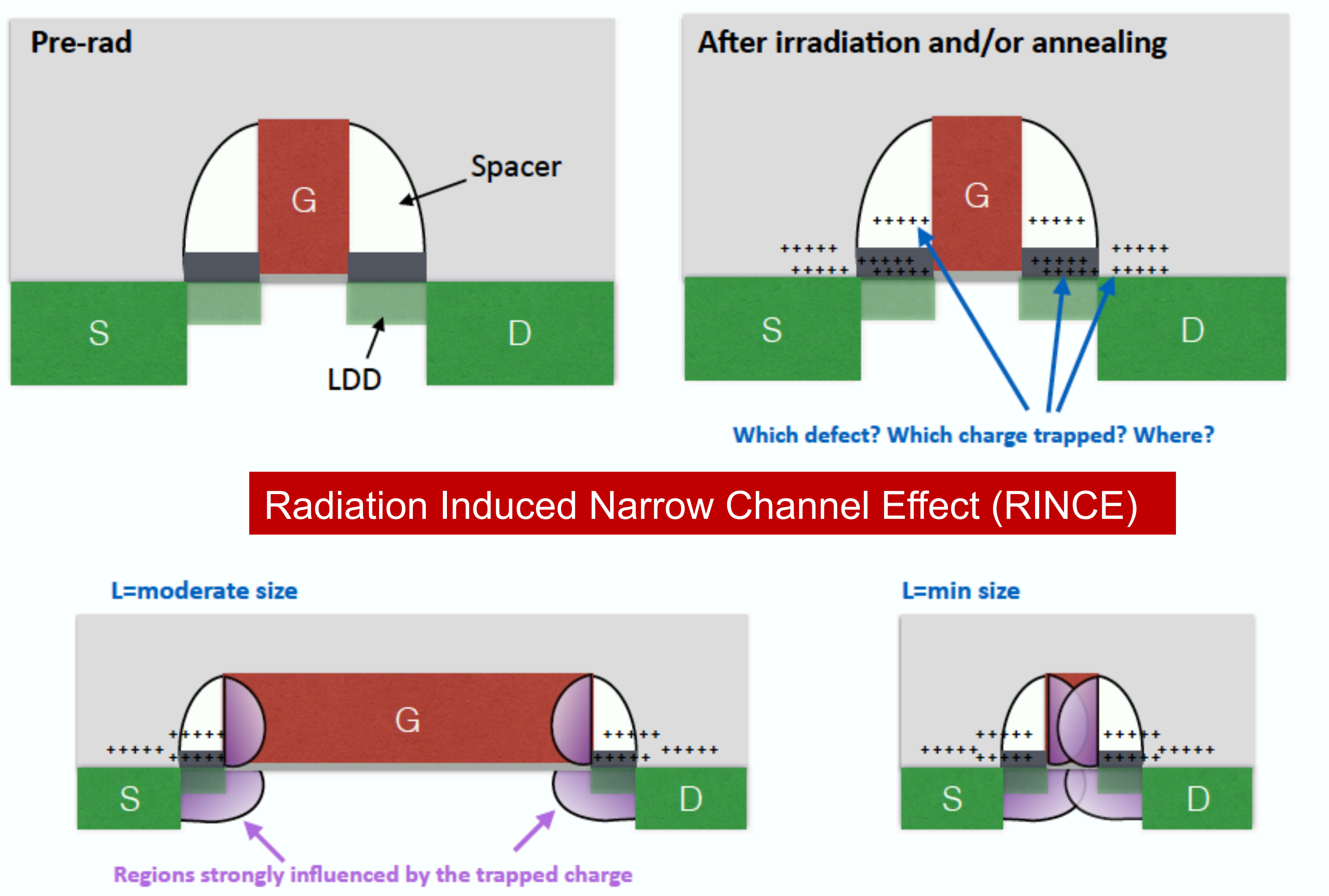
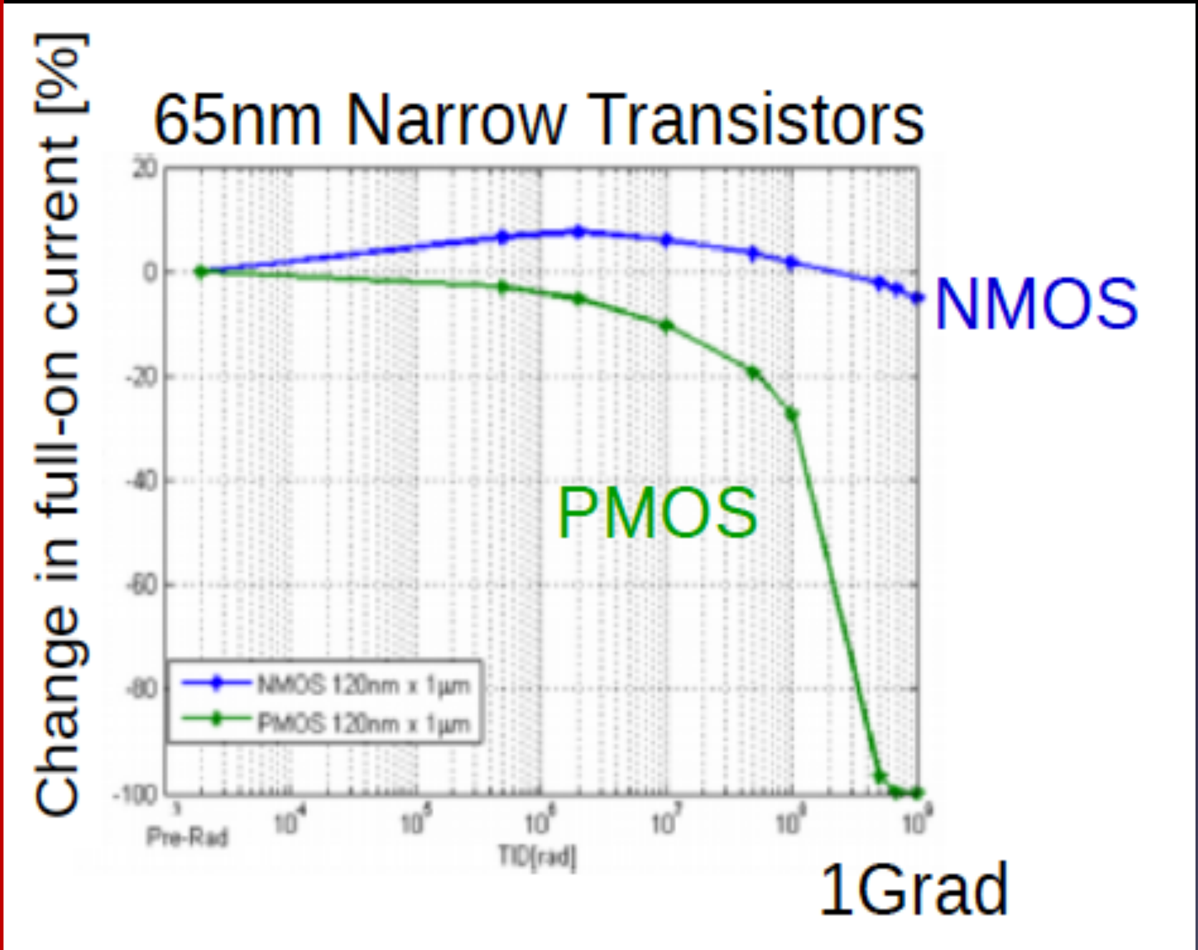
10,000,000
1,000,000
100,000
10,000
1,000
Transistors
1970
8080
8008
4004
Enabling a Steady Technology Cadence
TECHNOLOGY GENERATION
65nm 2005
45nm 2007
32nm 2009
22nm 2011
14nm 2013
10nm 2015
7nm 2017
Beyond 2020
MANUFACTURING
DEVELOPMENT
RESEARCH
Defined
To be defined
What to do now to enable these future generations ?
Not to scale
intel

# Radiation effects in 65 nm CMOS



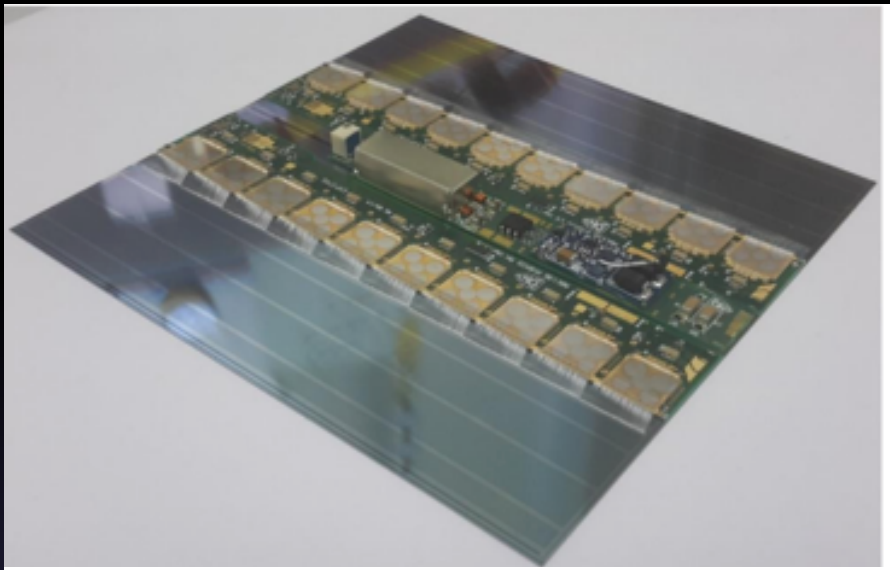
# Radiation effects in 65 nm CMOS

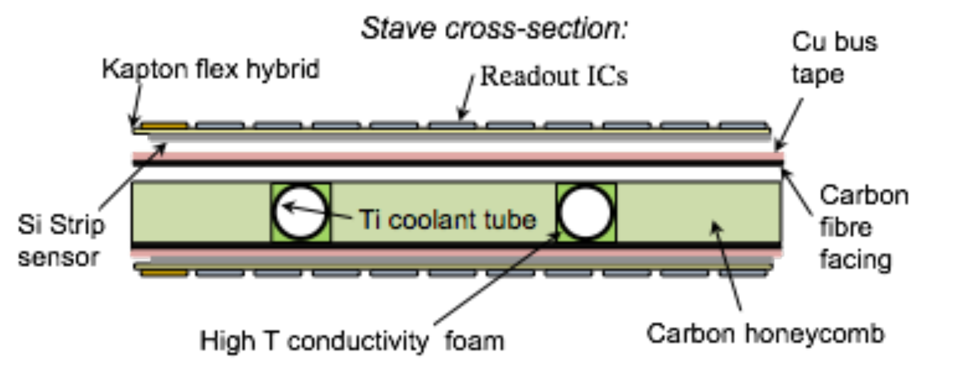
- NMOS are working without large damage up to 1Grad (damage < 20%)
- PMOS transistors do not work above 500Mrad
- Further studies ongoing including DRAD chip to investigate different transistors (size and shape)

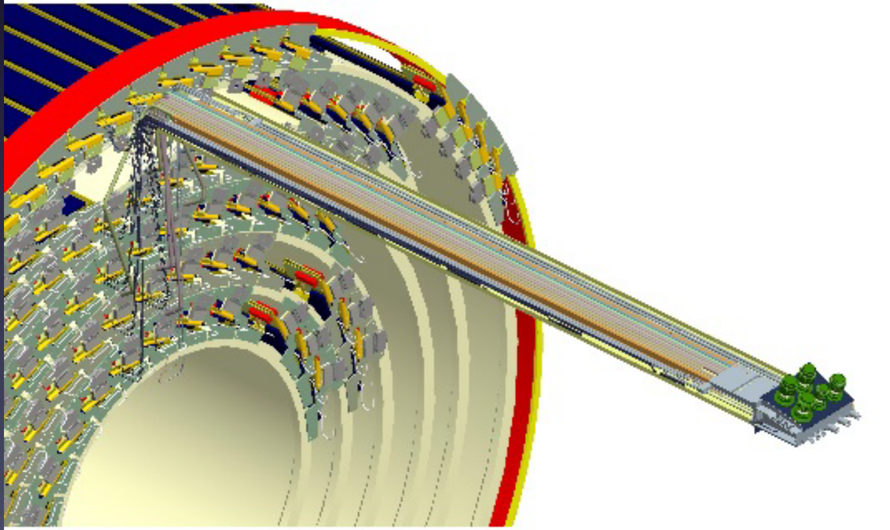


# ATLAS Tracker

- Driving design considerations
  - finer segmentation
  - simplicity & robustness maintaining minimal material
  - affordable cost



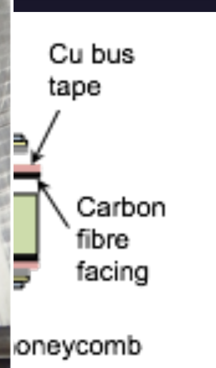


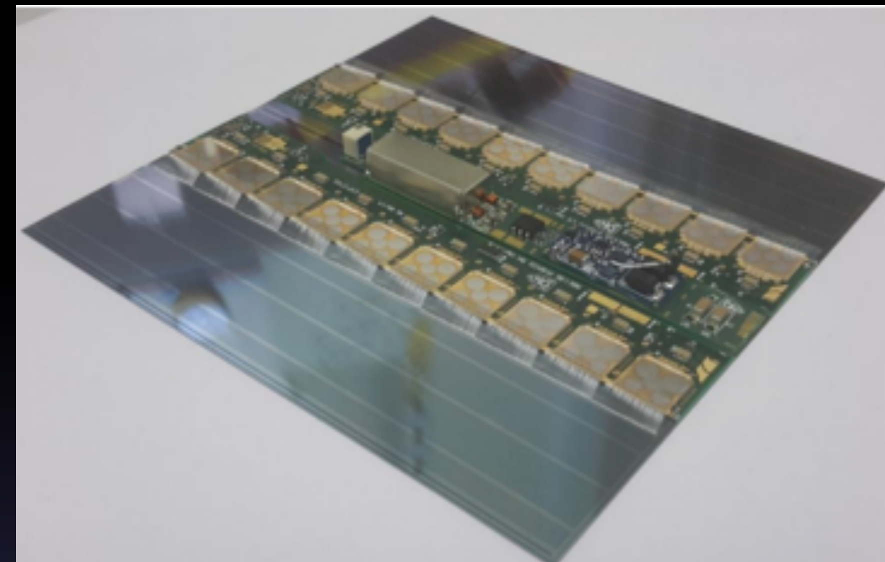



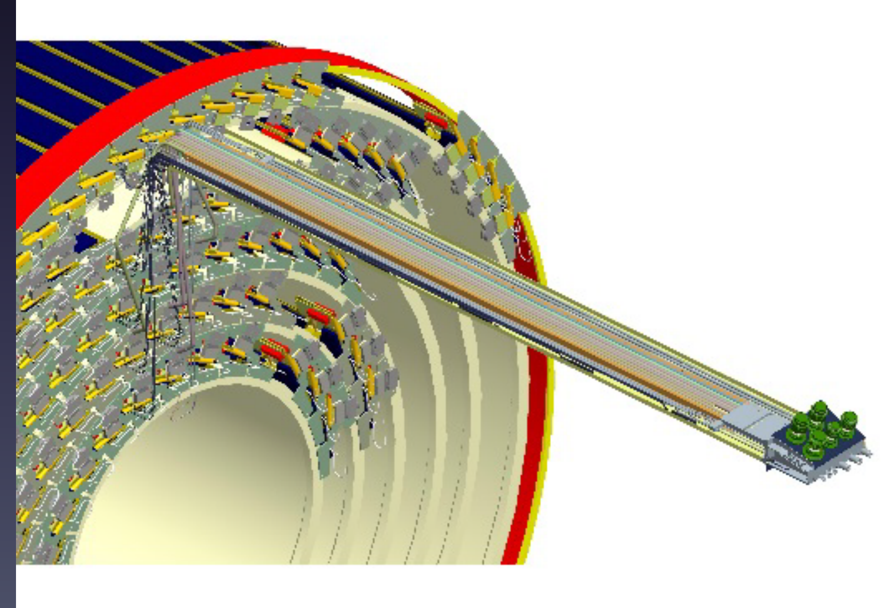
# ATLAS Tracker

- s

  ntaining



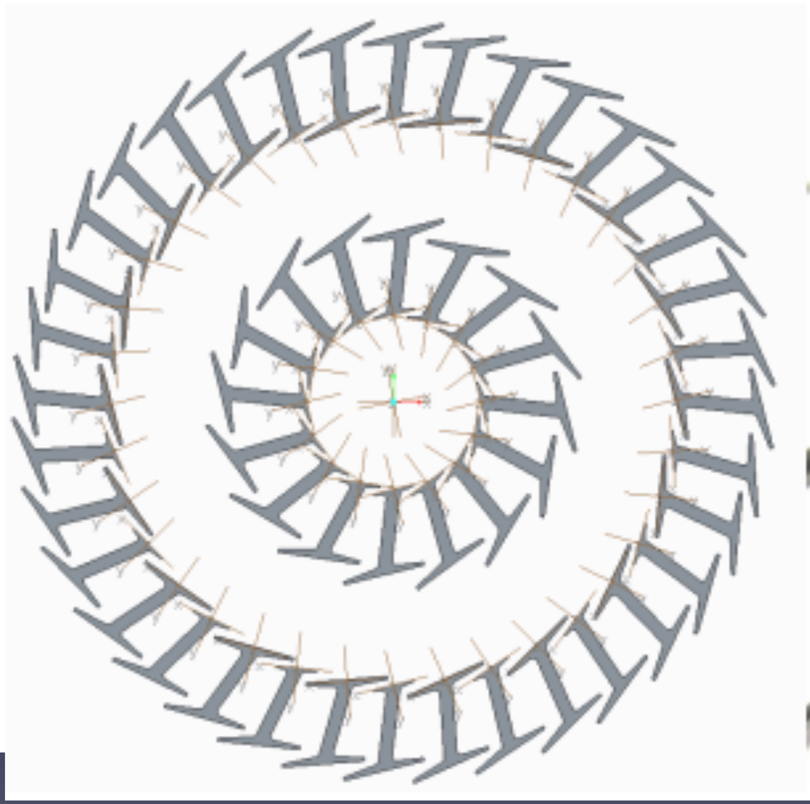



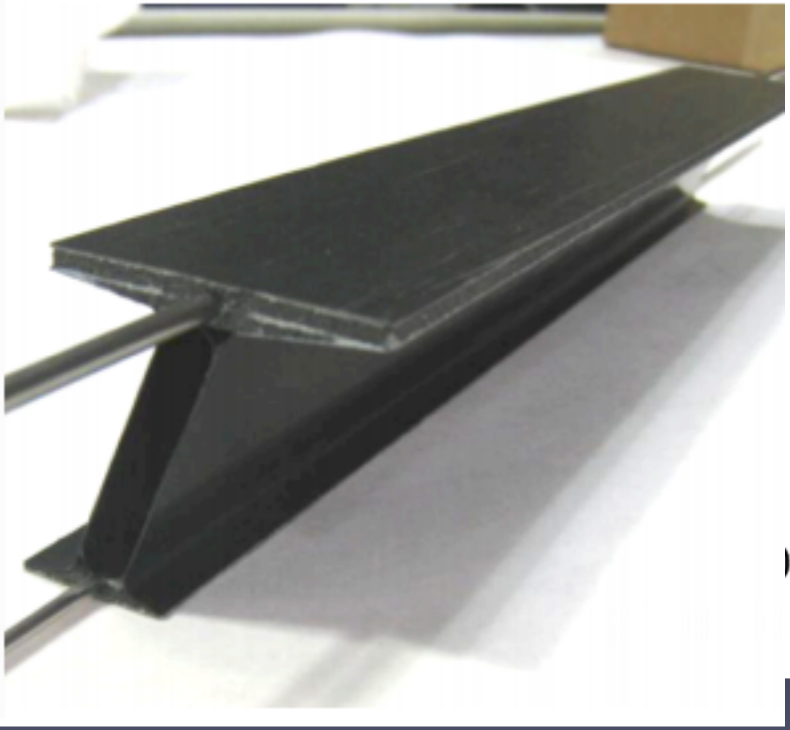


# ATLAS ITK Layouts

- Several layout under study

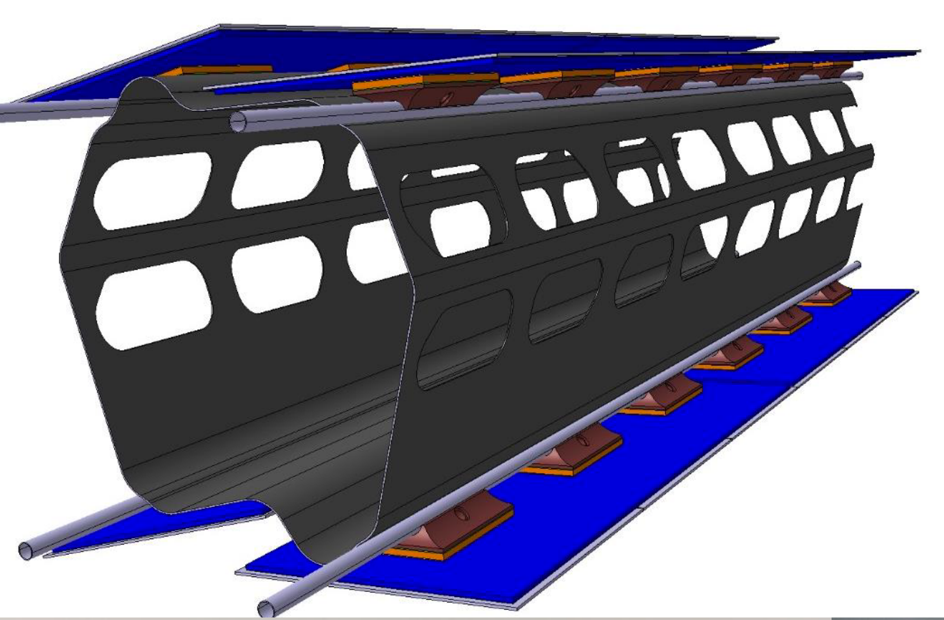
**I-beams:** low-mass carbon composite support structure

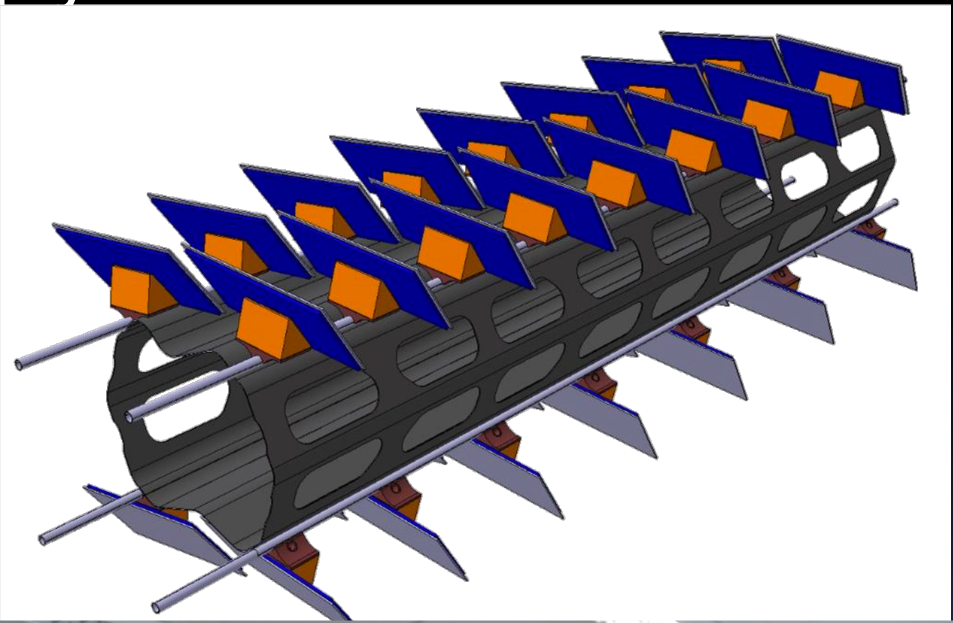


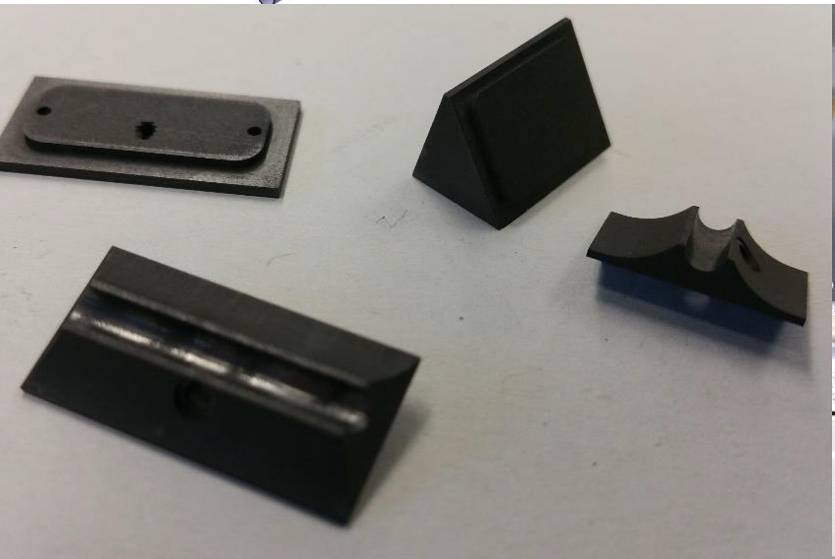


# ATLAS ITK Layouts

- Several layout under study



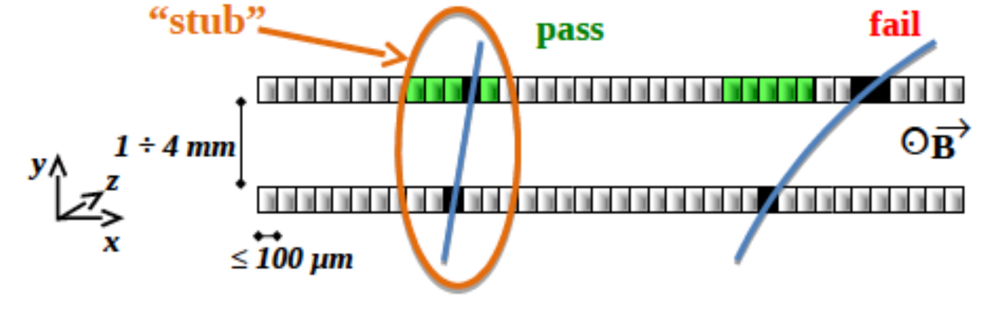


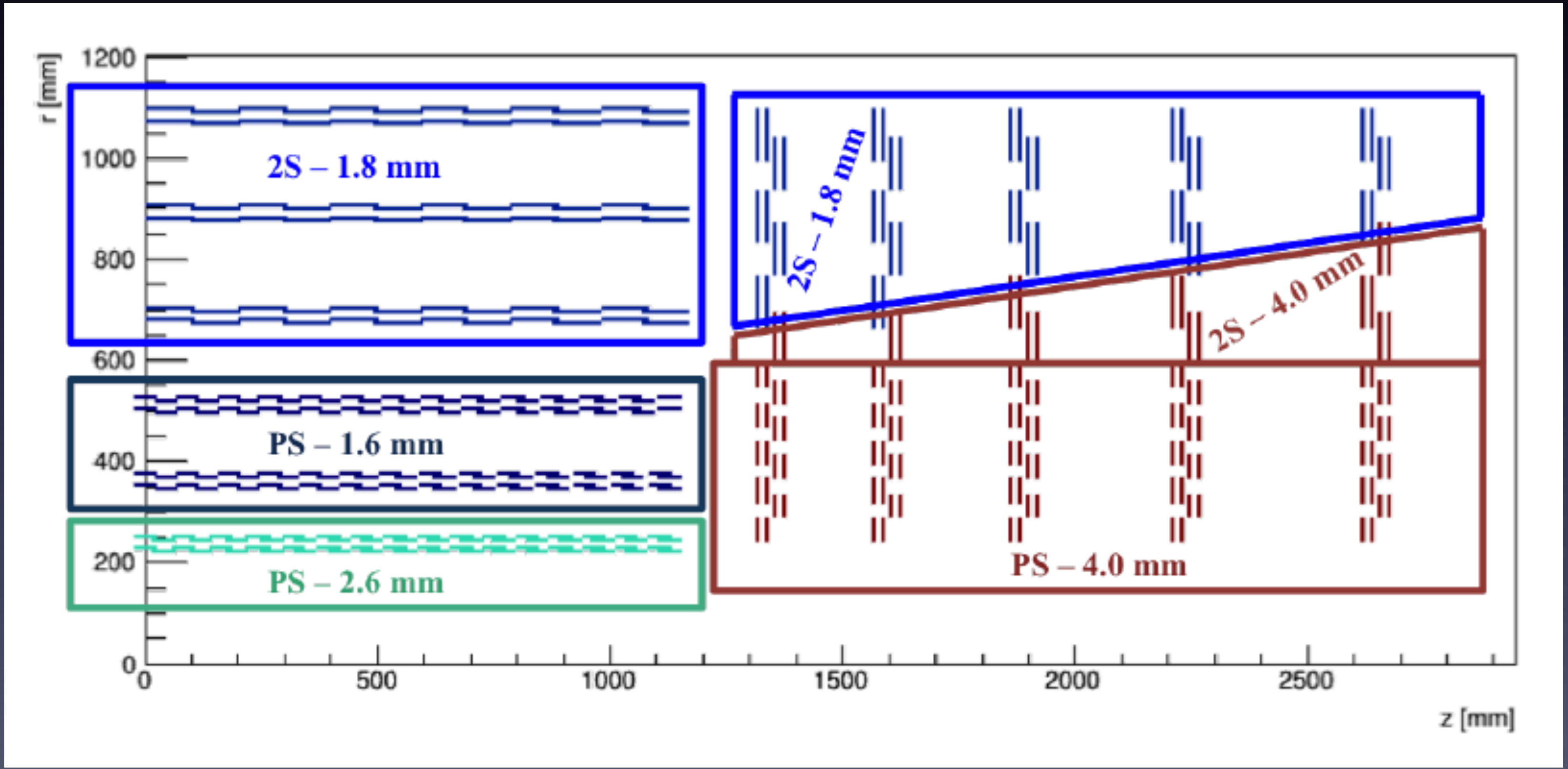


# CMS Tracker

- Excellent tracking performance
- Focus on triggering @ L1
- New industrial 8" (an possibly 12") sensors

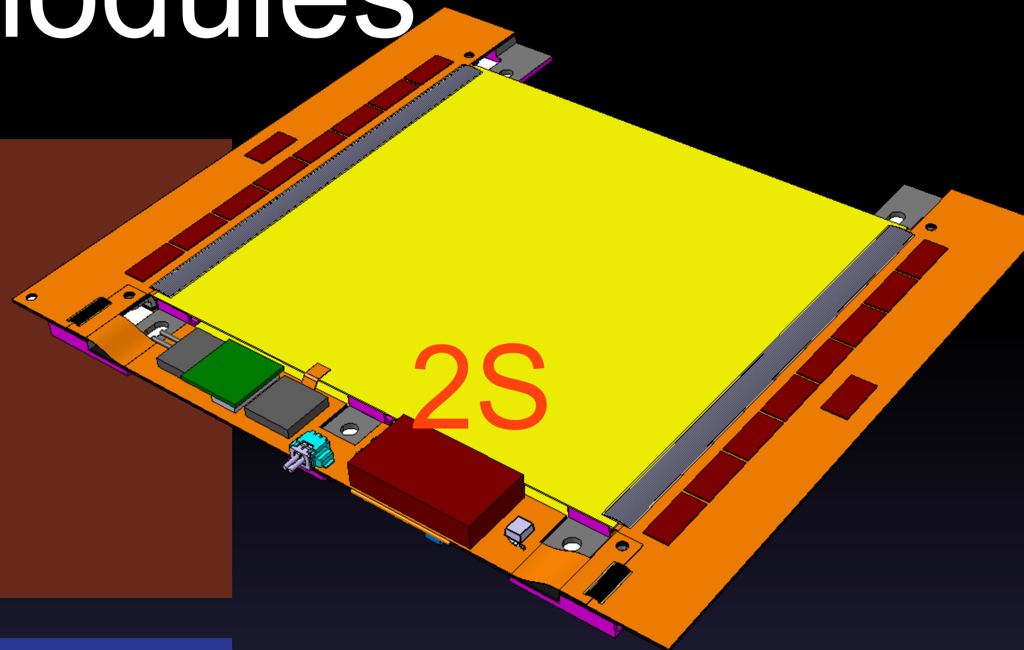
- Sensor spacing in the Outer Tracker was tuned to have $p_T$ cut of 2 GeV/c



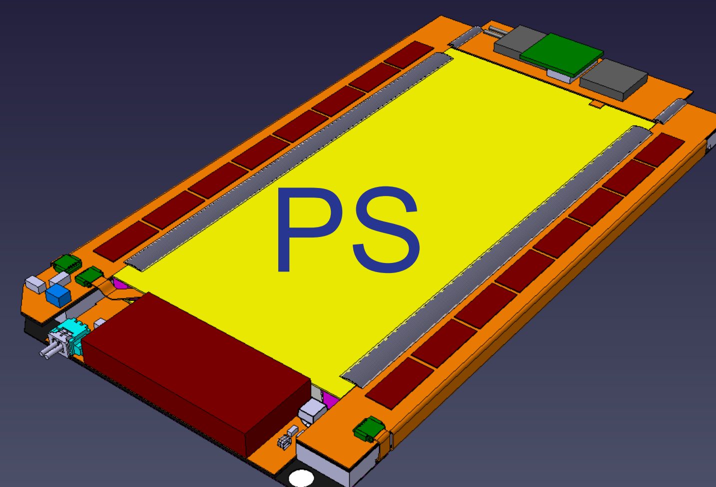



# pT modules

- 2 Strip sensors
- 2x1016 Strips: ~ 5 cm x 90 µm
- 2x1016 Strips: ~ 5 cm x 90 µm
- P ~ 5 W
- ~ 2x 90 $cm^2$ active area
- For r > 60 cm
- Spacing 1.8 mm and 4.0 mm

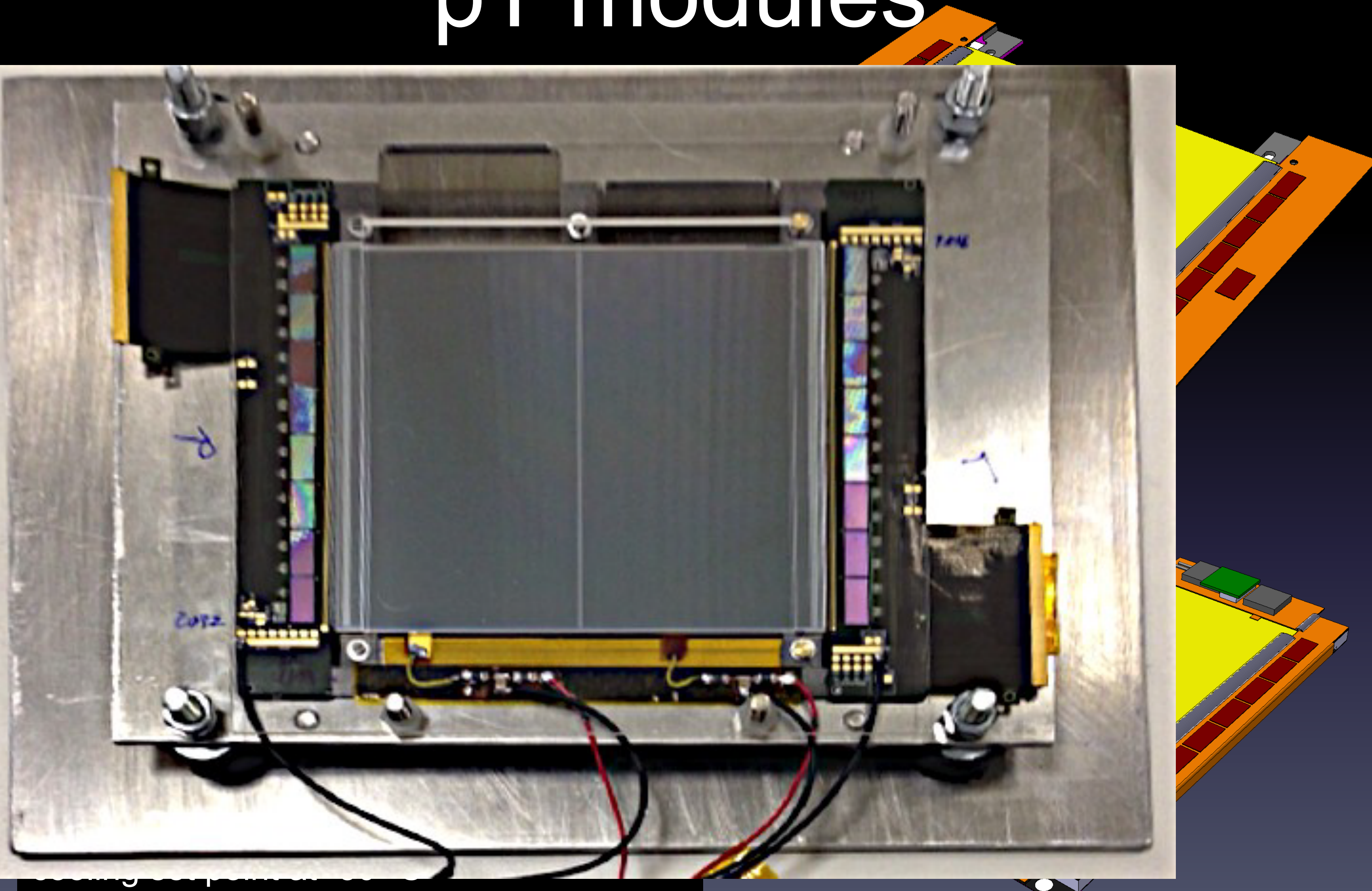



- Pixel + Strip sensors
- 2x960 Strips: ~ 2.5 cm x100 µm
- 32x960 Pixels: ~ 1.4 mm x100 µm
- P ~ 7 W
- ~ 2x 45 $cm^2$ active area
- For r > 20 cm
- Spacing 1.6 mm, 2.6 mm and 4.0 mm

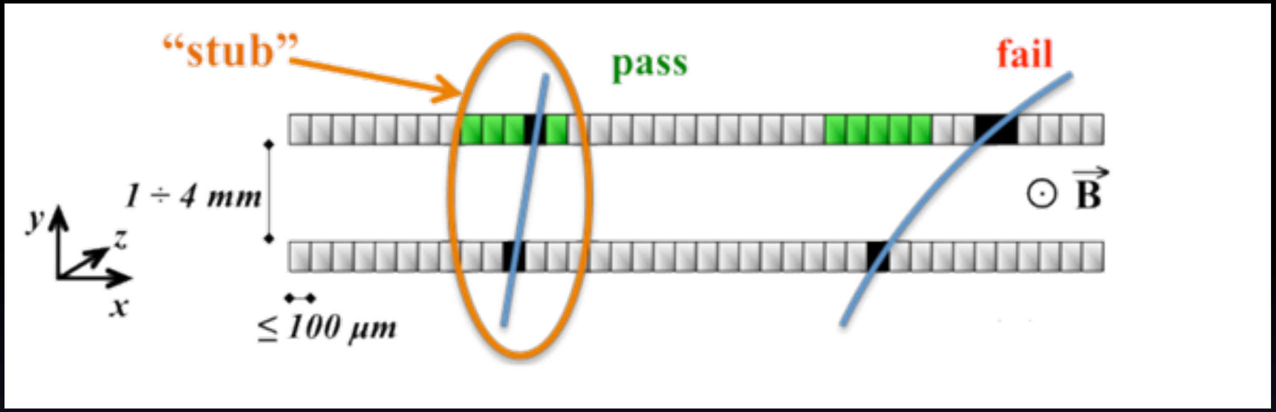



Operate sensors at about -20 $^{o}$C with cooling set point at -30 $^{o}$C

# pT modules

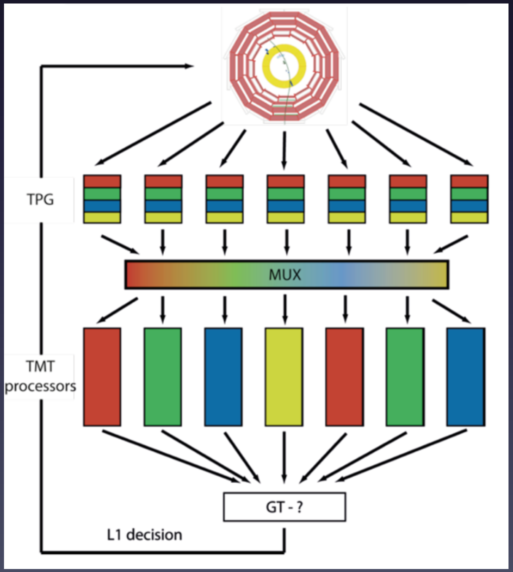


# CMS Track trigger

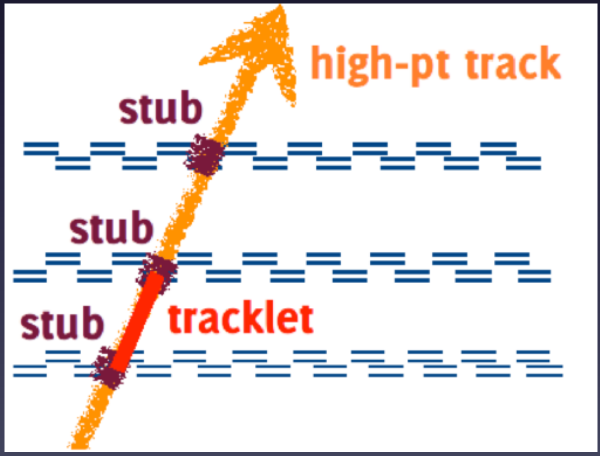



Associative memories

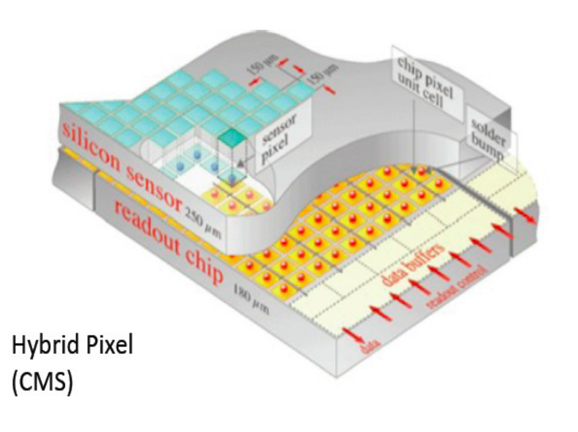

Time MUX Trigger to process complete event

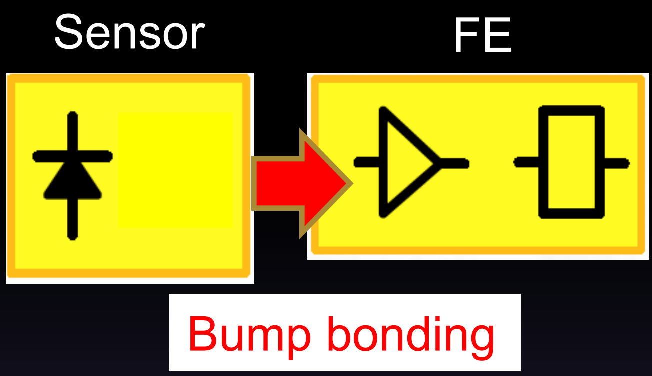



tracks seeded by stubs pairs

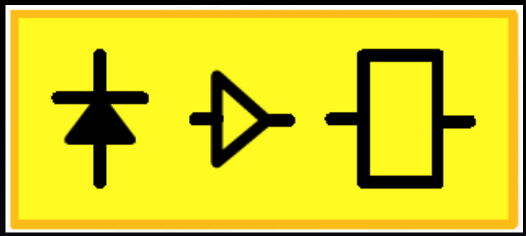


# From hybrid to monolithic pixels

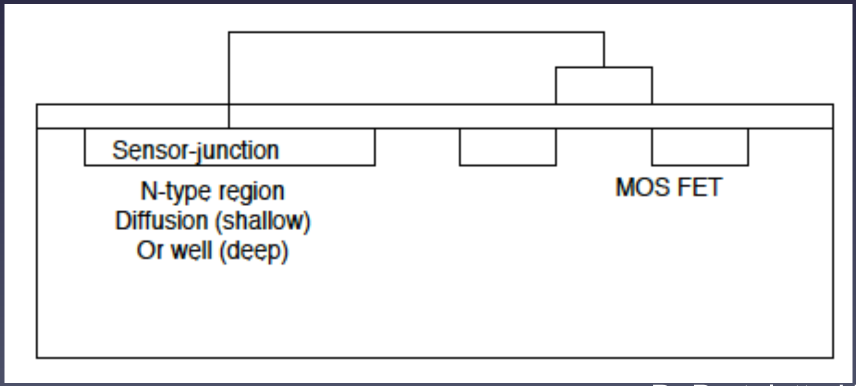


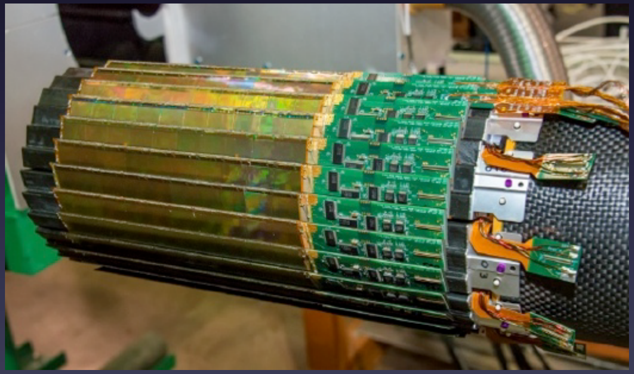

- Can we combine detection and readout in one ROC ?



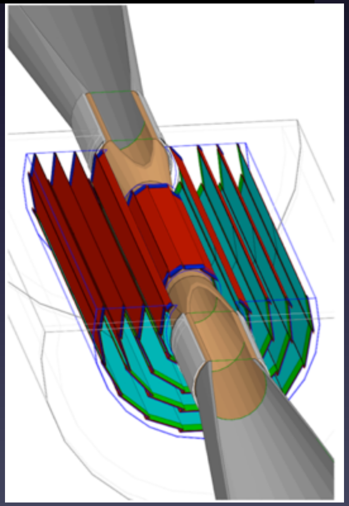
- Cheaper & better performance?
  - Better resolution
  - Easier module production
  - No bump-bonding
  - Lower material budget




STAR MAPS 2014 0.16 $m^2$

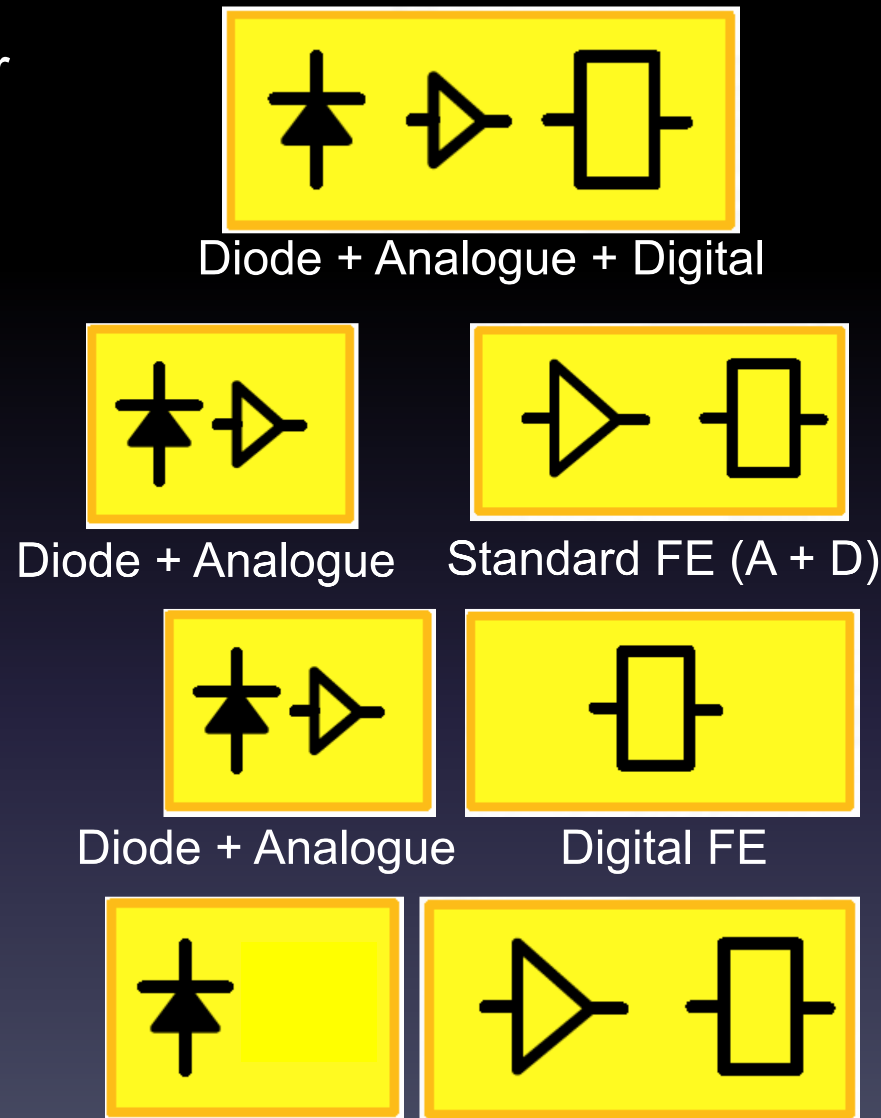


Technology of choice for ILC



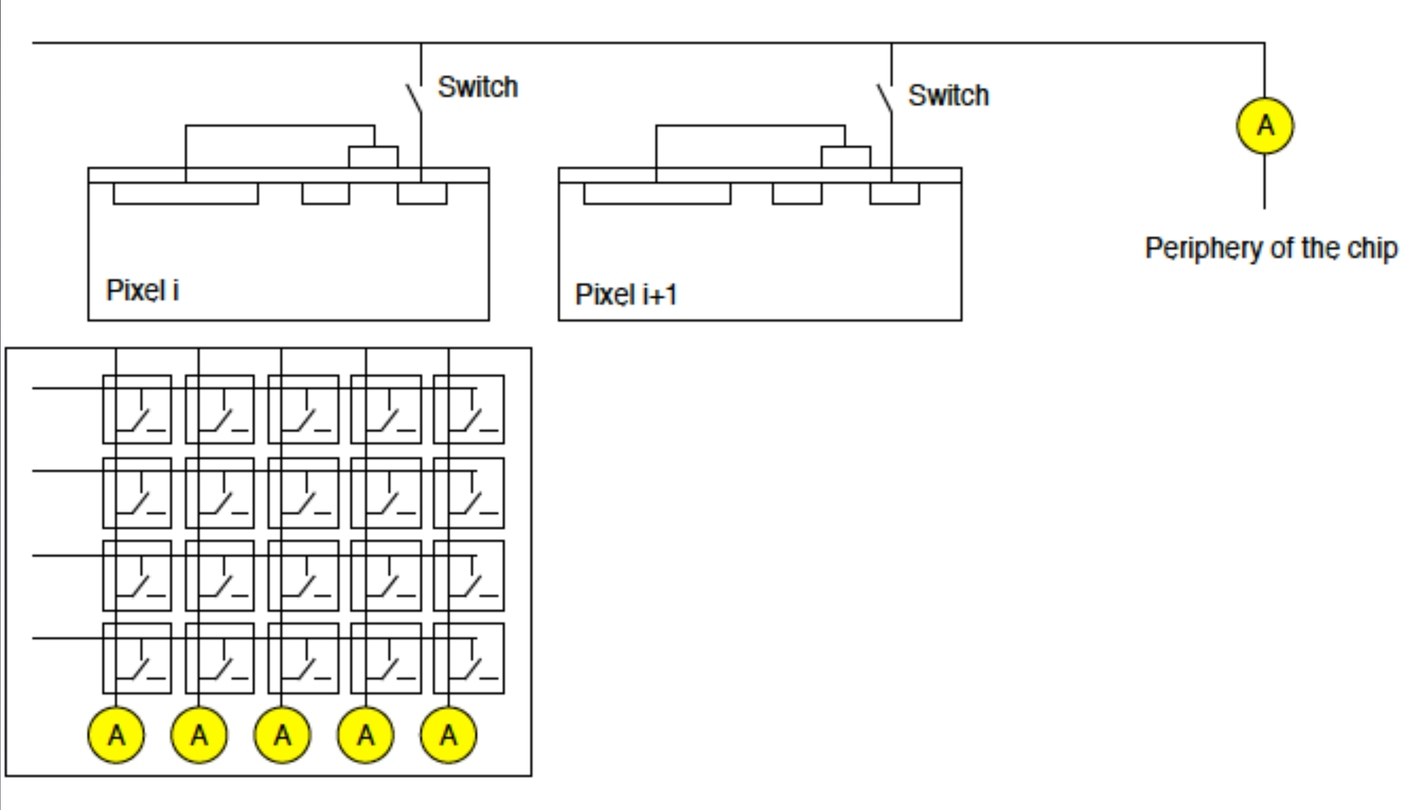
# A CMOS revolution ?

- Depleted Monolithic Active Pixel Sensor
  - HR-material (charge collection by drift)
  - Fully depleted MAPS (DMAPS)
- Hybrid Pixels with Smart Diodes
  - HR or HV-CMOS as a sensor (8”)
  - Standard FE chip
  - CCPD (HVCMOS) on FE-I4
- CMOS Active Sensors + Digital R/O chip
  - HR or HV-CMOS sensor + CSA (+Discriminator)
  - Dedicated “digital only” FE chip
- Passive CMOS Sensor + R/O chip
  - HR or HV-CMOS sensor
  - Dedicated FE chip
  - Low cost C4 bumping and flip-chip



# CMOS for imaging

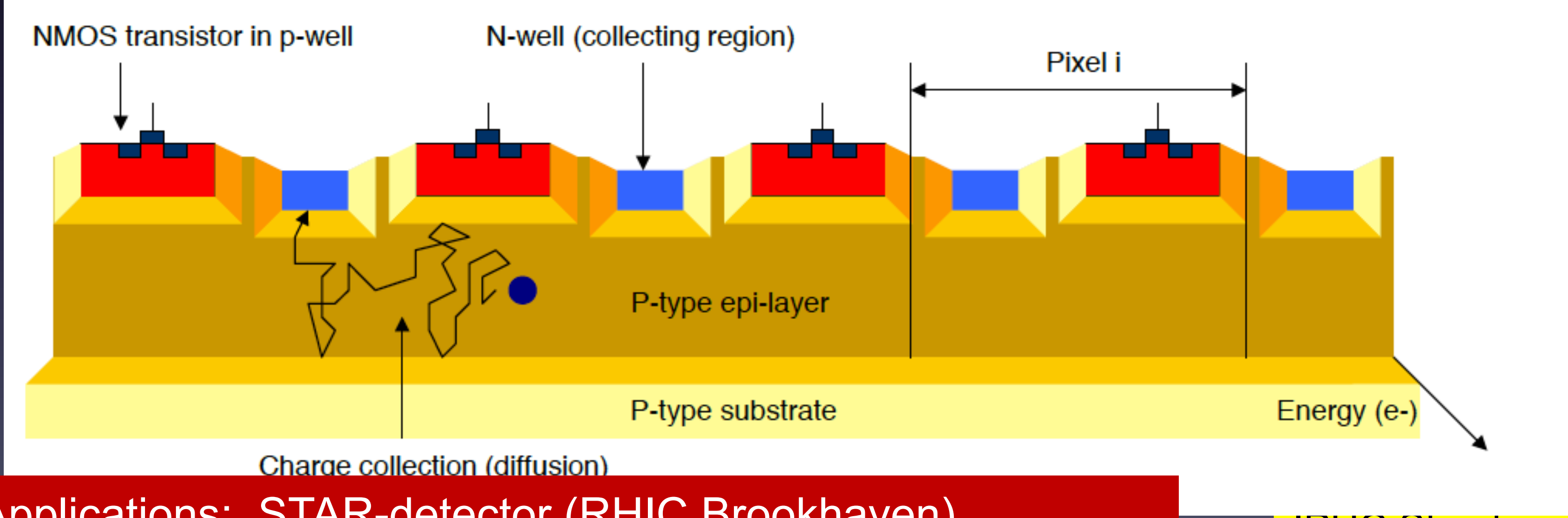
- Rolling shutter architecture
  - Pixels of the same column share the same column line.
  - The gates of the switches are connected row-wise
  - For the readout of whole matrix we need n steps, where n is the number of rows.
  - Proper concept for imaging



# Monolithic Active Pixels

- Use standard CMOS technology
- Signal is created in epitaxial layer (10-15 µm e.g. AMS 0.35 µm)
- Q≃80 e-h/µm ➠ signal <1000 e−
- Q collected many by diffusion P-MOS transistor could lead to a loss of charge
- Small pixel sizes(pitch 20 –30 µm) ➠ few µm resolution

- Very thin sensitive volume impact on signal magnitude
- Sensitive volume almost un-depleted
- Collection through diffusion slow ➠ impact on radiation tolerance & speed
- Only N-MOS transistors

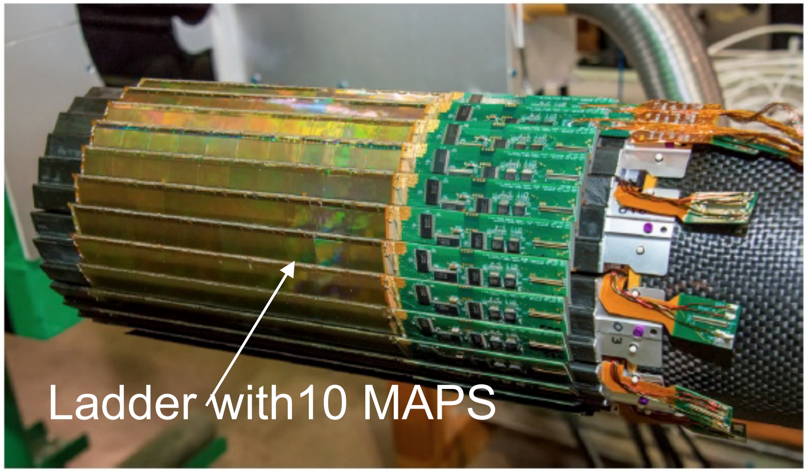



Applications:, STAR-detector (RHIC Brookhaven)
Eudet beam-telescope

IPHC Strasbourg
(PICSEL group))

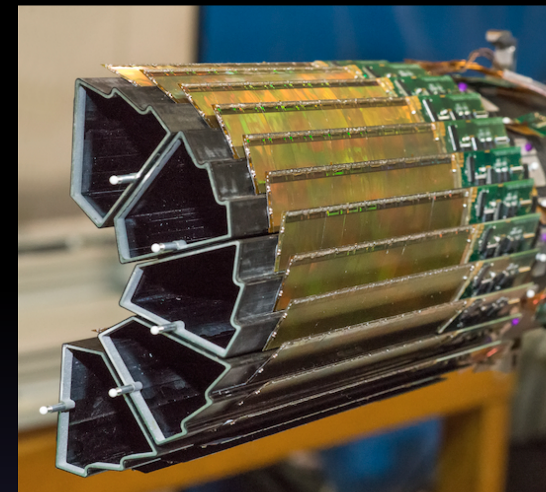
# MAPS in STAR

- Data taking since 2014 (Au-Au, p-p, p-Au-collisions)



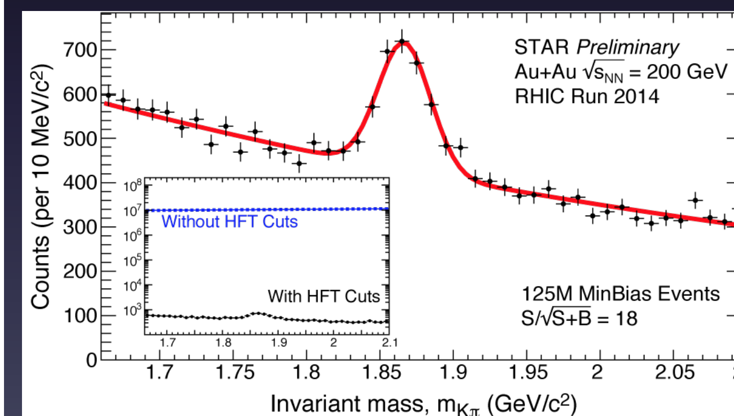

356 M pixels in 2 layers ~0.16 m$^2$

L. Greiner, FEE 2014



carbon fiber sector tubes (~ 200 µm thick)

| | |
|---|---|
| DCA Pointing resolution | (10 ⊕ 24 GeV/p·c) µm |
| Layers | Layer 1 at 2.8 cm radius<br>Layer 2 at 8 cm radius |
| Pixel size | 20.7 µm X 20.7 µm |
| Hit resolution | 3.7 µm (6 µm geometric) |
| Position stability | 5 µm rms (20 µm envelope) |
| Material budget first layer | $X/X_0$ = 0.39% (Al conductor cable) |
| Number of pixels | 356 M |
| Integration time (affects pileup) | 185.6 µs |
| Radiation environment | 20 to 90 kRad / year<br>2*10$^{11}$ to 10$^{12}$ 1MeV n eq/cm$^2$ |
| Rapid detector replacement | < 1 day |

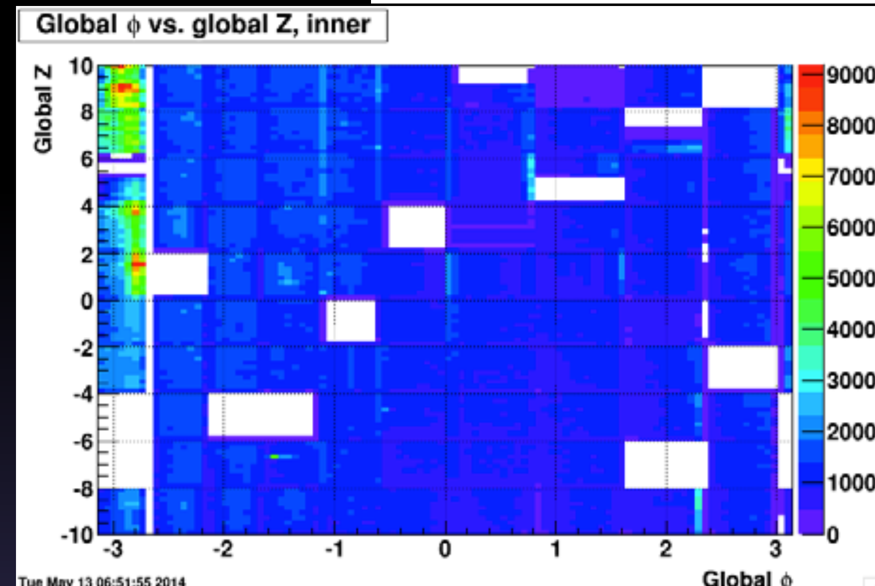


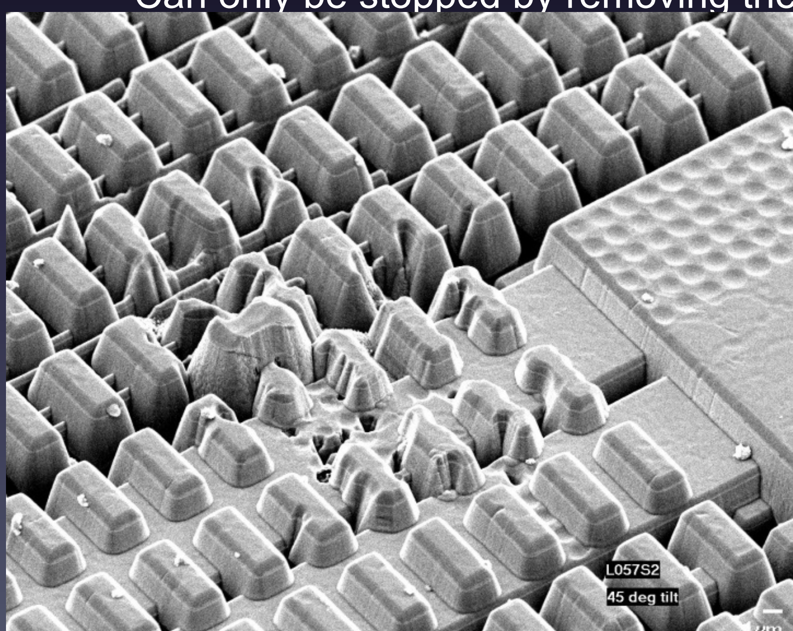

Topological reconstruction of charm hadrons such as $D^0$ which a lifetime ~ 120 µm

# MAPS in STAR

- Unexpected damage seen on 15 ladders in the STAR radiation environment in 2014 Run first 2 weeks
- ***Latch-up phenomenon:***
  - Self feeding short circuit caused by single event upset
  - Can only be stopped by removing the power

*Inner layer damage: 14%*

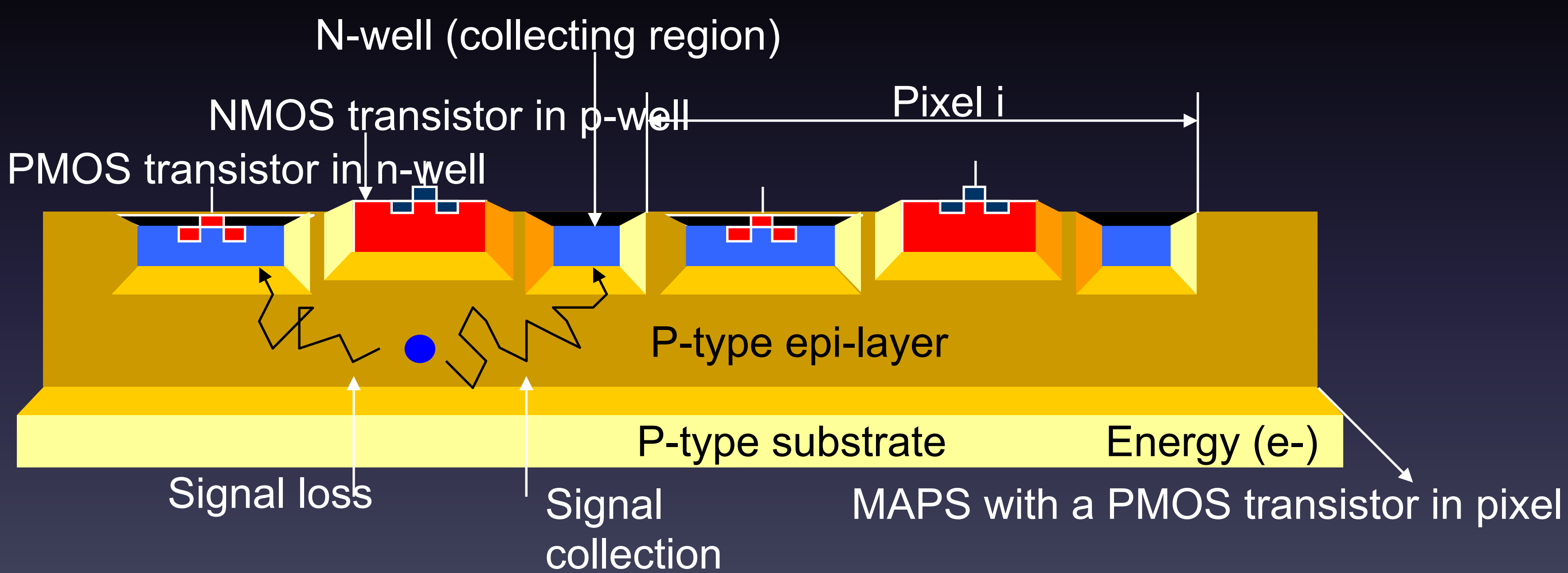


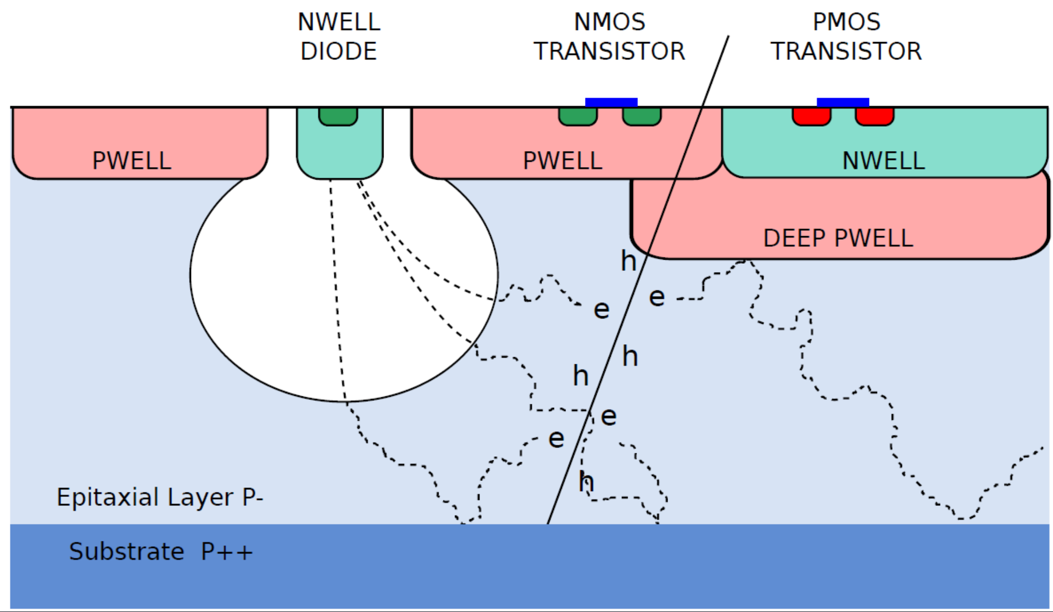

- Pixel sensor layers deconstructed (plasma etching technique) and viewed with SEM.
- The metal layer appears to be melted
- Safe operations envelope implemented
  - Latch-up protection at 80 mA above operating current
  - Periodic detector reset

# Full CMOS MAPS

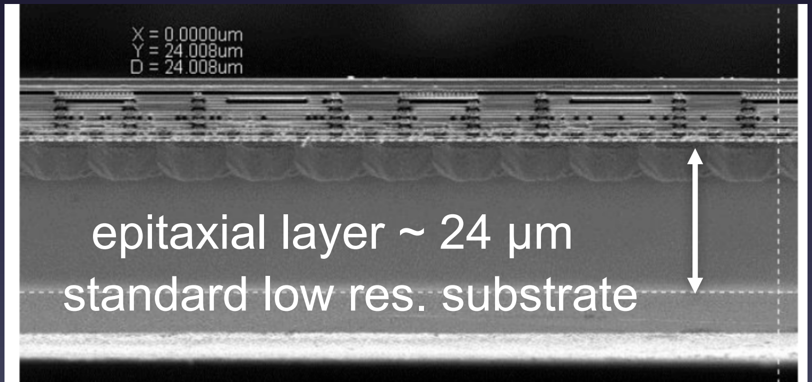
- If PMOS transistors are introduced, signal loss can happen



# INMAPS




- TowerJazz and Rutherford Appleton Laboratory
  - Deep P-Well to shield the PMOS transistors from epi layer
    - No charge loss occurs
    - Full CMOS ➠ Smart pixels possible
  - Disadvantages
    - Not a standard process ➠ limited number of producers




ALICE ITS, SEM picture of prototype chip

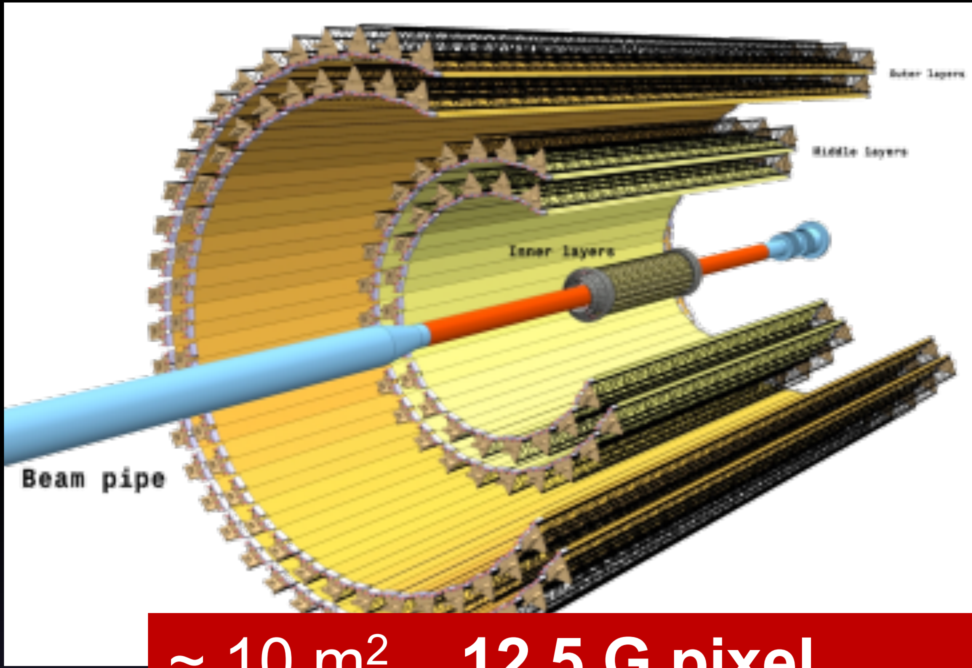
**Application in HEP: ALICE**

- INMAPS on High Resistivity resistivity (> 1kΩ cm) p-type epi-layer 18-40 µm thick
  - Moderate reverse bias to increase depletion zone around NWELL diode ➠ some charge collection by drift
  - Small n-well collecting diodes small ➠ $C_{in}$
  - Radiation tolerance (TID) to 700 krad (= 1/1500 of HL-LHC-pp)

R. Turchetta, W. Snoeys

# ALICE: MAPS

- Improve impact parameter resolution by a factor of ~3 in (r-$\phi$) and ~5 in (z)
  - –Closer to IP: 39 mm → 21 mm (layer 0)
  - –Reduce beampipe radius: 29 mm → 18.2 mm
  - –Reduce pixel size: (50 μm x 425 μm) → O(30 μm x 30 μm)
  - –Reduce material budget: 1.14 % $X_0$ → 0.3 % $X_0$ (inner layers)



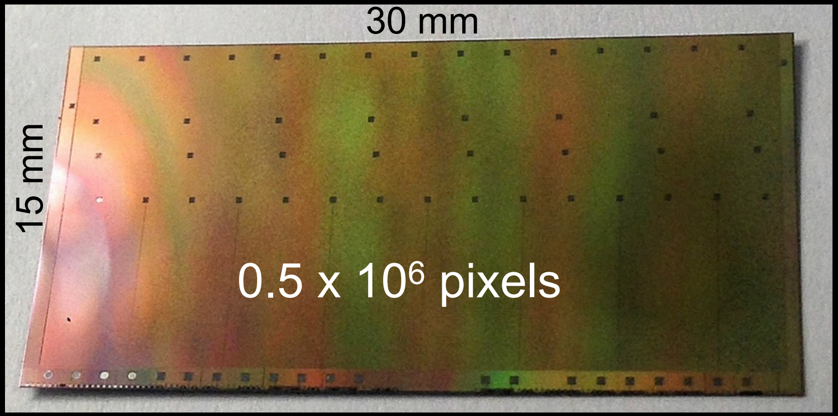

**~ 10 m$^2$ 12.5 G pixel**

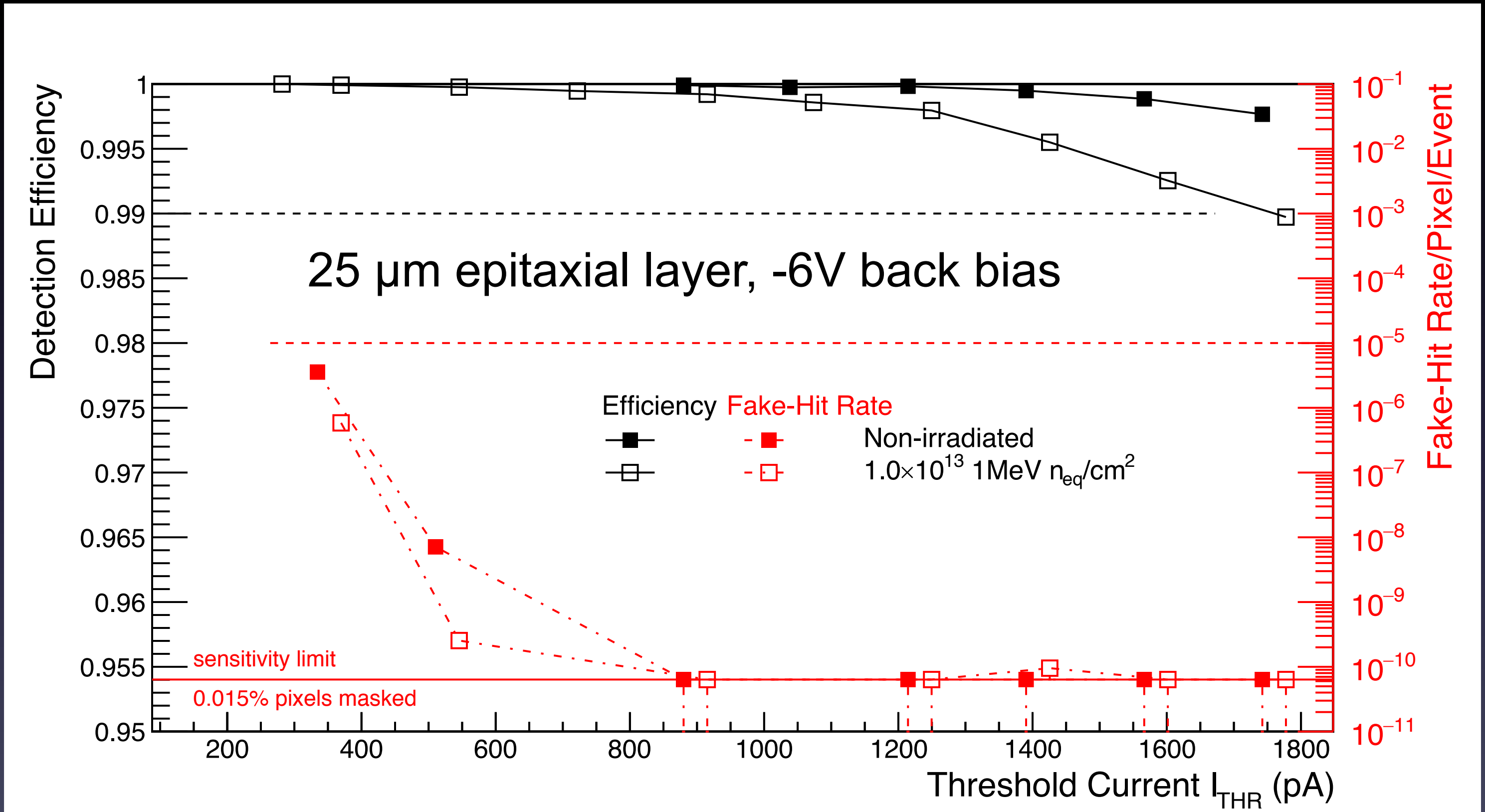
- High tracking efficiency and $p_T$ resolution
  - – Increase granularity and radial extension → 7 pixel layers
- Fast readout of Pb-Pb interactions at 50 kHz (now 1kHz) and 400 kHz in p-p interactions
- Rad hard to TID: 2.7 Mrad, NIEL: 1.7 x $10^{13}$ 1 MeV $n_{eq}$ $cm^{-2}$ (safety factor 10)
- Fast insertion/removal for maintenance

P. Riedler

# ALPIDE

- Pixel size: 29 x 27 μm² with low power front-end **~40 nW/pixel**
- Extensive tests before and after irradiation



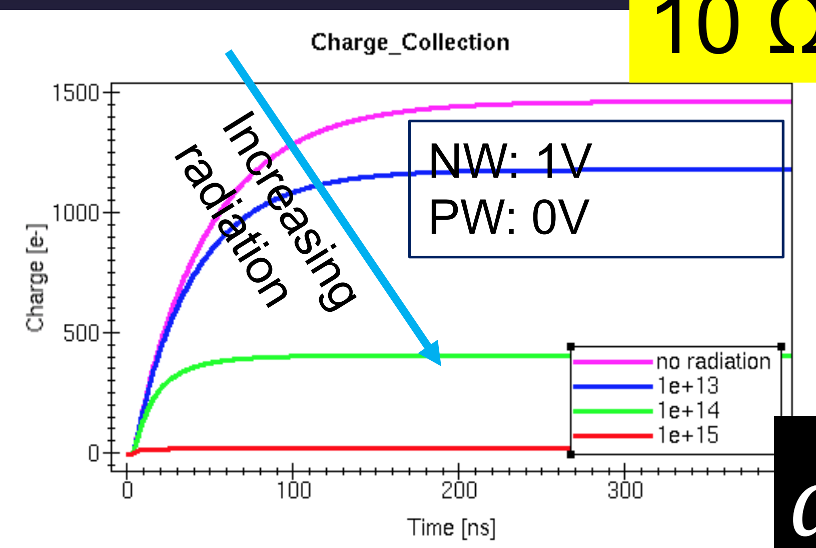

- **Efficiency > 99.5% and fake hit rate << $10^5$ over wide threshold range**
- **Excellent performance also after irradiation to $10^{13}$ (1MeV $n_{eq}$)/cm²**

# CMOS HL-LHC

- The rate/radiation environment of the HL-LHC is challenging but CMOS could:
  - Lower cost large area detectors using commercial fabs
  - More pixel layers in trackers
  - A reduction of material and power
- R&D is ongoing with the goal of:
  - Achieve a depletion depth of 40 – 80 μm
  - Fast charge collection (for < 25ns "in-time" collection)
  - Reasonably large signal ~4000 e-
  - Small collection distance to avoid trapping and increase rad hardness

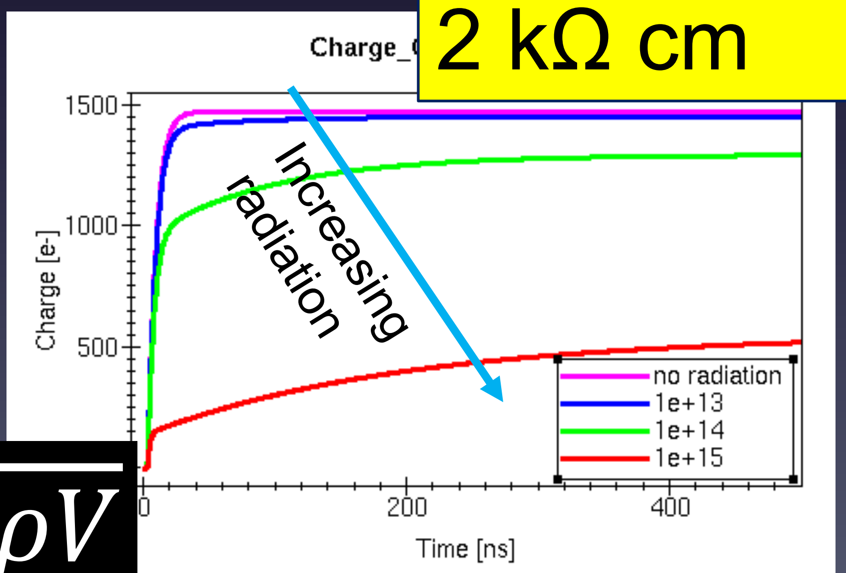
low resistivity

10 Ω cm




High resistivity

2 kΩ cm




$$d \propto \sqrt{\rho V}$$

# CMOS HL-LHC

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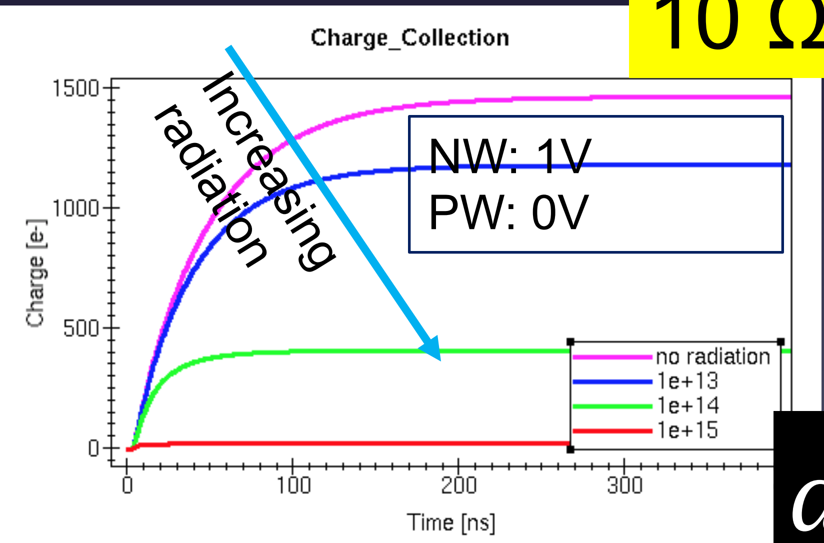
  - Small collection distance to avoid trapping  and increase rad hardness

low resistivity, low voltage

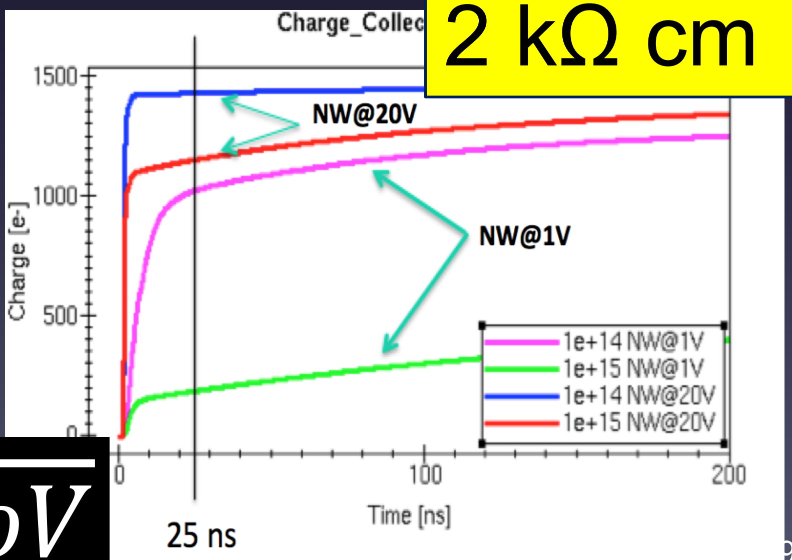
10 Ω cm




$$d \propto \sqrt{\rho V}$$

High resistivity, high voltage

2 kΩ cm

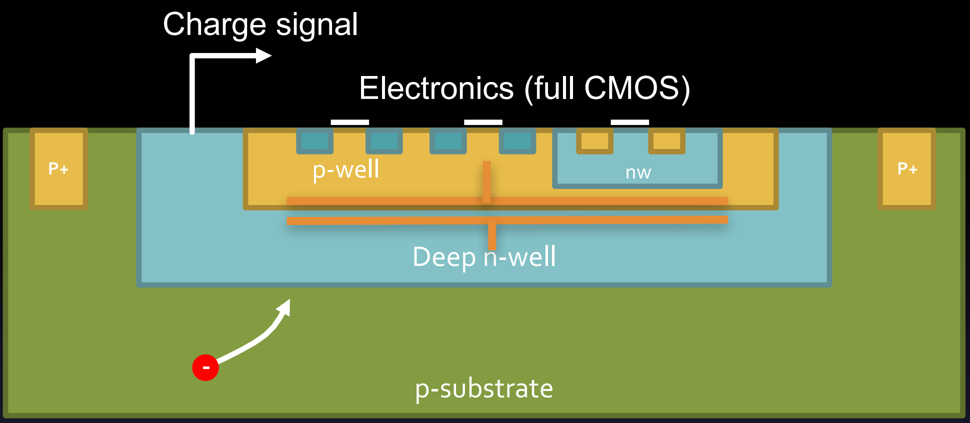


# Enabling technologies

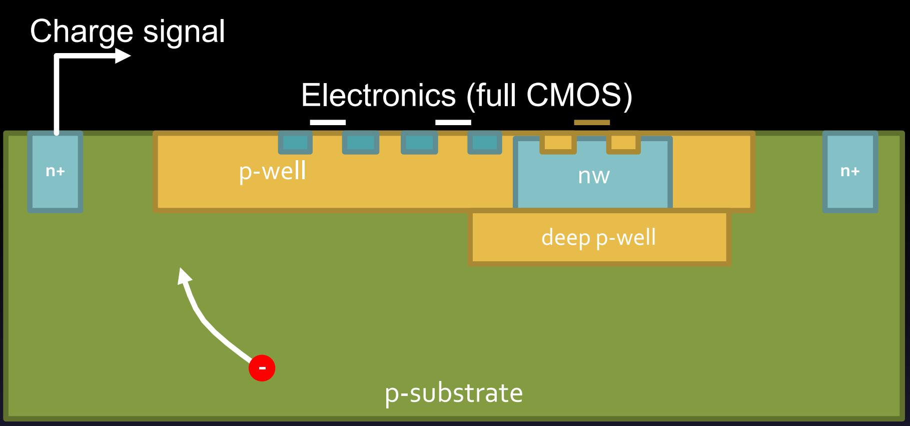
| | |
|---|---|
| • "High" Voltage | Special processing for automotive and power management application to allow the HV necessary to create a depletion layer in a well's pn-junction of o(10-15 μm). |
| • "High" resisitivity | Hi/mid resistivity silicon wafers accepted/qualified by the foundry to facilitate the needed depletion layer |
| • "Technology features | Radiation hard processes with multiple wells. Foundry must accept some process/DRC changes to optimize the design for HEP. |
| • Backside processing | Wafer thinning from backside and backside implant to fabricate a backside contact aner CMOS processing |

# R&D on DMAPS

## Electronics inside charge collection well



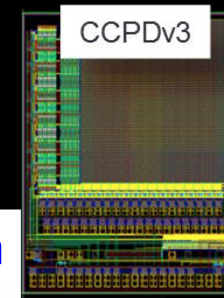

## Electronics outside collection well



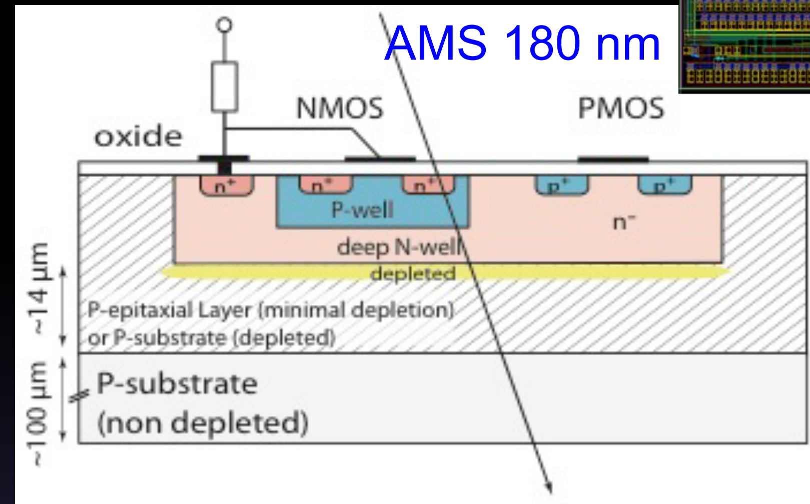

- Deep n and p wells
- Large collection node
- Large sensors capacitance sensor capacitance (DNW/PW junction!) ➠ X-talk, noise & speed (power) penalties
- Short drift path

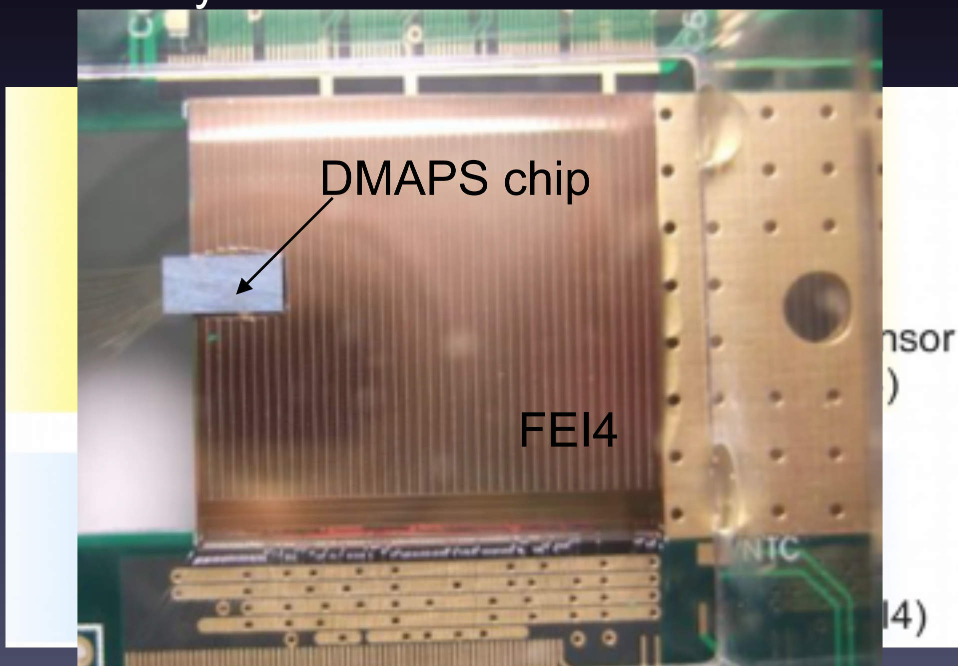
- Full CMOS with additional deep-p implant
- Small collection node
- Smaller capacitance ➠ less power
- Long drift path

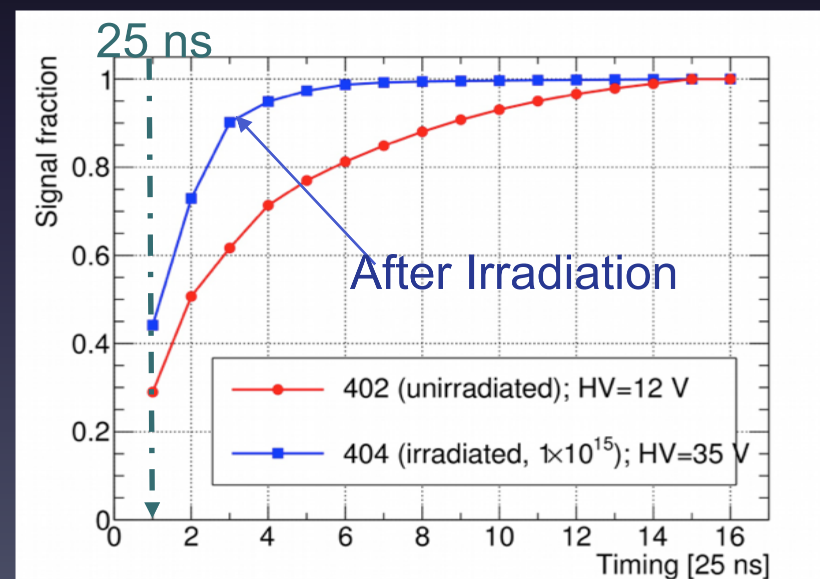
# R&D on HV/HR CMOS




- CCPD
  - triple well process
  - 10 Ωcm, 60 – 100 V
  - depletion depth 10-20 μm -> 100 μm after irradiation
  - ~1000 e- by drift
  - R/O by AC coupling to FEI4 via glue layer



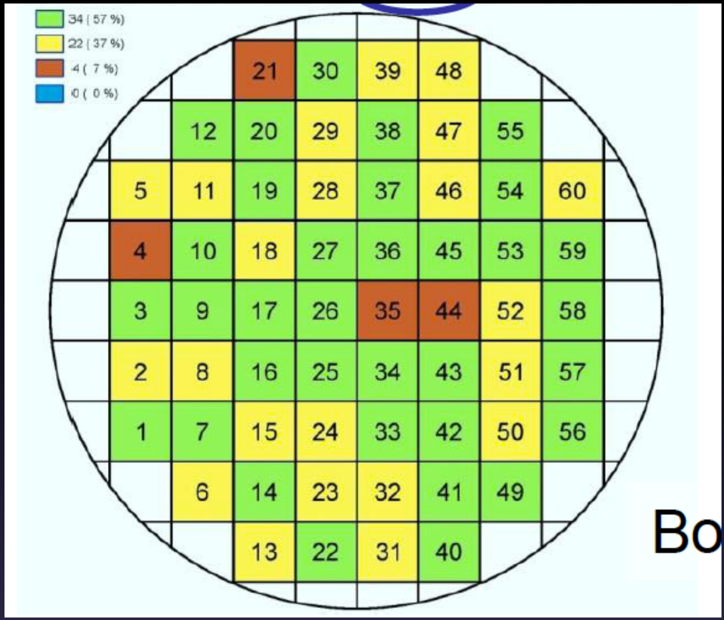



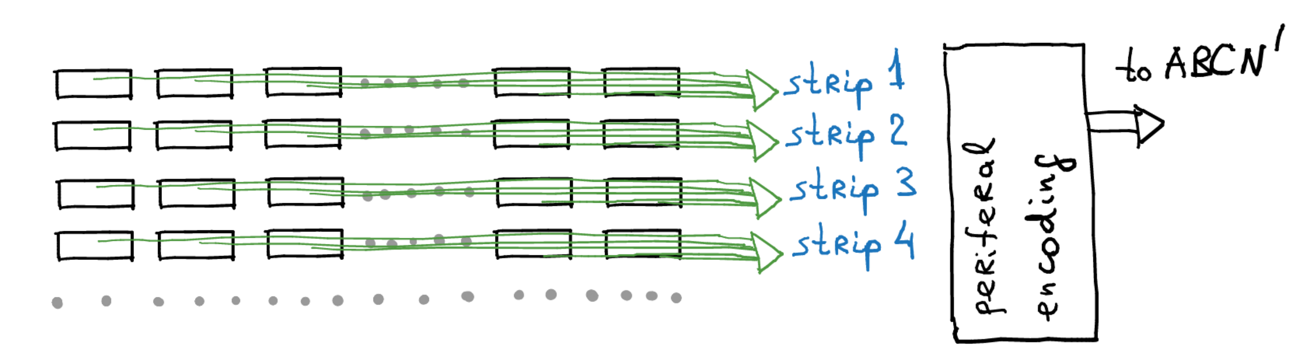



I. Peric et al., NIM A765 (2014) 172-176

# HV/HR-CMOS: strip

- Amplifiers and comparators could be on sensor but the rest of digital processing, command I/O, trigger pipelines, etc will go into a readout ASIC
- The active area is *pixelated*, with connections to the periphery that can yield 2D coordinates
- Pixel size ~40 μm x 800 μm
- Max reticle sizes are ~2x2 $cm^2$. Therefore rows of 4-5 chips could be the basic units (yield performance is critical here)

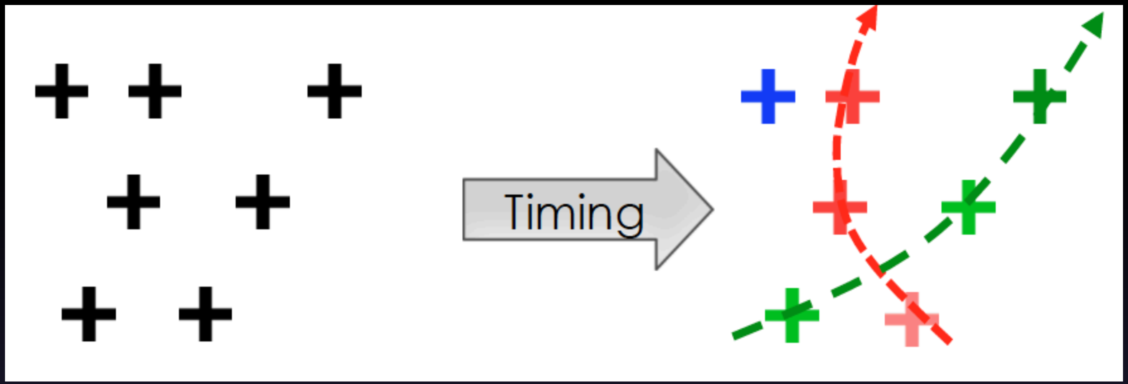



- Cost savings.
- Faster construction
- Less material in the tracker.

# 4D Tracking

- Timing at each point along the track:
  - Massive simplification of patter recognition
  - Faster tracking algorithm even in very dense environments by using only “time compatible points

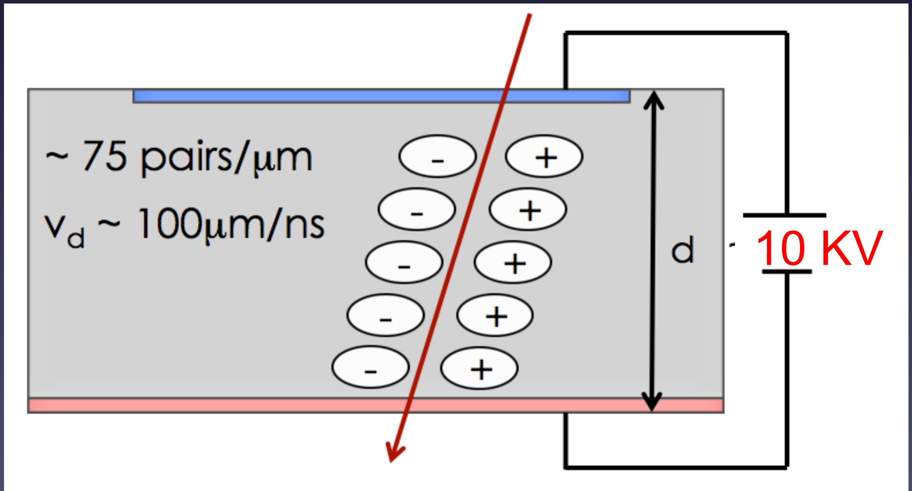



- Achieve ≈10 ps timing resolution with Si detectors using charge amplification with Low-Gain Avalanche Detectors

- Gain in silicon detectors is achieved through the avalanche mechanism which occurs when are accelerated by the electric field to energies sufficient to create mobile or free electron-hole pairs via collisions with bound electrons. Avalanche starts in high electric fields: E ~ 300 kV/cm

# Gain in Silicon

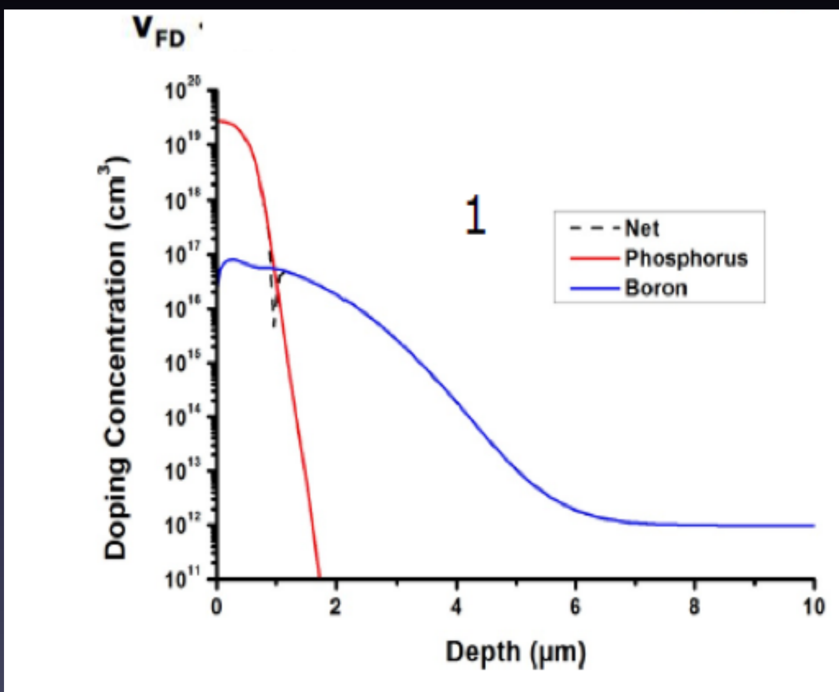
- Charge multiplication: $N(l)=N_0\, e^{\alpha l}$ and $G= e^{\alpha l}$
- Silicon devices with gain:
  - Avalanche Photo Diodes APD with G=5-500
  - SiPm $G=10^4$
- Use external bias: assuming a 300 micron thick silicon detector, we need $V_{bias}$ = 10 kV to achieve E ~ 300kV/cm

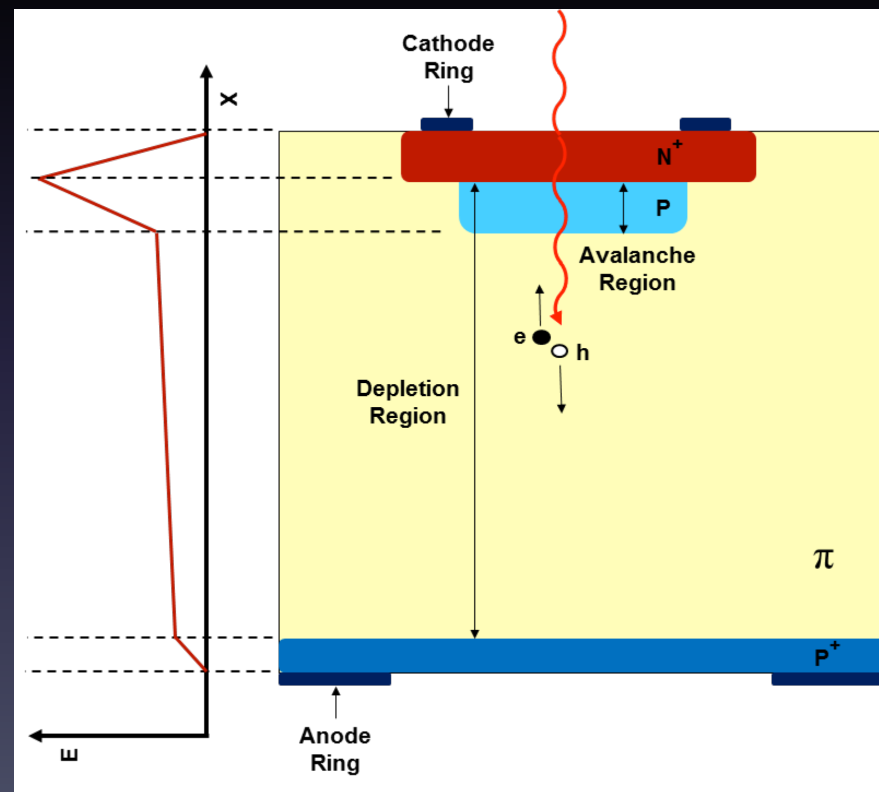



Not possible

# LGAD

- LGAD sensors obtain the high E-field by adding an extra doping layer



# Current from thin and thick detectors

- Thick detectors have higher number of charges

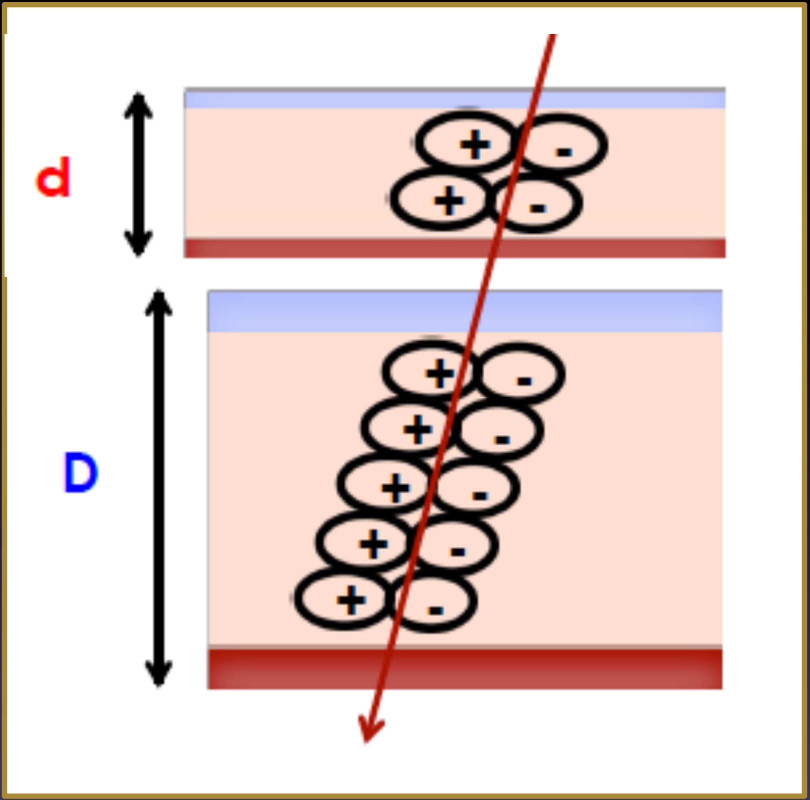
  $Q_{tot}$~75qd

- However the charge contributes to the initial current as

$$i = -\frac{dQ}{dt} = q\vec{E}_W\vec{v}$$

Shockley-Ramo Theorem

$E_W$=weighting field determines how the charge couples to the electrode




$$i = (75qd)\frac{k}{d}v = 75\ kv = 1\text{-}2 \times 10^{-6}\ A$$

The initial current is constant

# Gain and thickness

- The rate of particles produced by the gain does not depend on the thickness
- The gain current depends on d (via the weighting field)

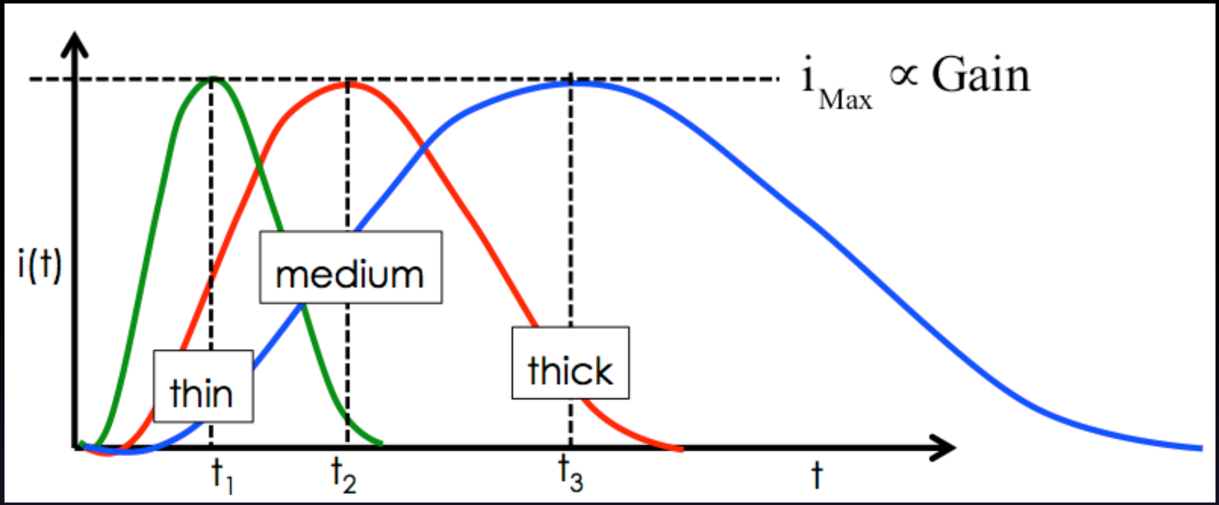
$$di_{gain} \propto dN_{Gain} q v_{sat} \left(\frac{k}{d}\right)$$

- A given value of gain has much more effect on thin detectors

$$\frac{di_{gain}}{i} \propto \frac{dN_{Gain} q v_{sat} \frac{k}{d}}{k q v_{sat}} = \frac{75(v_{sat} dt) G q v_{sat} \frac{k}{d}}{k q v_{sat}} \propto \frac{G}{d} dt \quad !!!$$

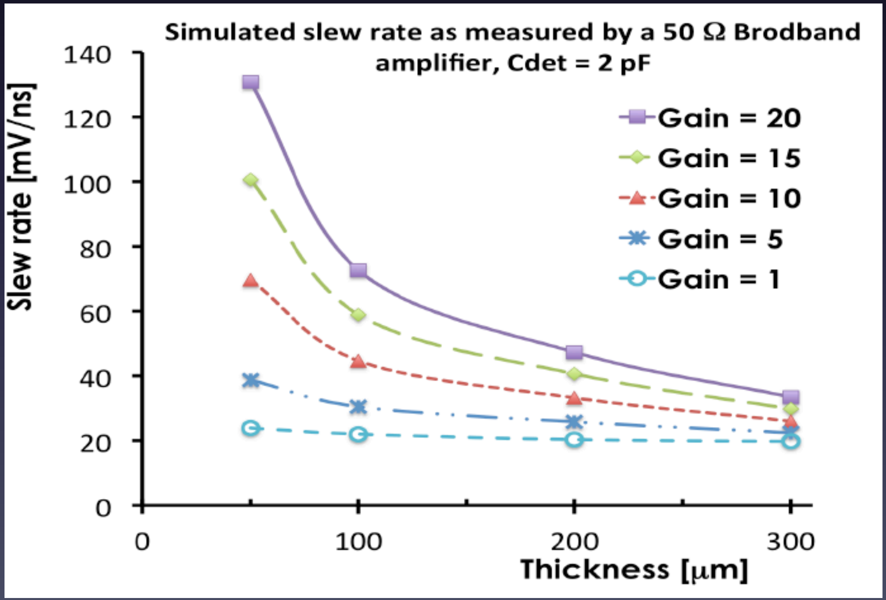
# LGAD

•




For a fixed gain:

- amplitude = constant
- rise time ~ 1/thickness




Slew rate:

- Increases with gain
- Increases ~ 1/thickness

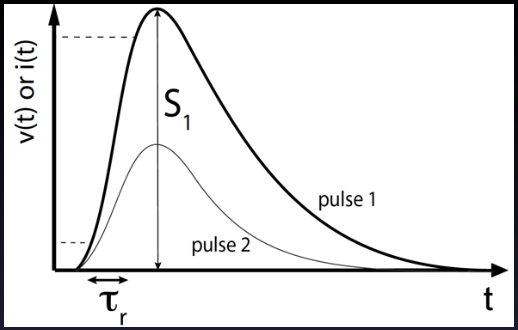
$$\frac{dV}{dt} \propto \frac{G}{d}$$

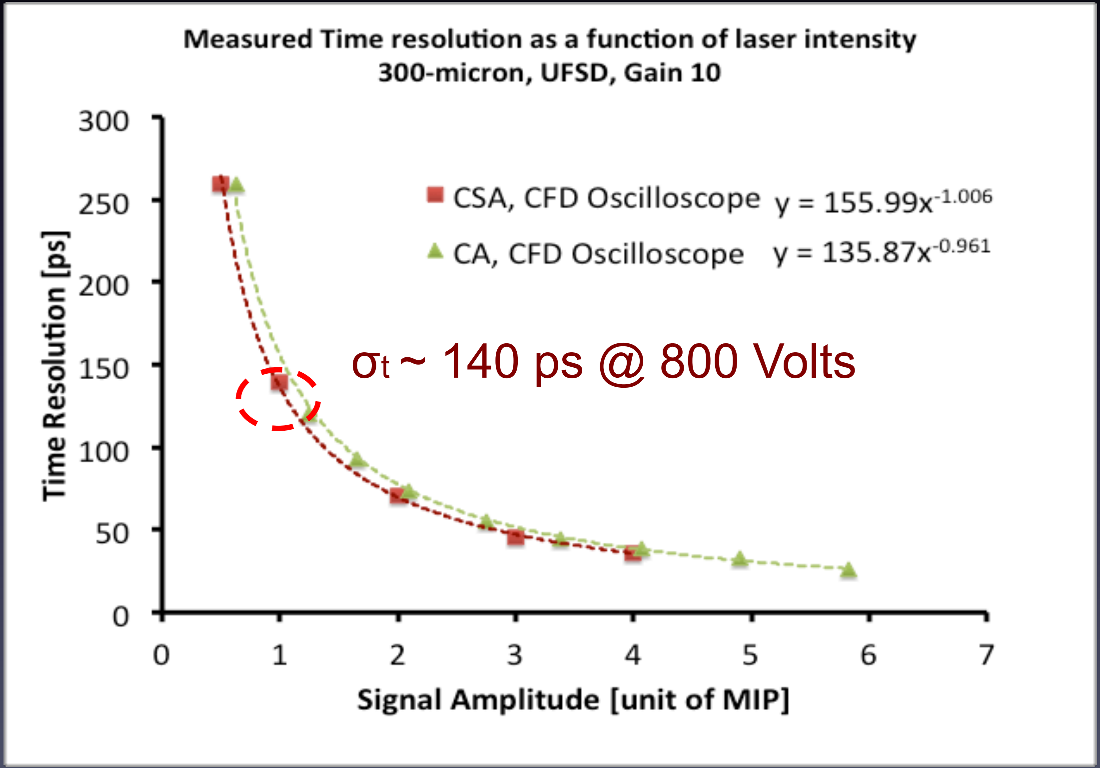
# Time resolution

- Figure of merit for $\sigma_t$ is the "slew rate" $dV/dt \approx Signal/\tau_{rise}$

$$\sigma_t^2 = \underbrace{\left( \frac{V_{th}}{dV/dt}\bigg|_{rms} \right)^2}_{\text{signal time walk}} + \underbrace{\left( \frac{\text{Noise}}{dV/dt} \right)^2}_{\text{noise time jitter}} + \underbrace{\left( \frac{TDC_{bin}}{\sqrt{12}} \right)^2}_{\text{TDC binning}}$$

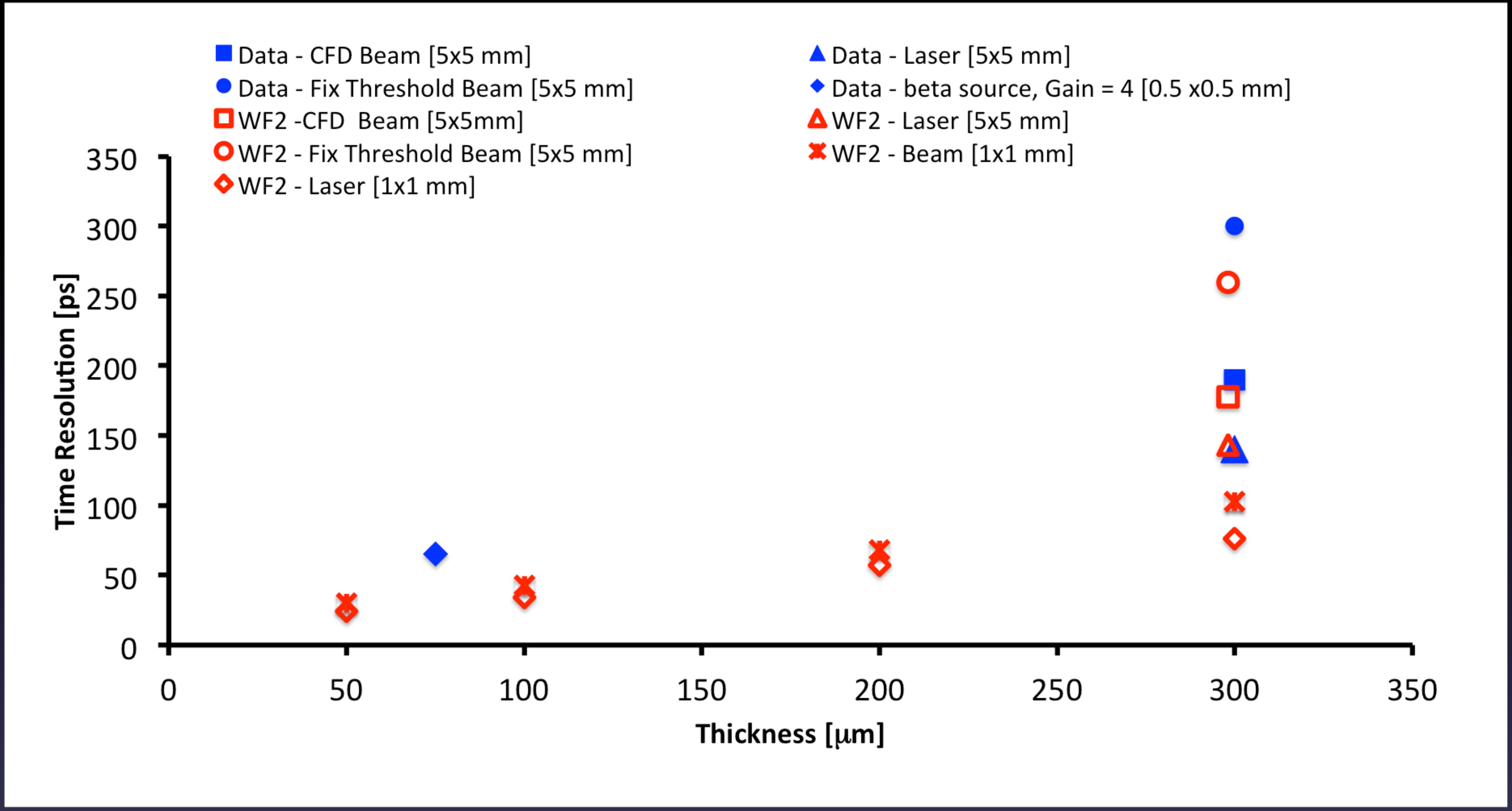
TDC binning can be made negligible




- Need: fast drift, large signals, low noise
  - $e^-$ drift velocity in saturation (E = 20 kV/cm, $v_D \approx 10^7$ cm/s)
  - collect electrons fast ➠ thin detectors
  - large signals ➠ gain
  - small C, small $i_{leak}$ , low noise ➠ small electrodes
  - broad-band amplifier

# Time resolution




R&D ongoing with CNM and FBK to make thinner faster detectors

# Conclusions

- Tracking is essential to the reach our ambitious physics goals
- Technologies come and go but the use of silicon sensor for tracking is not yet going

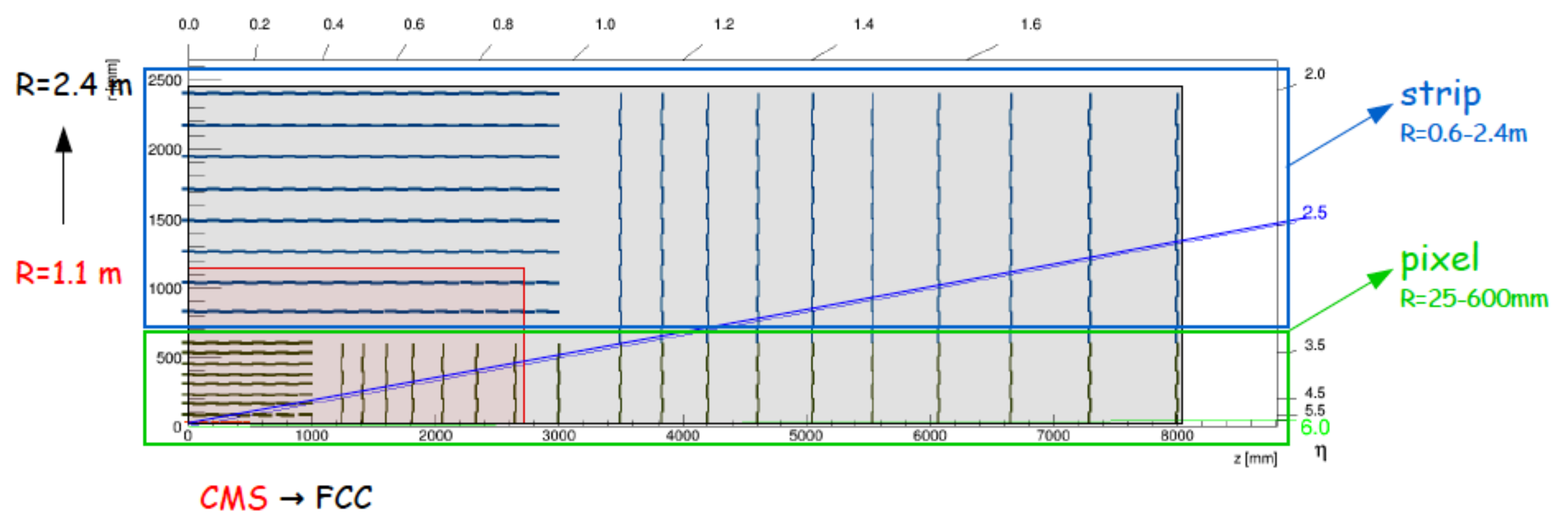

- Larger: >>200 $m^2$ (FCC-HH)
- More channels: Giga pixels
- Thinner: 20 μm
- Less noise
- Better resolution

# References

- Interaction with Matter & detectors:
  - CERN Summer school lectures (D. Bortoletto, W. Reigler): https://indico.cern.ch/event/387976/
  - The Physics of Particle detectors- DESY- organized by E. Garutti http://www.desy.de/~garutti/LECTURES/ParticleDetectorSS12/Lectures_SS2012.ht
  - CERN-Fermilab Hadron Collider Physics Summer School: http://hcpss.fnal.gov/hcpss14/
- Silicon: Manfred Krammer http://www.hephy.at/fileadmin/user_upload/Lehre/Unterlagen/Praktikum/Halbleiterdetektoren.pdf
- CMOS:
  - I. Peric :https://indico.cern.ch/event/237380/
  - W.Snoyes https://agenda.infn.it/getFile.py/access?contribId=62&resId=0&materialId=slides&confId=8834
- Tracking
  - Excellent lectures on tracking algorithms by A. Saltzburger at HCPSS2014
  - Previous CERN academic lecture by P. Wells https://indico.cern.ch/event/526765/
- New ideas for silicon detectors:
  - Great summary by Norbert Wermes at VCI 2016: https://indico.cern.ch/event/391665/sessions/160850/#20160215
  - TWEPP: Topical Workshop on electronic for Particle Physics. Excellent talk by F. Faccio on radiation effects on electronics
  - VCI, VERTEX, PIXEL, Trento workshops

# FCC

- Tracker Detector evolution for the FCC



# Thin sensors

- Reduced material
- Reduced $_{ILeakage}$
- Planar sensors: work at $2x10^{16}\ n_{eq}/cm^2$
  - need high bias voltage
  - n in n (inner),
  - n in p (outer layers)
- Slim edges (both for 3D and planar