Microdetector Electronics

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Fermilab Institutional Review
June 6-9, 2011

U.S. DEPARTMENT OF ENERGY

Fermilab

Outline

- Introduction: mission and resources
- ASICs/sensors projects and technologies
- Integrated solutions: 3D
- Integrated solutions: monolithic
- Ongoing development for experiments
- Conclusion

Mission

- Provide integrated circuits for detectors to run experiments
- R&D on detectors for future

- Primarily: instrumentation for HEP;
  secondarily: where synergies and where appropriate
  - leverage technologies for other fields and work through collaborations

Resources

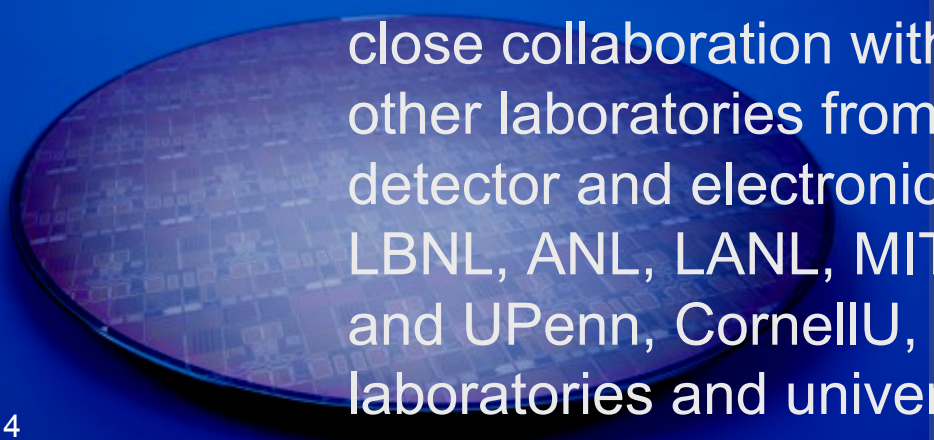
Team:
PPD/EED

- 6 ASIC designers (3 PhDs)
- 1 engineering physicist (PhD)
- 2 test engineers
- 1 technician

+ depending on needs 1 PCB drafter

+ occasional support from other resources within PPD/EED, CD and other departments at Fermilab

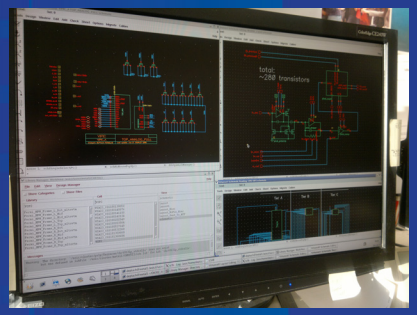
close collaboration with: physicists from Fermilab and other laboratories from the US and abroad and with detector and electronics development teams BNL, LBNL, ANL, LANL, MIT-LL, SANDIA, CERN, KEK, and UPenn, CornellU, GT, SMU ... + numerous laboratories and universities

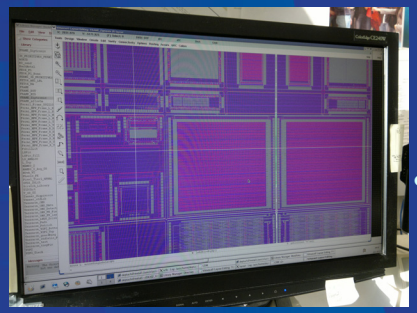


Tezzaron wafer for 3D chips from Fermilab MPW run

Resources: Software

Current Tools:





- **Cadence – Mentor Graphics – Magma – – Silvaco – Tanner**
  set of selected tools – significant cost, but unavoidable to fulfill needs, stay competitive and innovative
  from schematic entry, analog/digital simulation, custom layout and limited automated layout, physical and functional verification, post layout simulation to tape out license: 6 seats (basic) + single seats of verification and advanced tools (no digital synthesis, place & route and delay verification)
- Software for tests
  LabView – VisualStudio C++, etc.

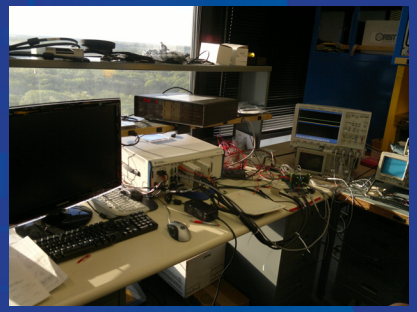
Tools to consider:

- Cadence Virtuoso Digital Implementation – limited version of RTL-to-GDSII for digital simulation, synthesis, floorplan, P&RVirtuoso (Cadence Encounter® RTL Compiler + Cadence Encounter® Digital Implementation System L)

Resources: Test and Characterization Infrastructure

Tools Current:

ASIC test lab



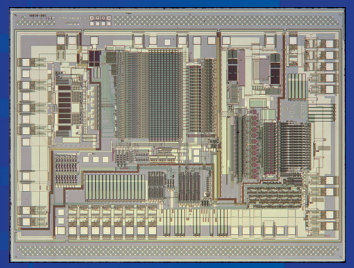
bench test setup

- **ASICs, transistors, sensors + systems**
  automated probe station 8” wafers
  robotic chip testing station
  manual bonding stations
  PCB components mounting station
  PXI/PXIe FlexRIO National Instruments digital/analog (ADC,LVDS,CMOS,DAC,DMM,power) system (LabView)
  parameter / spectrum / LCR / Logic / network analyzers
  V / I source, pA, digital oscilloscopes, etc.

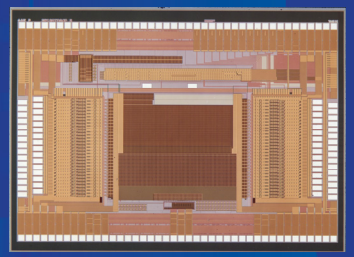
Tools Planned:

- Controlled temperature liquid He closed circuit cryogenic chamber T=RT↔70K
- X-ray irradiation chamber with on-wafer irradiation capability + detector testing with X-rays
- Dark box and parameter analyzer upgrade

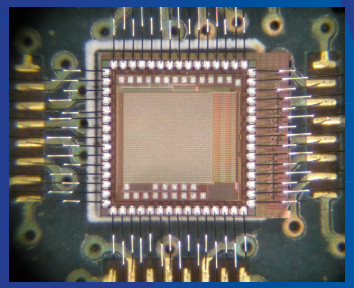
ASICs/sensors projects and technologies



QIE9



DCAL



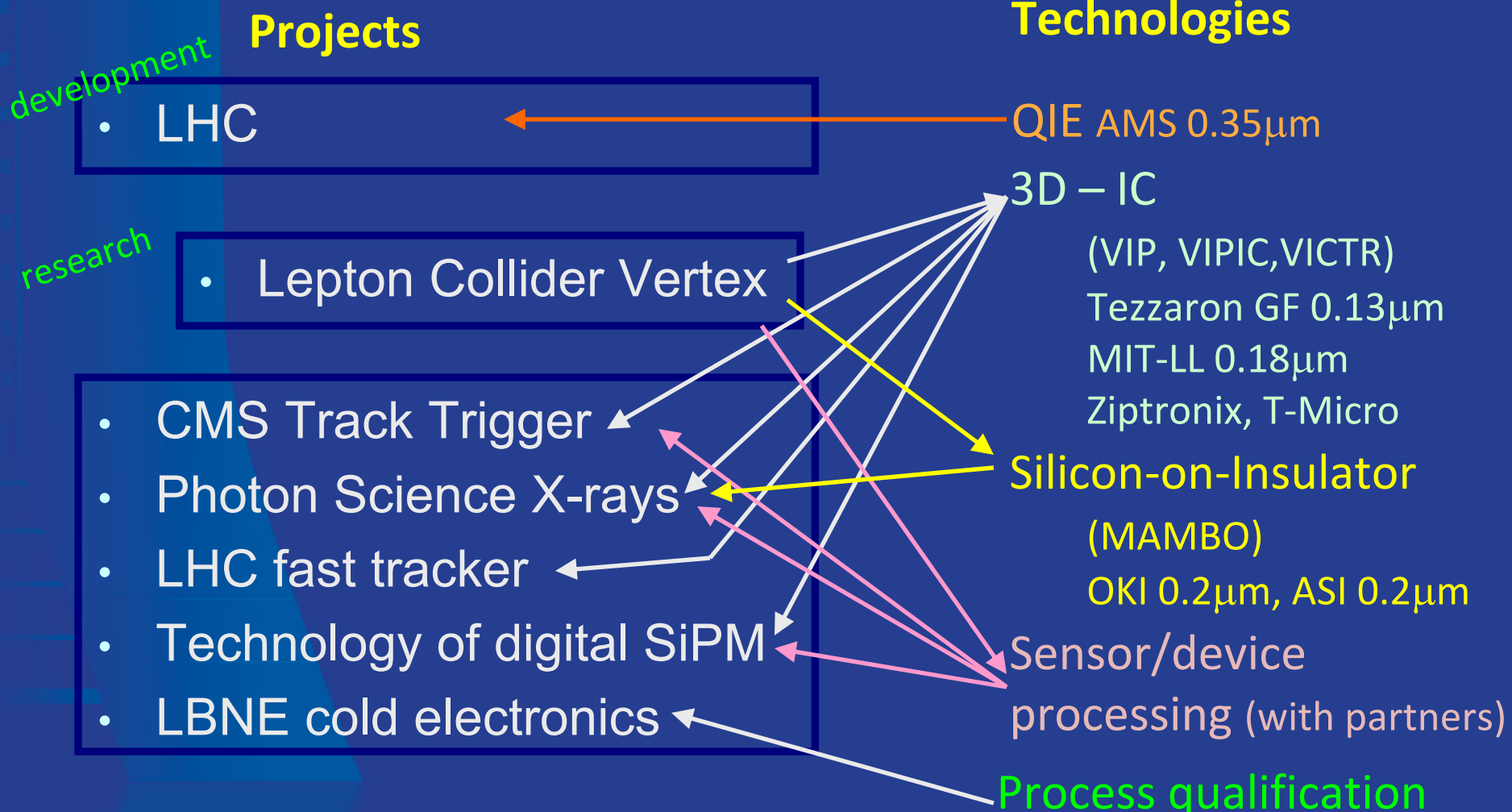
VIP2a 3D-IC

- Electronics and sensor technology is central to Particle Physics research – leads to spinoffs to domains using detection techniques of the same kind
- Industrial technology is moving rapidly – science is a niche market – leverage of technologies for advancing instruments of capabilities which have so far not even dreamed of
- Sensor arrays of unprecedented sizes and in-situ processing
  - CMS tracker-trigger
  - LHC in hardware tracker (content addressable/associative memories)
  - solid state PM (G-APD, SiPM)
  - photon science instr. (X-ray Photon Correlation Spectroscopy - BNL)
  - DE focal planes

  and more
- There are many HEP opportunities, we need to take care to use resources wisely
- Prospects of cooperation beyond HEP (different timescales) - resources must be managed even more carefully

ASICs/sensors projects and technologies

Currently:



ASICs/sensors projects and technologies

Future brings new challenges – research in electronics/detector technologies is building a toolbox to deal with these challenges

challenges are multidimensional:

- Unprecedented impact parameter resolution
- Transparency (no mass)
- Radiation backgrounds
- Precise timing – time resolution
- Unprecedented occupancy
- Large scales of systems
- Enormous quantities of raw data – in situ processing
- Increased heat production and heat evacuation
- Cryogenic extreme operation condition
- Nanoscale limits for device operations
- Single photon sensitivity, low dark current rates
- Unprecedented need for yield and reliability

Integrated solutions: 3D

- Particular set of challenges of the ILC's vertex detector led to complex circuitry.
- Initially small efforts, started at Fermilab, aroused great interest among the detector community worldwide and eventually materialized in the 3D-IC consortium formed and led by Fermilab

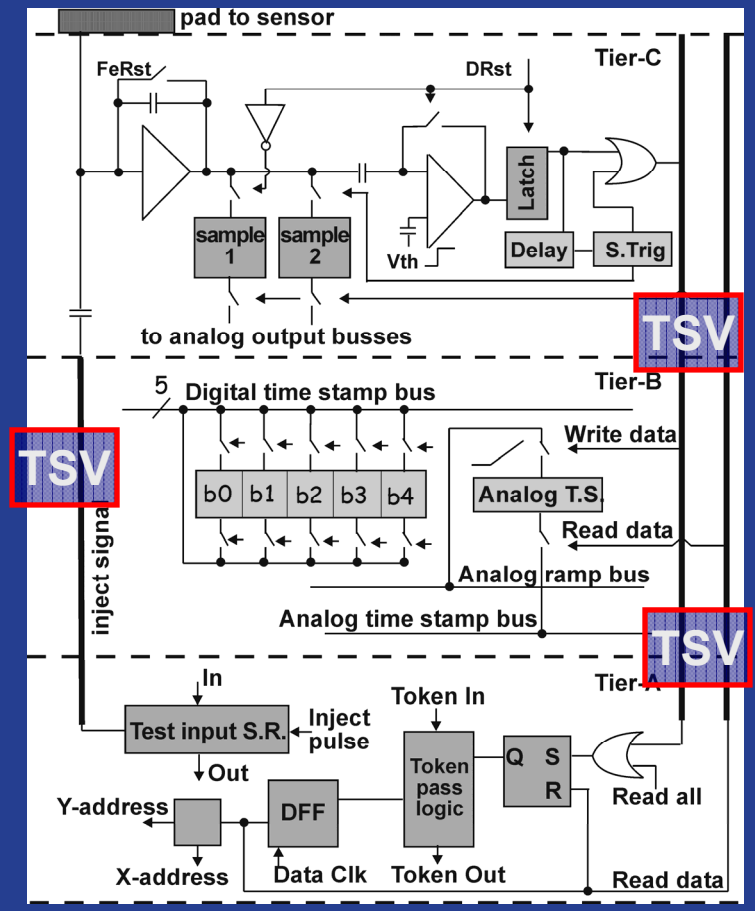
ILC VXD must:

provide spatial resolution of single point particle impact better than σ=5 μm

deal with congested hit patterns 252 hits/beam train/mm^2

- **pixel size ~20×20 μm^2, detector 50-100 μm/layer**
- **spatial resolution improved by interpolation**
- **data driven, fast, sparsified readout**
- **groups of BXs timed**

Fitting # transistors can be achieved only with 3D – IC technology



3tier pixel scheme of VIP for ILC

Integrated solutions: 3D

Why?

- Current fine-grained detector technologies face serious limitations; incremental improvements have proved inadequate
- 3D integration offers a transformational change to address current roadblocks to advance detectors in these areas

3D-IC definition:

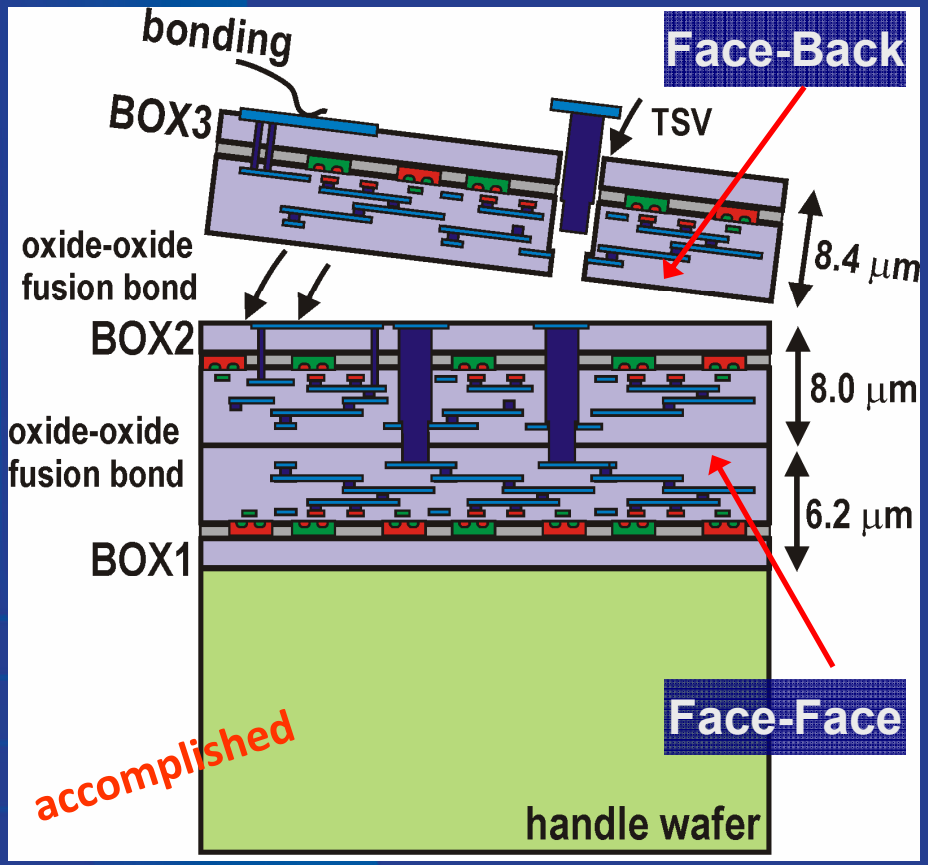
A chip in three-dimensional integrated circuit (3D-IC) technology is composed of two or more layers of active electronic components, integrated both vertically and horizontally

3D-IC (revolution) technologies:

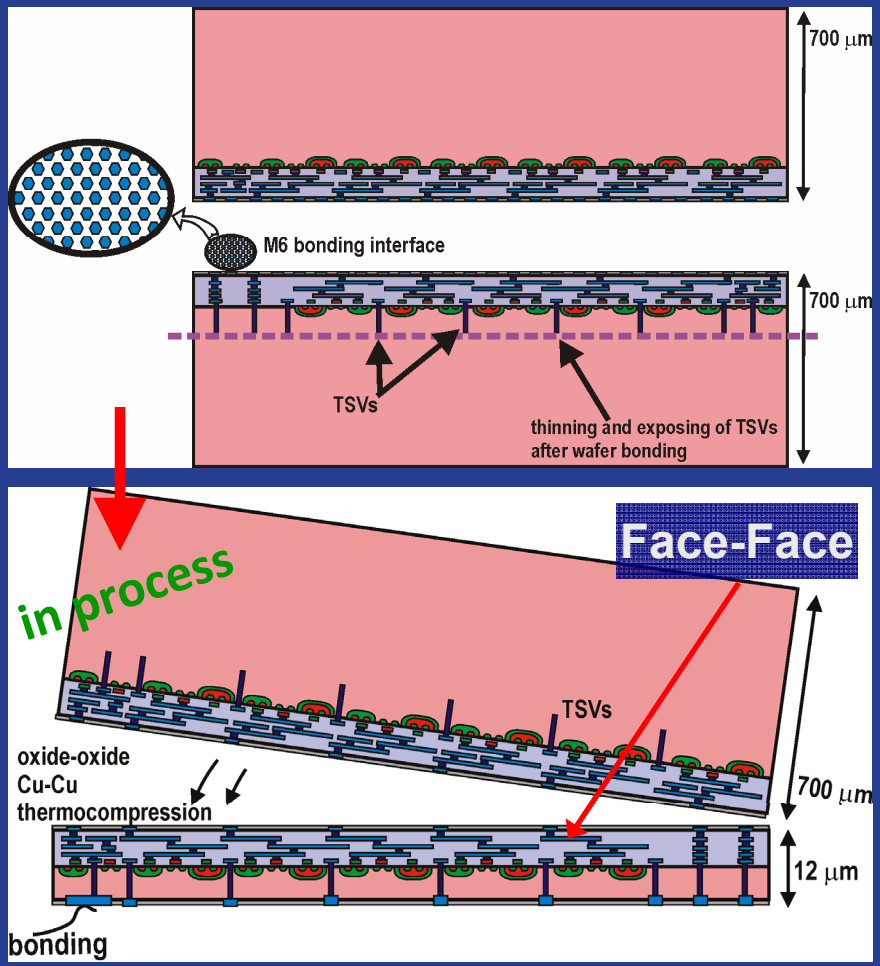
- Through Silicon Vias (TSV) for vertical wafer/chip connectivity
- Bonding: Oxide, polymer, metal, or adhesive strengthened (W-W, C-W, C-C)
- Wafer thinning: agressive and precise
- Back-side metallization and patterning

Integrated solutions: 3D

- experience with MIT-LL, RTI, Tezzaron, T-micro, Ziptronix



MIT-LL 0.18 / 015μm FDSOI
3 tiers, via-last ϕ=1.75μm

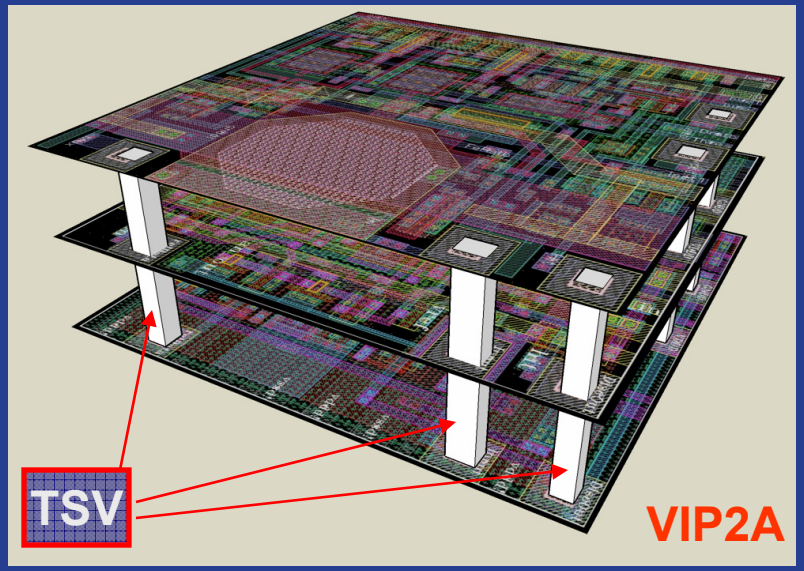


Tezzaron GF 013μm bulk, 2 tiers,
via-first/middle ϕ=1.3μm

Proof of principle, MIT-LL no longer available

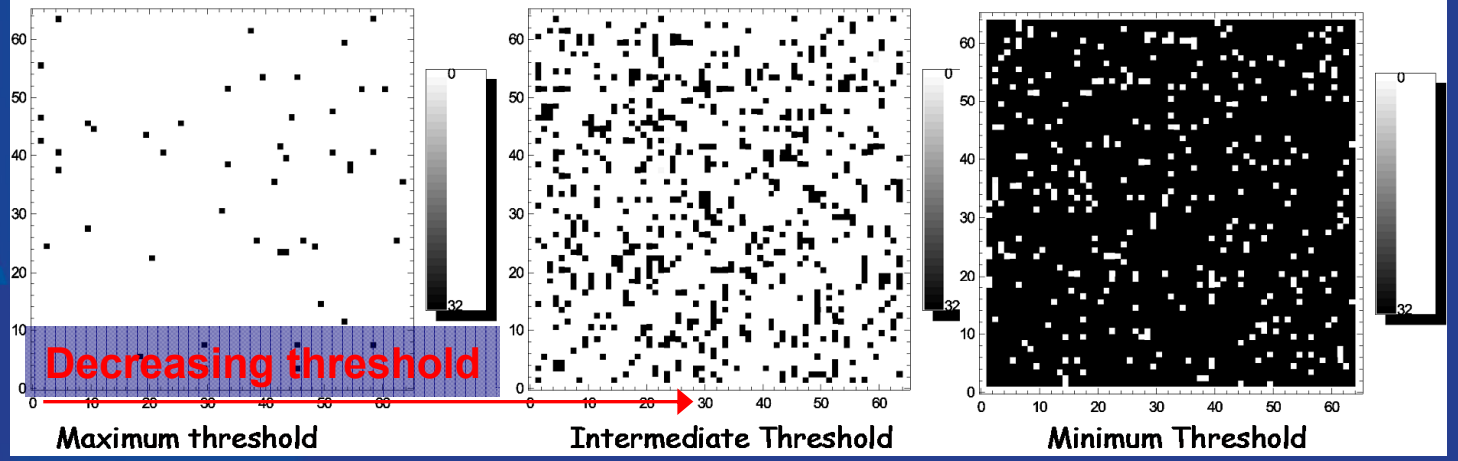
Integrated solutions: 3D MIT-LL

- 2 generations of Vertically Integrated Pixel (VIP1 & VIP2A) processing was lengthy: from 13 to 20 months to get devices back
- First iteration (Oct. 2006) had a number of processing difficulties
- Learned a lot about dealing with a leading edge R&D process -> good understanding
- Second iteration (Aug. 2008) with conservative design works well



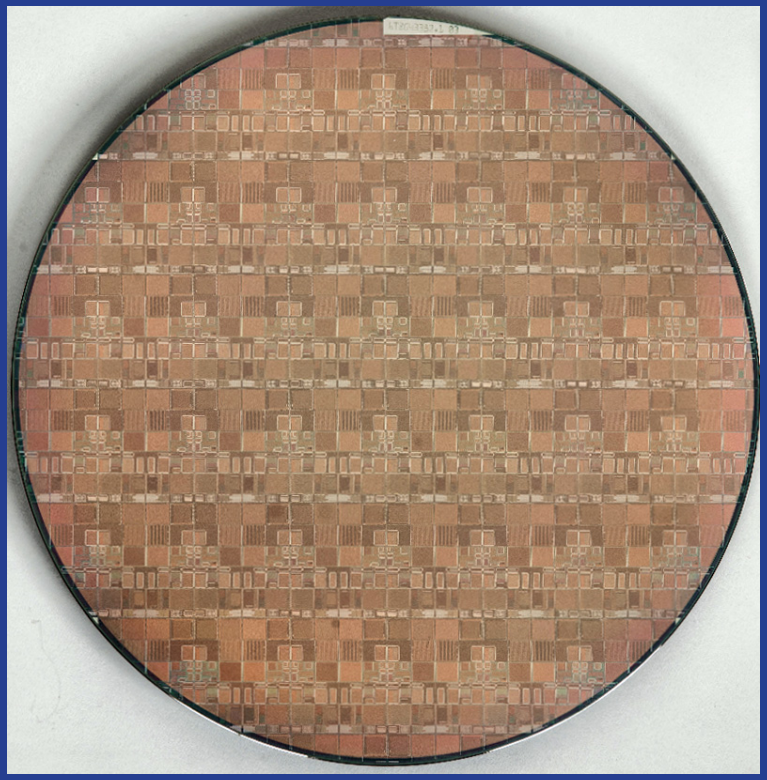
Chips were operational

Data readout out using data sparsification scheme.



Integrated solutions: 3D Consortium run

- Consortium established by Fermilab in late 2008, now 17 members; 6 countries (USA, Italy, France, Germany, Poland, Canada) with Tezzaron (IL)
- Initial designs for MPW (Multi Project Wafer) run completed in May 2009; Chartered (GF) 0.130 μm CMOS
- Numerous challenges were addressed with designs, software tools at Tezzaron, shifting Chartered requirements, etc.
- MPW frame accepted by Chartered in March 2010
- Fermilab, has worked closely with commercial brokers to establish MPW runs for 3D ICs



Tezzaron wafer for 3D chips from Fermilab MPW run

-- transfer --

http:\\3dic.fnal.gov

CNRS-INPG-UJF

CMC MICROSYSTEMS

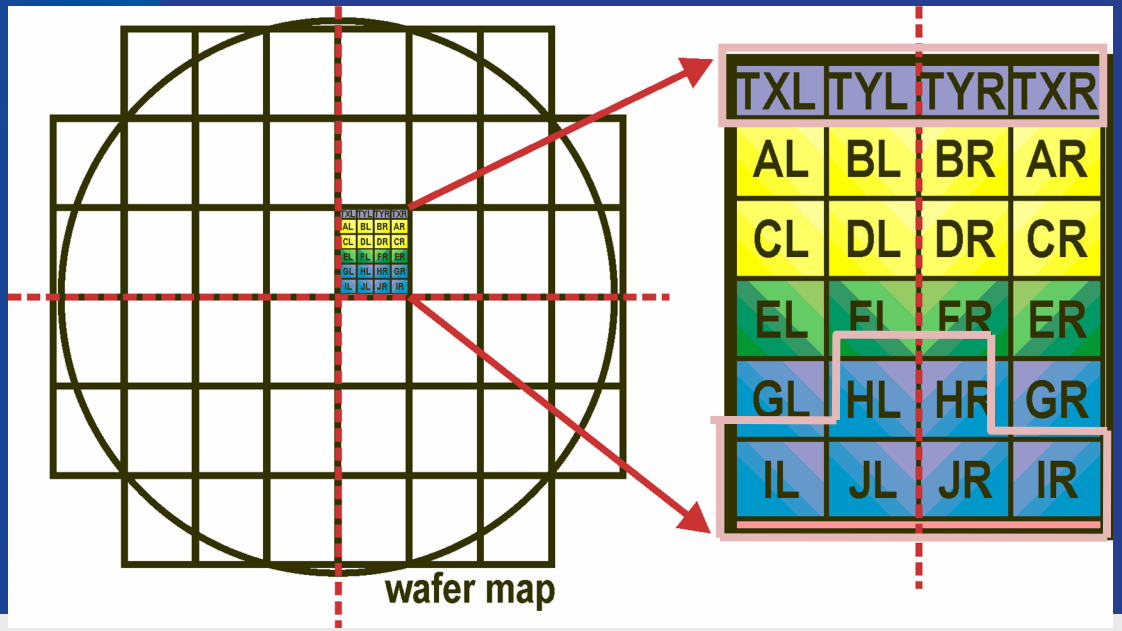
ANNOUNCEMENT

CMP/CMC/MOSIS partner to introduce a 3D-IC process

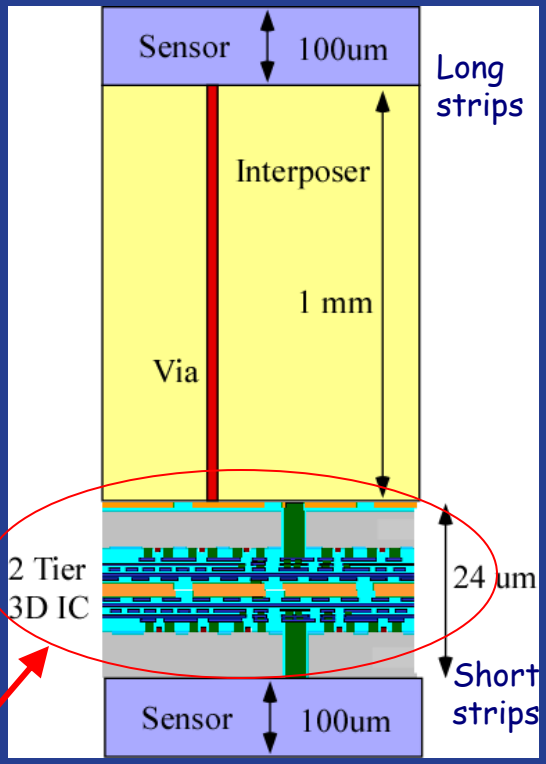
Grenoble, France, 22 June 2010, CMP/CMC/MOSIS are partnering to offer a 3D-IC MPW service based on Tezzaron's SuperContact technology and GLOBALFOUNDRIES 130nm CMOS.

Next run, first through CMP/CMC/MOSIS partnership, in 2011 once chips from the Fermilab run received and evaluated. Run subscribed by the HEP community, Commercial runs will take place too

Integrated solutions: 3D Fermilab designs

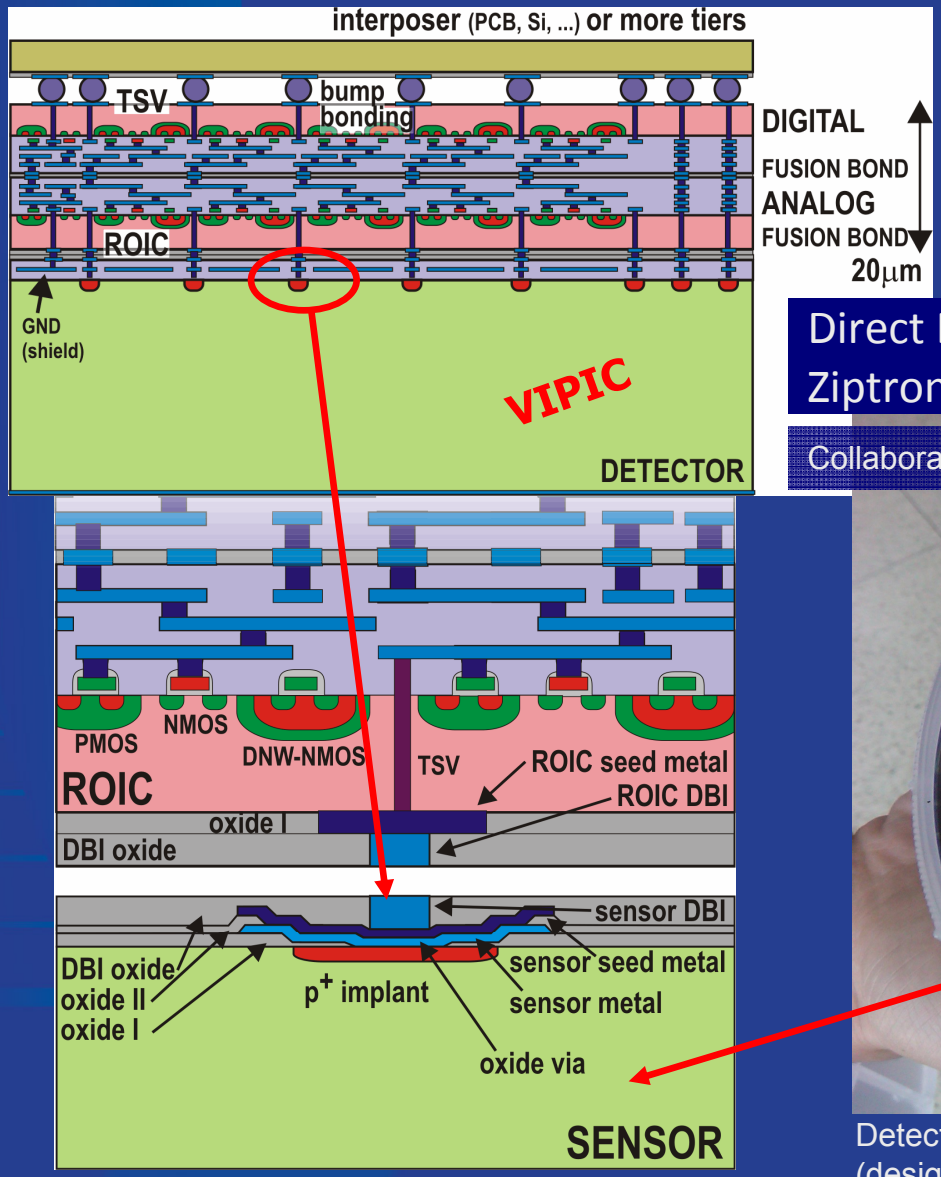


Division of the frame into 12 subreticule pairs: left-right.



- **H = VICTR**; short pixel realizing p_T cut for L1 trigger embedded in tracker for CMS @ SLHC (*particle physics*)
- **I = VIP2b**; time stamping pixel for vertex detector @ ILC (*particle physics*)
- **J = VIPIC**; very high frame rate with sparsification pixel for X-ray Photon Correlation Spectroscopy @ light source (*photon science*)
- **TX, TY**; test structures (single transistors and subcircuits)

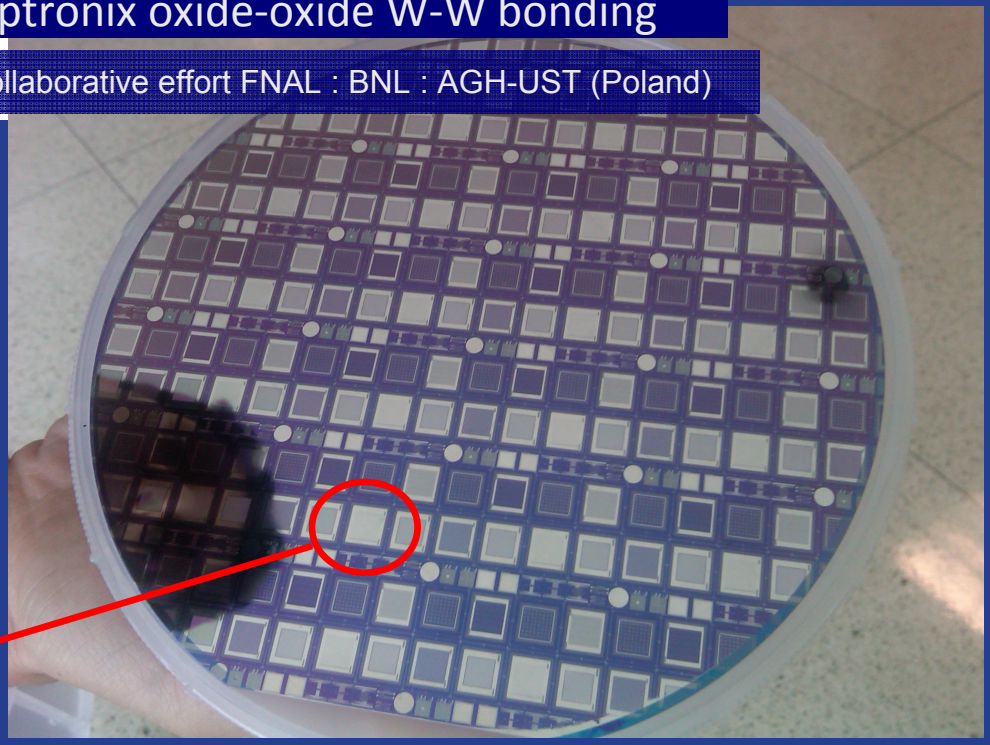
Integrated solutions: 3D Sensor integration



- 3D technologies can also be used to integrate sensors to ICs
- Pitches as small as 3μm, thinned to 25μm
- Provides for fully active sensors as large as 6" (or 8" wafer) based on tiled ROICs

Direct Bonding Interconnect (DBI®) by Ziptronix oxide-oxide W-W bonding

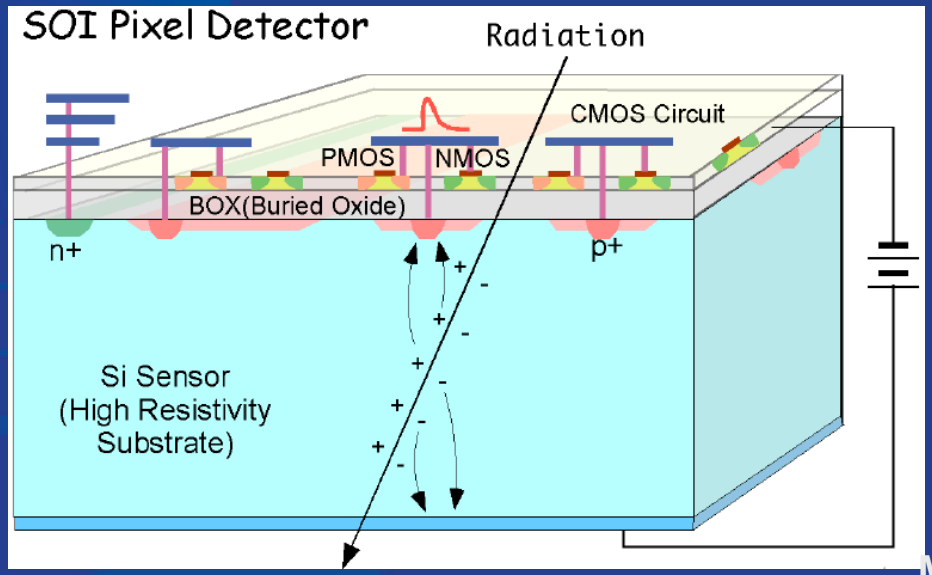
Collaborative effort FNAL : BNL : AGH-UST (Poland)



Detector wafer for 3D pixel chips from the MPW run (designed at Fermilab fabbed at BNL)

Integrated solutions: monolithic

- Silicon-on-insulator (SOI) devices with high resistivity (*up to 10kΩcm FZ*) detector handle wafers – OKI Semiconductor (SOIPIX collaboration led by KEK US-Japan Collaboration Funds) + ASI (SBIR)
- Truly integrated sensor/electronics - Monolithic structure: minimal interconnects, low node capacitance
- Supplementary / complementaty for 3D work (can be first layer of 3D)
- Can be back-thinned, back-side implanted, laser annealed, metalized - demonstrated by Fermilab



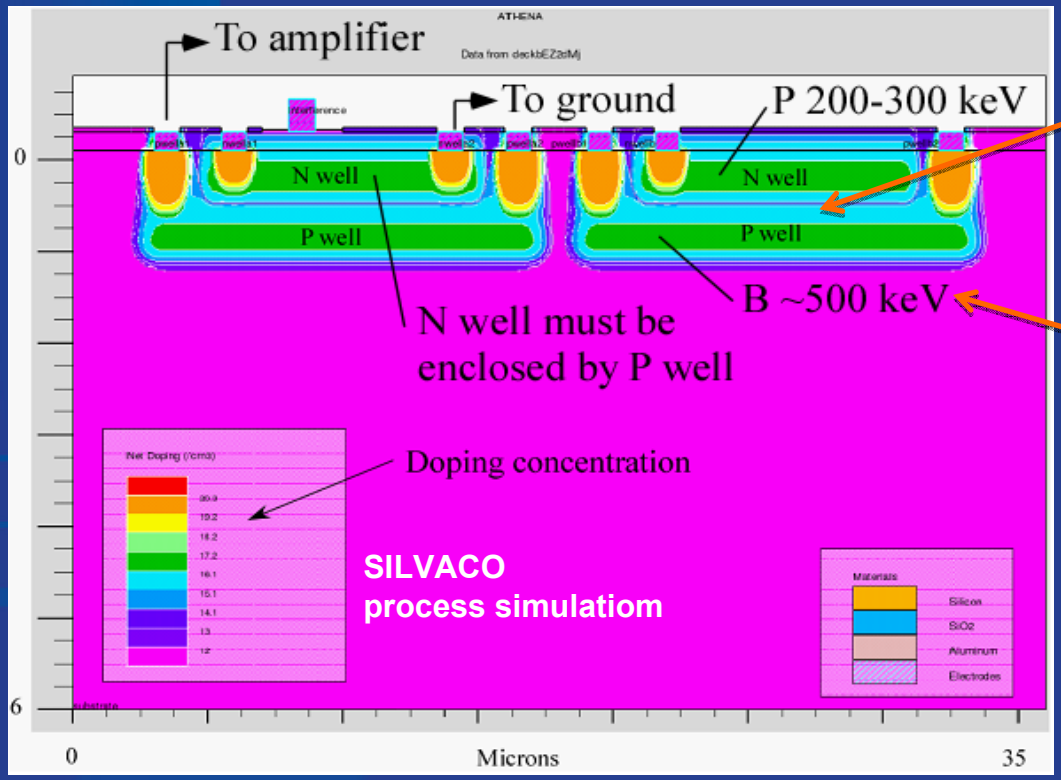
particularly suitable:
minimum scattering and
low energy range (soft X-ray detection)

Multi-year program at Fermilab:

5 prototype, pixelated structures developed and submited over last 5 years, 2.5×2.5 mm² and 5×5 mm², MAMBO Monolithic Active Matrix with Binary Counters

Integrated solutions: process improvements

- The potential of the substrate can change the fields at the top transistor and affect performance – "back-gate"
- Back-gate effects are significant in OKI process - limit bias that can be applied
- Digital-analog coupling can also destroy performance
- FNAL suggested process changes to OKI to fix this
- Initial tests show the chips are not affected by back potential any more



This well separates digital circuits from sensor substrate and prevents back gating effects

This well collects the charge

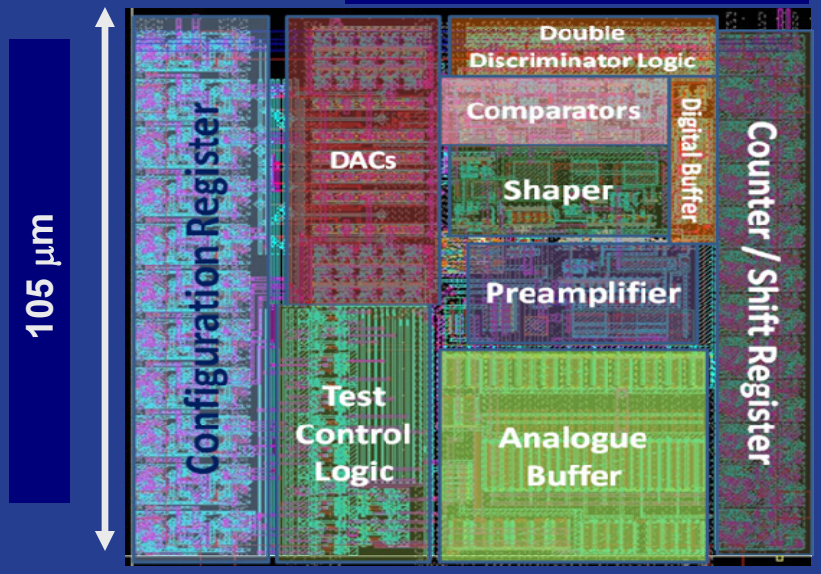
Patent application under discussion OKI-KEK-FNAL

Integrated solutions: monolithic

- MAMBO x-ray pixel imaging counting pixel chip with window discriminator (f_{MAX}= ~ 1 MHz)
- Each pixel: CSA, CR-RC^2 SHA, window discriminator + 12 bit binary counter

• MAMBO IV nested wells (105×105 μm^2, ~950 Ts/pix.)
Aug. 2010 -> Dec. 2010, under tests
• MAMBO III – the same as MIV but 3D with T-micro
Jan. 2010 -> still in bonding

MAMBO III and IV, pixel



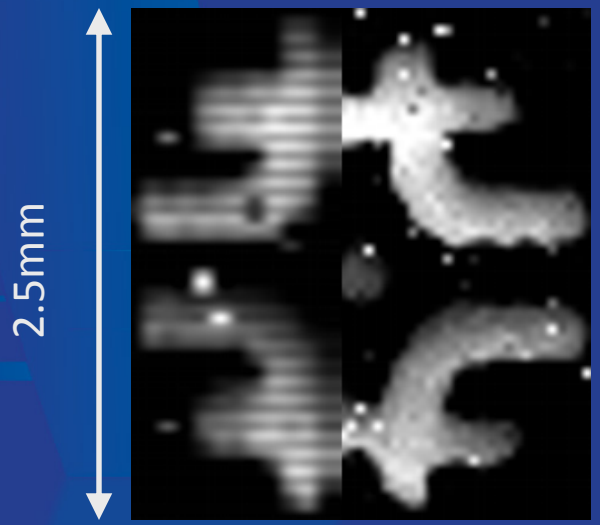
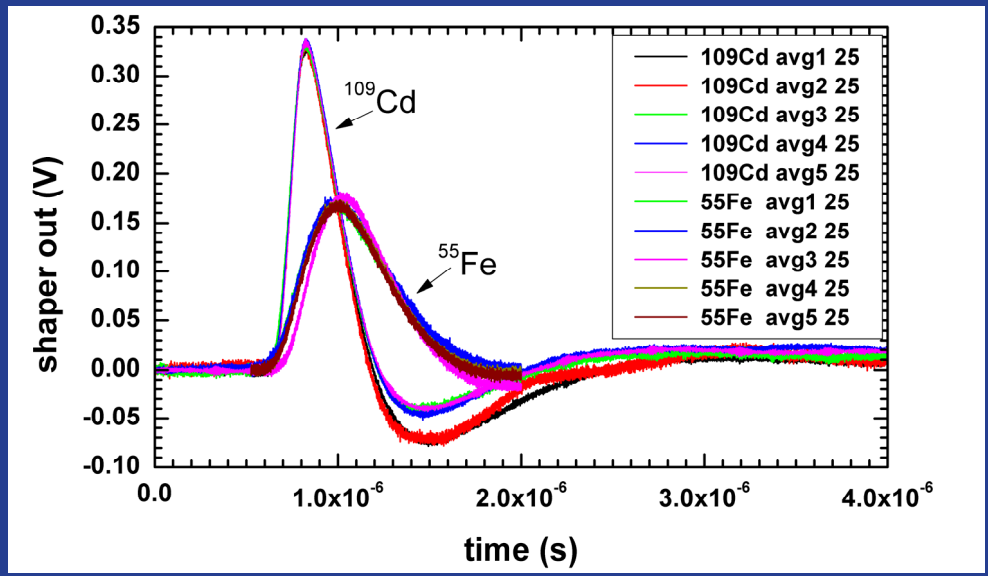


Image of Fermilab W logo integrating SOI pixel ^{109}Cd radioactive source



Response of analog to radioactive sources MAMBO II

Ongoing development for experiments

QIE for ATLAS and CMS *(upgrades):*

QIE10: a wide dynamic range, charge integrating, floating point ADC

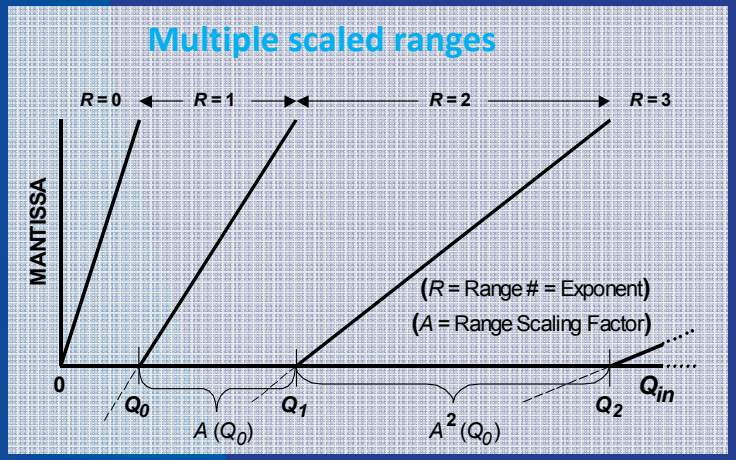
The challenge --

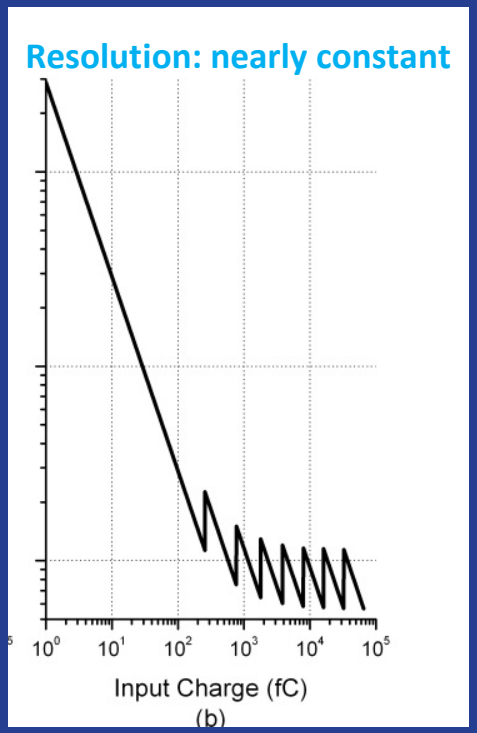
Integrate charge signals over a very wide dynamic range with nearly constant resolution and no dead-time

The QIE concept -- multiple ranges with scaled sensitivity

Pipelined multi-ranging charge integrators feeding a pseudo-log ADC.

Digital exponent (range) and mantissa are output every 25 ns.





Build on the success of the QIE8 currently used by CMS

QIE8: 0 – 30 pC, 2.7 fC/LSB at the low end (13.5-bit dynamic range), resolution = 2%

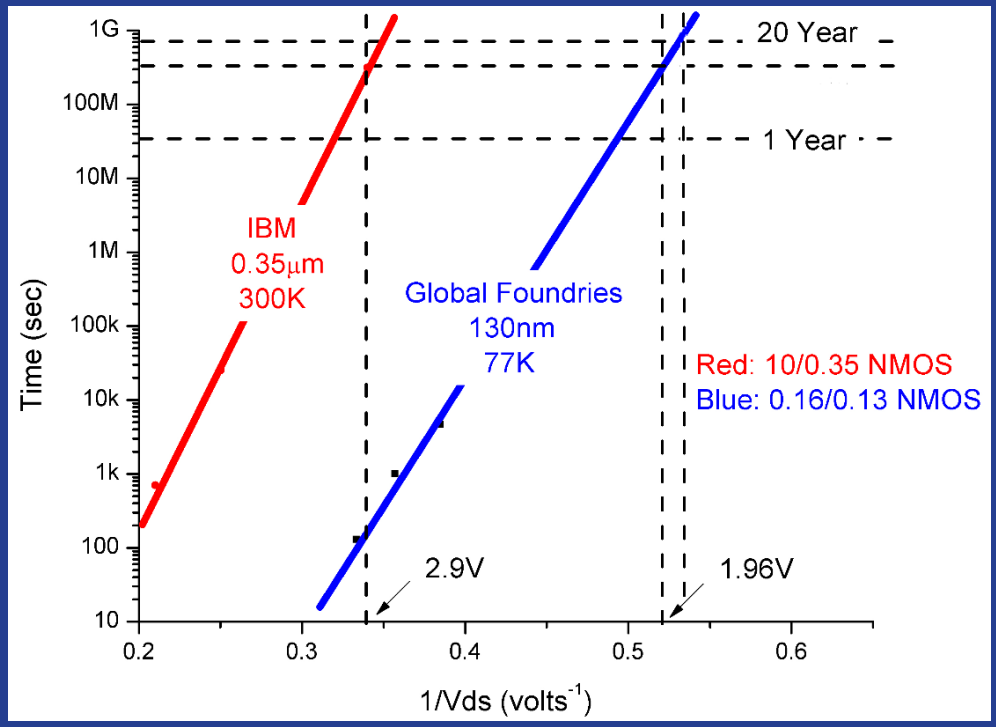
QIE10: 0 – 330 pC (*significantly higher!*), 3 fC/LSB at the low end (~17-bit DR), resolution = 1.4%

submission fall 2010

Ongoing development for experiments

Technology for in liquid Argon operation:

- Fermilab is involved with developing electronics which need to operate at cryogenic temperatures
- Reliability is anticipated challenge, hot carrier effects (HCE) at cryogenic temperatures => decrease of lifetime
- Reliability is derived from limited time measurements under worst stress conditions and extrapolation of lifetime towards full time of the experiment operation
- A method yields operation conditions providing non deteriorated performance
- Preliminary results for the GF/Chartered low power process indicate that no derating whatsoever is necessary at cryogenic temperatures showing that the GF process could be very robust at low temperatures.

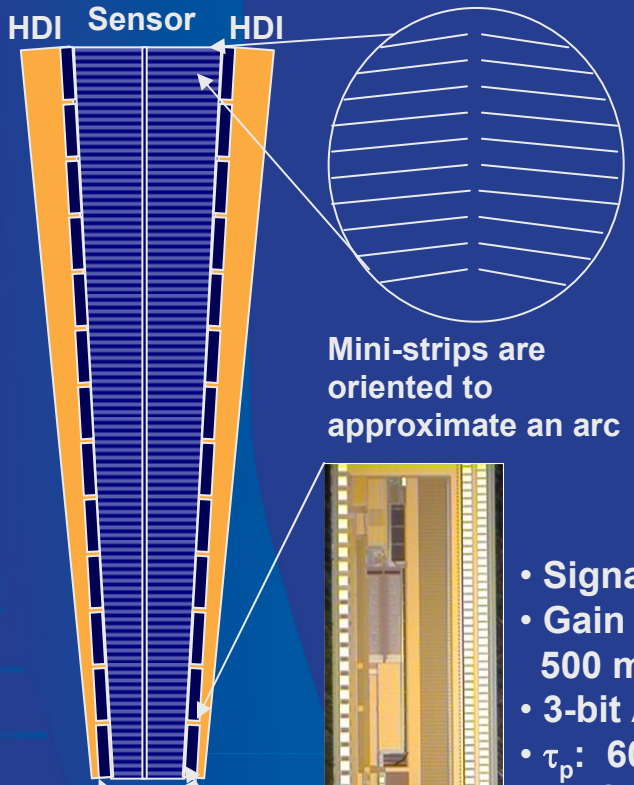


PRELIMINARY

Note:
The IBM process is a 3.3 volt process
The Global process is a 1.5 volt process

Recently completed projects

FPHX for Phenix at RHIC with LANL and BNL (completed 2009)

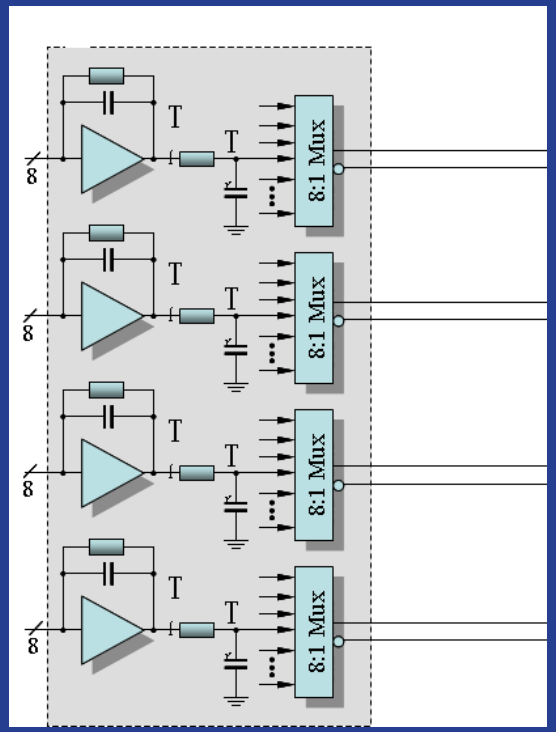


- Signal holes
- Gain at shaper: 500 mV/fC
- 3-bit ADC
- τ_p: 60 ns
- ENC: 150e + 140e/pF
- $Power_{MAX}$: 110 μW/ch
- $Ileak_{MAX}$: 100nA/strip

completed

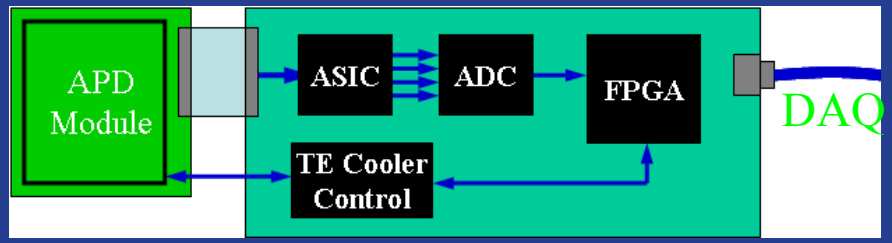
128 channels output data push

Front End Electronics for the NOvA Neutrino Detector (completed 2010)



- 8:1 Muxes run @ 16 MHz to sample each channel at 500
- 2 Msps per channel
- Adjustable risetime & fall-time

completed



Recently completed projects

We know what we do and people working with us are happy

PHENIX @ RHIC

-----Original Message-----
From: Jon Kapustinsky [mailto:jonk@lanl.gov]
Sent: Monday, March 28, 2011 3:01 PM
To: yarema@fnal.gov; zimmerman@fnal.gov; jimhoff@fnal.gov
Subject:

Hi Ray, Tom and Jim,

We are assembling the FVTX detector and I thought you'd like to see a few pictures. These are pictures of the small half-disk, the first station which has 10 chips/wedge. We are assembling the large half-disks now. The large wedges have 26 chips/wedge. The stability of the electronics performance has been remarkable. We test at several different stages of assembly, often without any great attention paid to shielding or grounding, and the noise levels are consistently around 400 electrons, on the bench, on the disk support, and with neighbors powered and clocked. This is the most robust system I have ever worked with. We also have seen almost no failures from the population of chips that passed the probe tests, only a handful of chips have died or had fatal problems, and some of those are probably pilot error. We see occasional hot, or inefficient channels on a small percentage of chips, and that is typically one or two out of 128 channels.

We are happy...

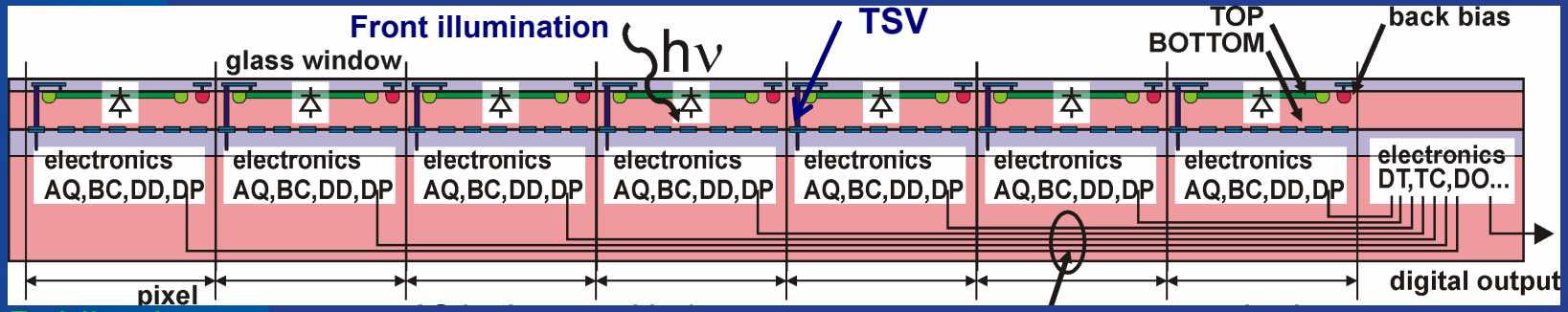
Best regards,
Jon

Jon S Kapustinsky
Deputy Group Leader
P-25 Subatomic Physics
Mailstop - H846
phone: 665-2800
fax: 665-7920

We can provide stable solution for current experiments and convey R&D for future

Conclusions

- Microdetector Electronics <-> ASIC + solid state detectors instrumentation
- People's skills are essential! The ASIC group is cohesive and productive
- Modern test hardware and design software is crucial and needs continuing investment
- Important to maintain healthy balance between R and D
  - provide experiments with readout electronics – and - develop new technologies for future (*often multidisciplinary skills are needed)*
- Difficult with decades between experiments - some projects with shorter timescales
- There are many opportunities – a hard part is matching our stomachs to our eyes. For us 3D is the enabling common thread
- Emphasis is on μdetector resources for HEP, not only for Fermilab - services to other fields of DoE
- Collaborations and serving broad communities
- New Ideas: e.g. Digital 3D Silicon PM



- Publications:
  2-3 articles / yr in peer reviewed journals (IEEE TNS, NIMA, PoS)
  and about 10 presentations / yr at conferences and workshops

Backup

- Content Addressable Memory (CAM) simultaneously compares external patterns to stored templates – very fast track resolving!!!.
- CAMs were used in the CDF SVT
- Similar concept being developed for ATLAS FTK
  - Extending the CAM concept to 3D improves density, speed, and power consumption – FNAL is working on the 3D tracking CAM design