Pixelization in HEP and NS

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Snowmass on the Mississippi

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Overview

- Requirements and technology
- R&D possibilities and physics impact for the future
  - High Rate
  - Low Mass
  - Low power
- Thoughts toward the establishment of cross-frontier R&D programs in areas of common need for the field (scattered in slides)
- Conclusion

~2020 Experiment Requirements

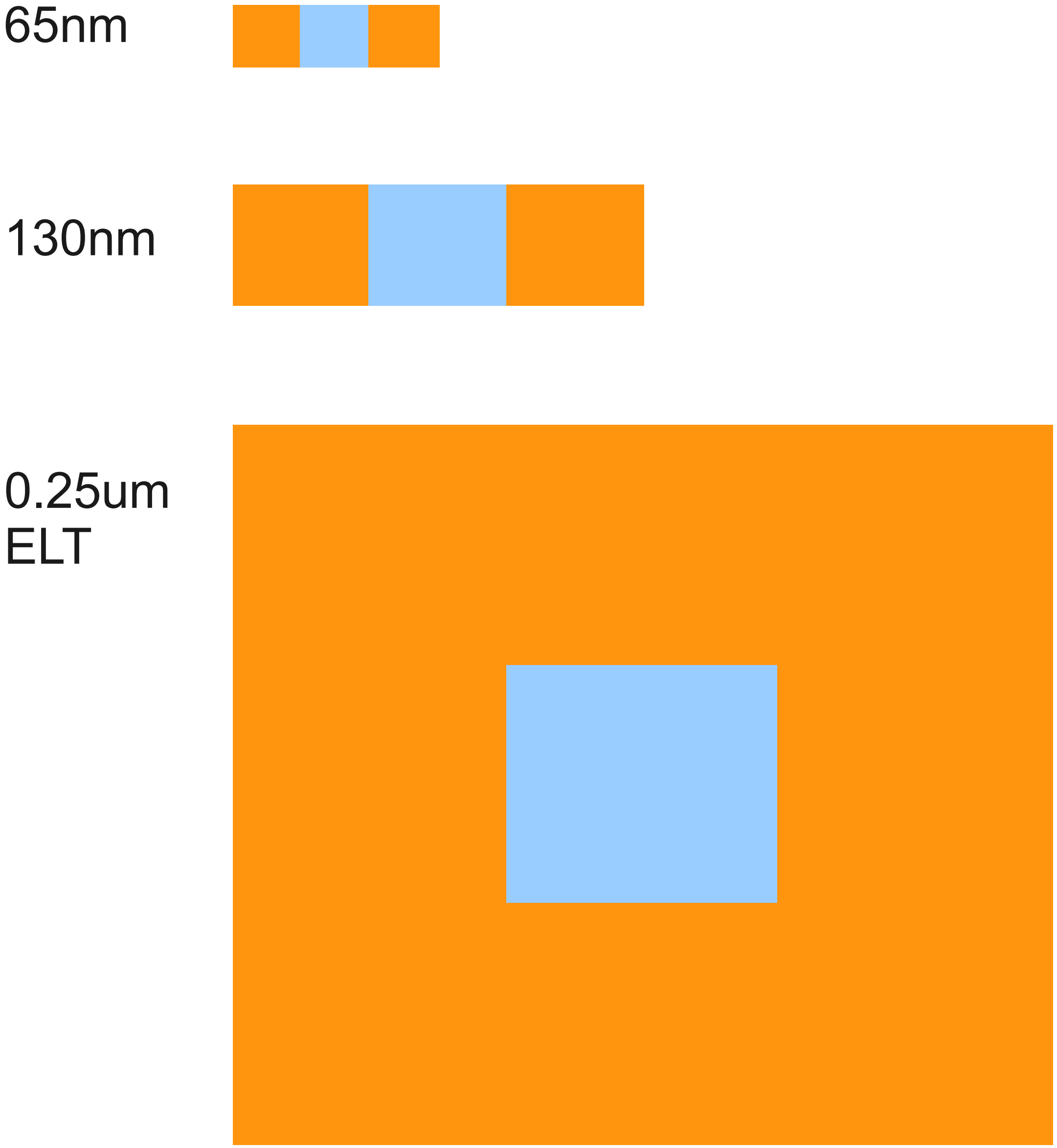
	Hit rate MHz / cm^2	Typical event hits / cm^2	Radiation Mrad	Pixel size um^2	Time resolution ns	Detector length cm	Mass per layer %X0
HEP p-p	1000.0	10	1000	5000	25	200	<2.0
NS heavy ions	2.0	100	1	500	100	30	0.2
B-physics p-p	400.0	10	400	3000	25	50	<1.0
B-physics e+e-	40.0	5	10	2500	100	30	0.2
HEP ILC	0.1	5	1	250	150	30	0.1
HEP mu+mu-	20.0	5	500	5000	1	30	<2.0

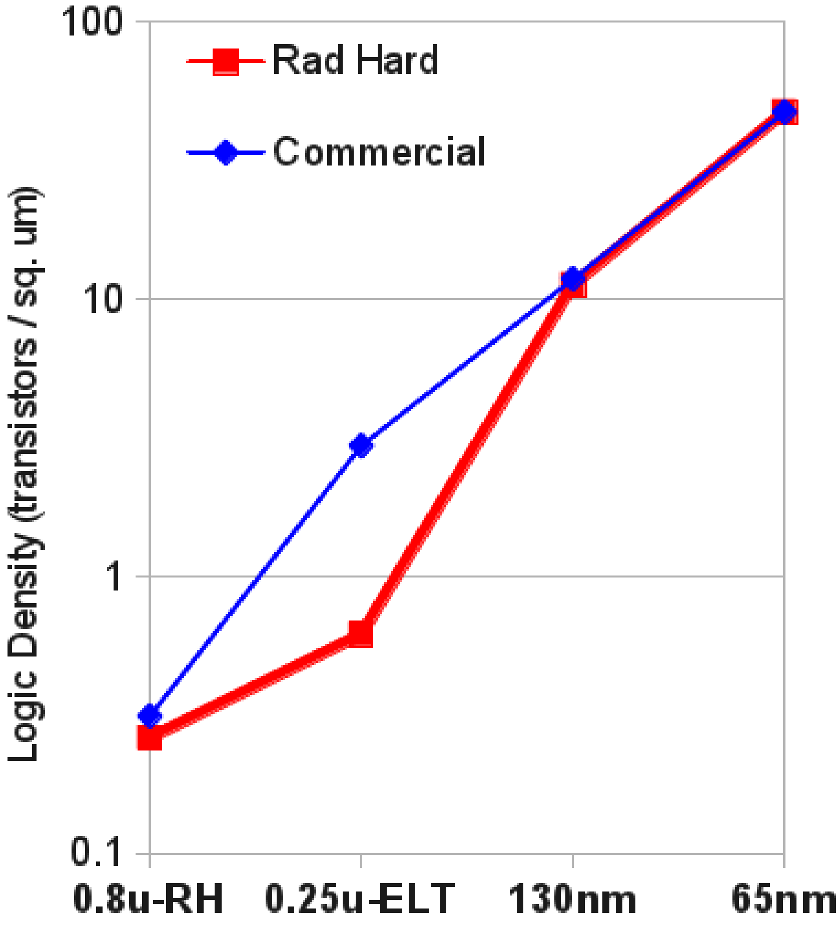
High Rate

- Requires readout of every pixel in parallel
  - Needs high logic density
- Fast timing goes hand-in-hand with high rate, requires fast signal collection in each pixel
- High rate is also associated with high radiation (because the particles being detected ARE the radiation)
  - Radiation tolerance also requires fast signal collection, among other things

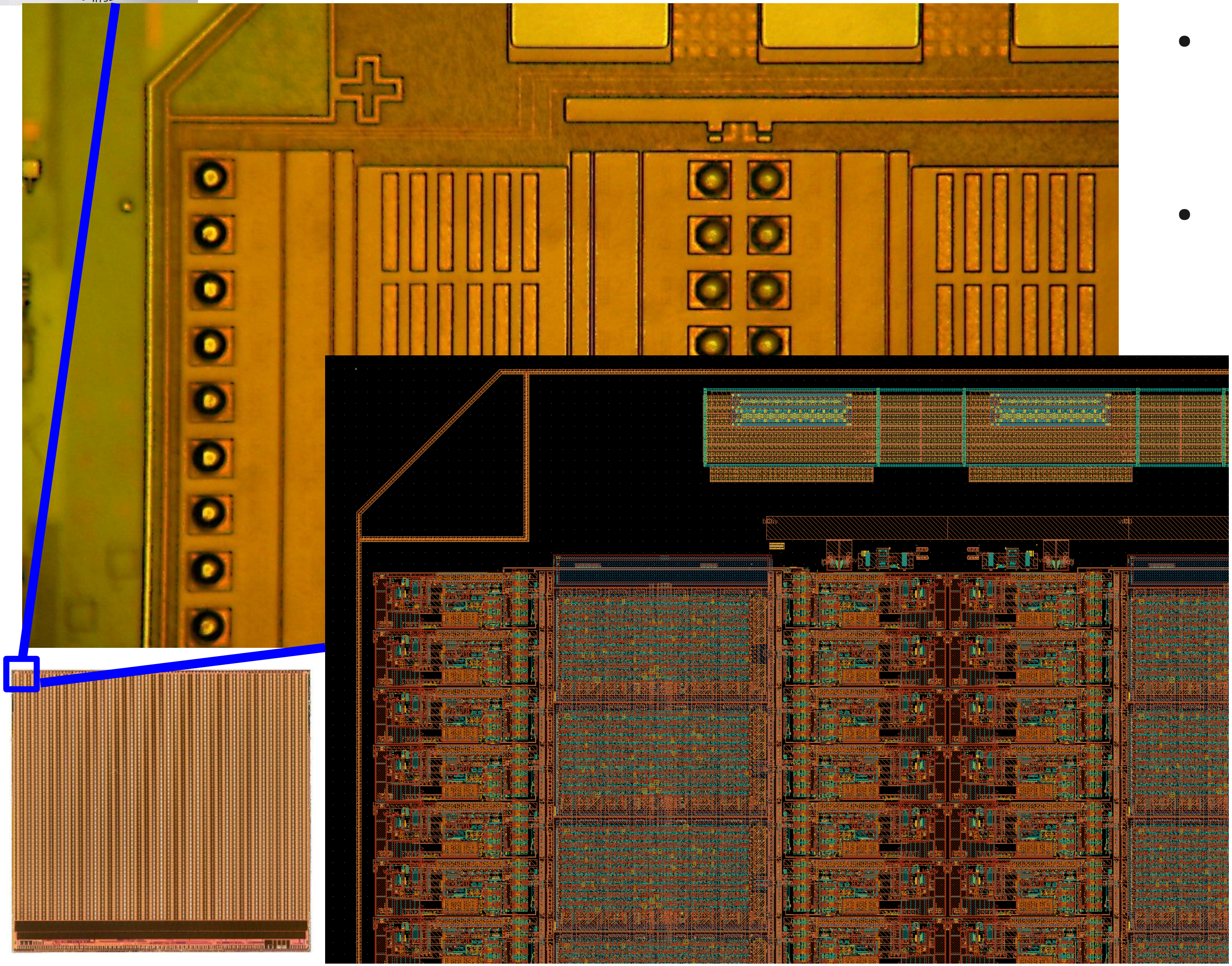
- Hybrid pixels are the proven solution to all of the above
  - But work is needed to meet the ~2020 requirements
- Why would we ever consider anything else?
  - Cost
  - New requirements

Rad Hard logic lagged Moore's Law due to ELT, but now caught up





FE-I4 Digital Column

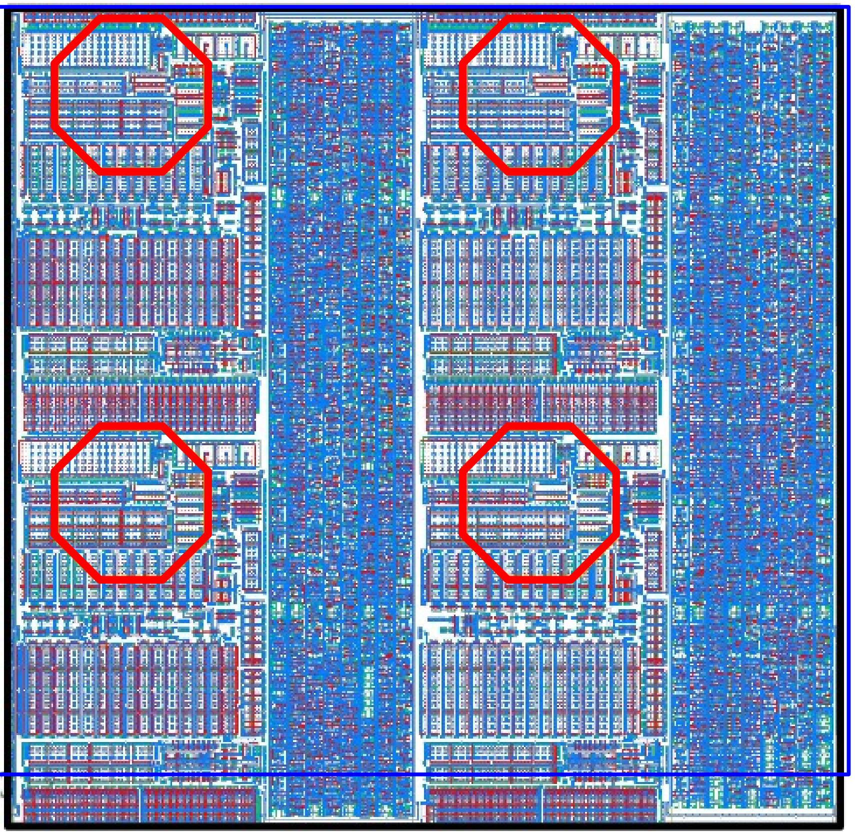


- **Column composed of 4-pixel digital regions**
- **Each region logic is one synthesized block (10K gates)**

Medipix 3RX 4-pixel group

FE-I4 region outline (half-width)

- **Similar concept where 4 pixels form a functional core**
- **Configurable allocation of 4 pixels:**
  - **Fine pitch: count 4 independent charges with 2 thresholds**
  - **Spectroscopy: count only the sum of 4 charges with 8 thresholds**
- **Analog communication between 4 pixels for charge summing, digital for allocation**



High Rate work needed

- Go from today's ~200 MHz/cm^2 to 1 GHz/cm^2
- Reduce pixel area a factor of ~4
  - Coincidentally same area factor going from 130nm to 65nm CMOS
  - Note this will reach, BUT NOT EXCEED, the density limit for proven bump-bonding technology
- Increase radiation tolerance to 1 Grad level (1E16 neq./cm^2)

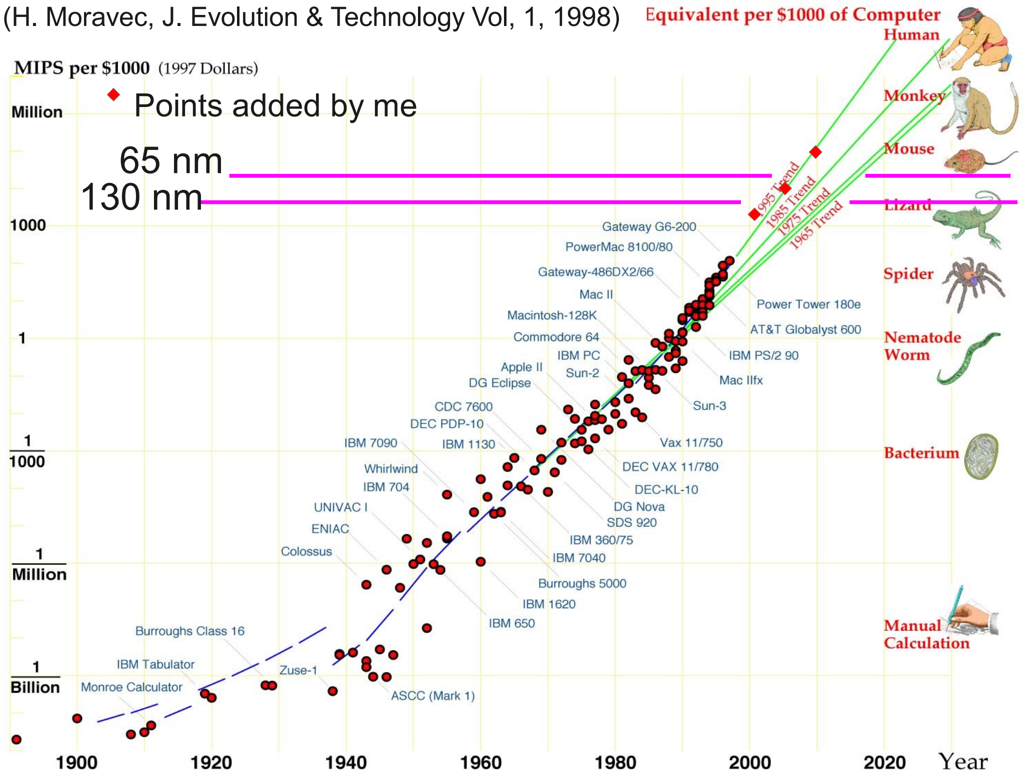
- Readout chip development now organized in RD53 collaboration- joint ATLAS-CMS
  - High rate pixels drive need for complex digital design
  - Opens up possible use for other applications that could not afford it on their own
- Very active sensor program dominated by Europe and Japan in both 3D and planar silicon

Challenges and opportunities of deep submicron CMOS digital desgin

From
G. Deptuch
HEPIC2013

45nm Intel Nehalem processor design team

(H. Moravec, J. Evolution & Technology Vol, 1, 1998)



New Requirements for High Rate applications

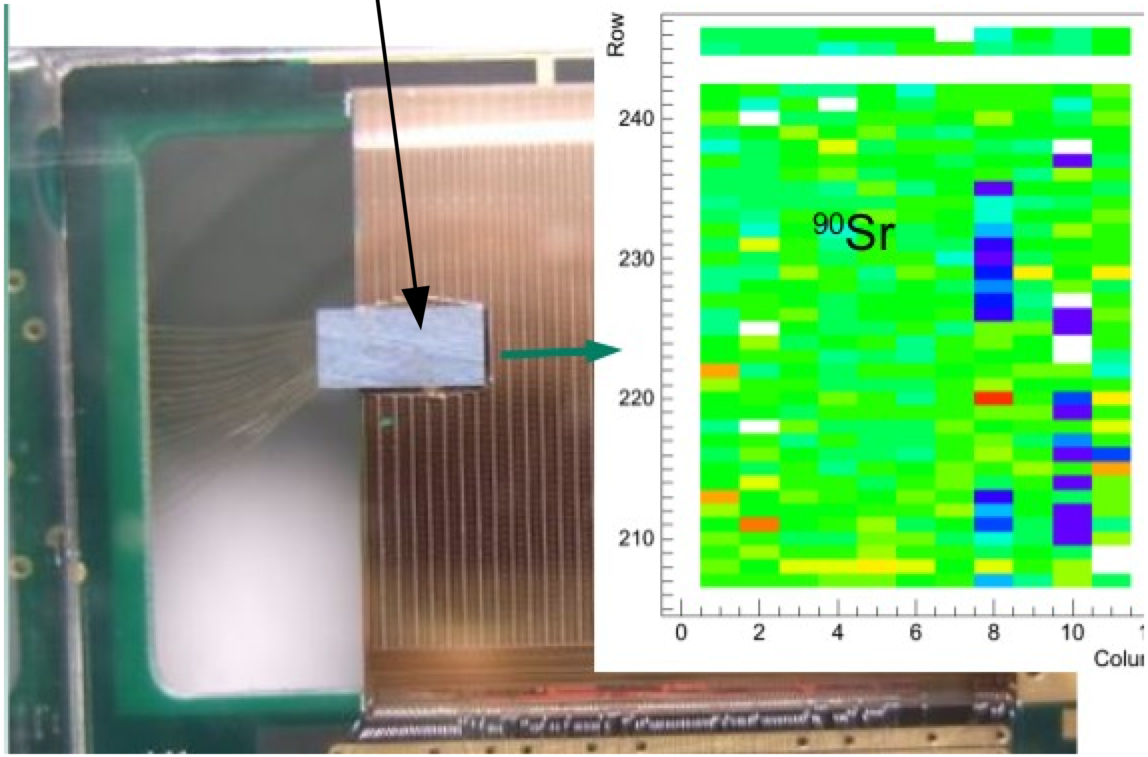
- Better 2-track separation for efficient tracking in boosted jets
  - This needs thinner sensors and also small pixels. But thinner sensors is critical
  - For diode sensors the challenge is to reduce capacitance along with thickness. Otherwise S/N degrades.
    - For bump bonded hybrid pixels interconnect capacitance cannot be reduced, making the challenge greater
- Track trigger capabilities
  - For pixels at small radius this simply means greater output bandwidth.
  - Few Gb/s per chip for ATLAS/CMS inner layer likely.
  - Commonality with triggerless LHC-b in terms of data output
  - Getting to within 1 order of magnitude of ATLAS/CMS triggerless
    - Too little to to consider this anything but pie in the sky?

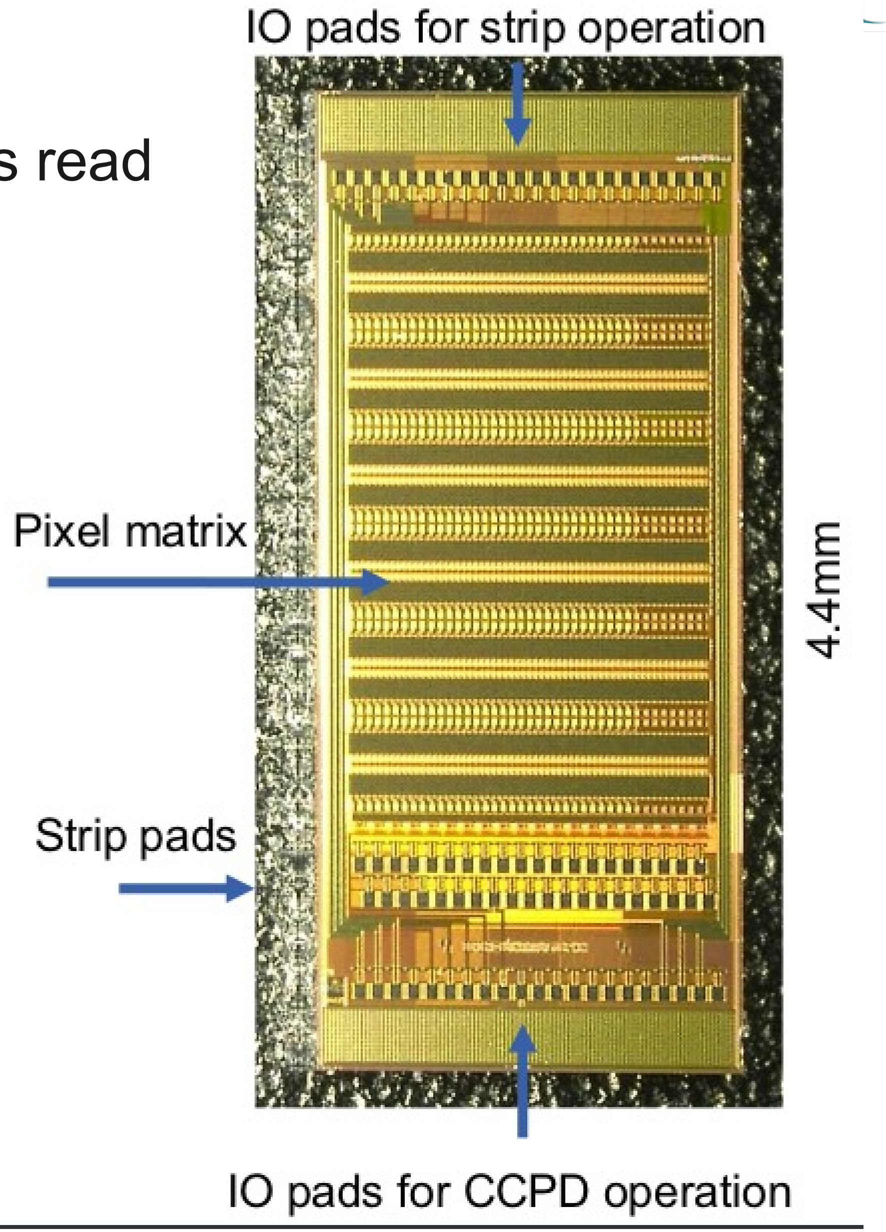
CMOS sensor option for ATLAS/CMS

- CMOS sensors have big advantage when it comes to the thin sensitive area & small pixels needed for tracking in boosted jets.
- But 2 tiny problems:
  - Typical MAPS do NOT read all pixels in parallel
  - Not rad hard to few Mrad, let alone 1 Grad
- Tow approaches so far develop ATLAS/CMS active pixels
  - Hybrid MAPS
    - Keep the pixel readout chips, replace sensor and bumps
    - Use an isolate well, HV-CMOS process to make it rad hard
    - Concept also works for replacing strip sensors where the cost reduction could be large.
  - MAPS in deep submicron CMOS with substrate isolation
    - Implement sensing in process used for FE-I4 and Medipix-3
- Significant opportunity as developments are recent, and commonality with MAPS for NS and e+e-

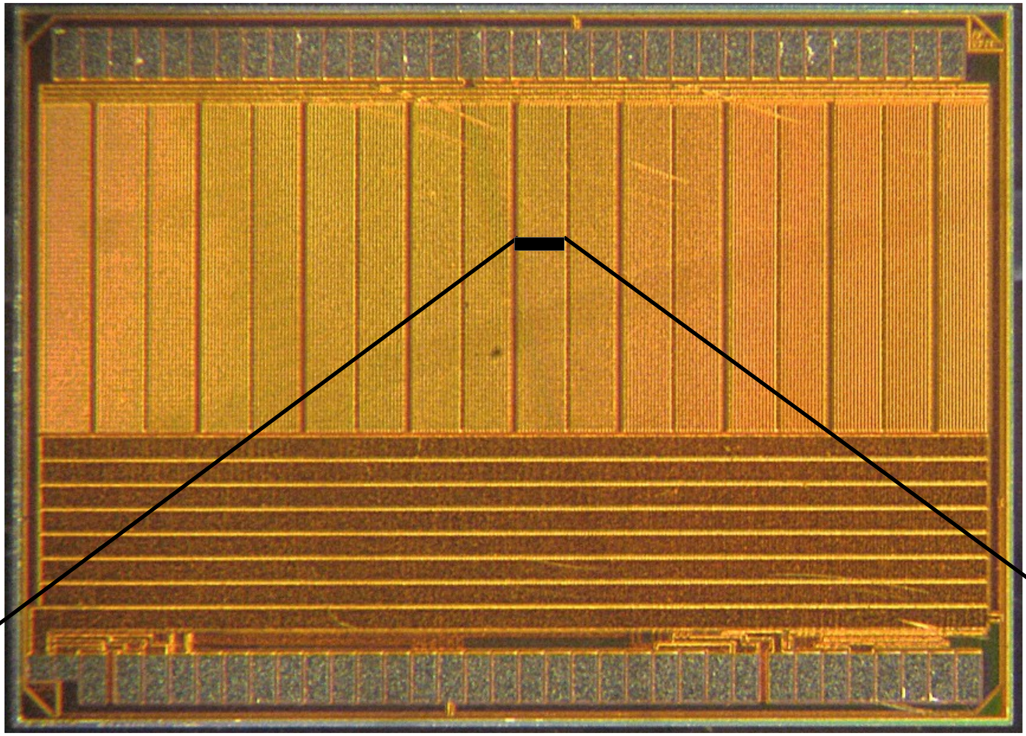
Hybrid MAPS

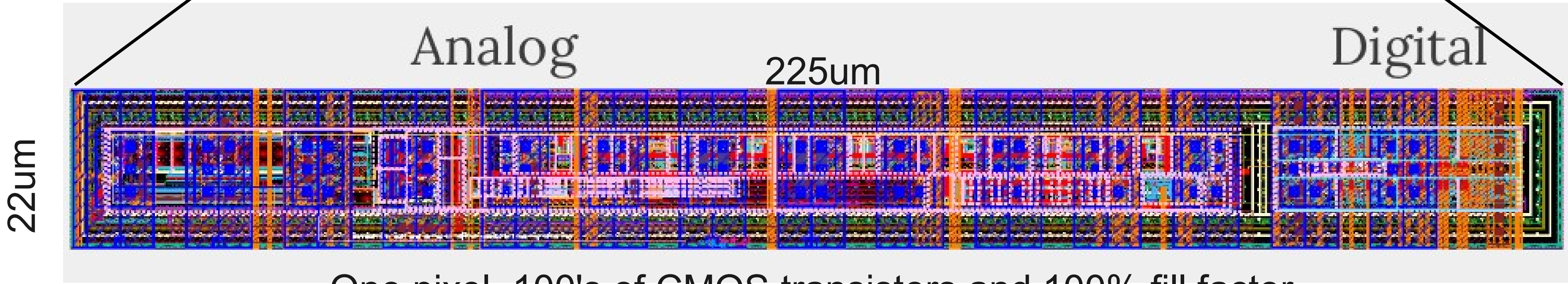
CMOS sensor glued onto FE-I4 chip. Signals read Capacitively. No bump bonding needed.





MAPS on 130mn CMOS





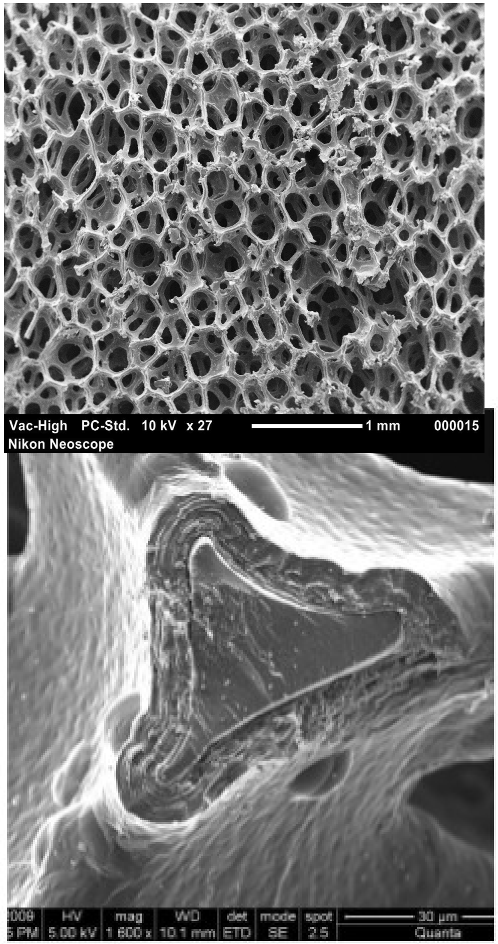
One pixel. 100's of CMOS transistors and 100% fill factor

Low Mass

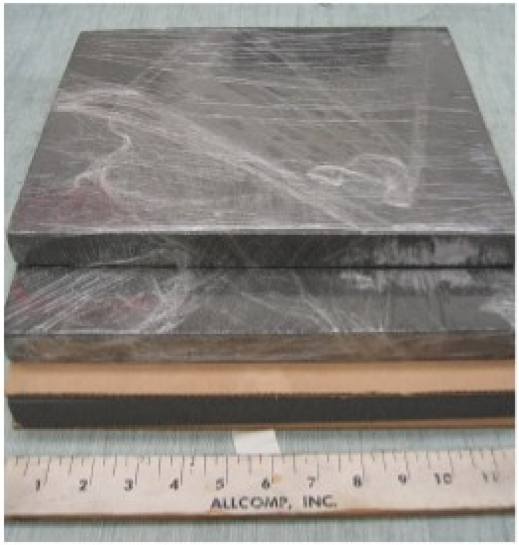
- High rate and long detectors are the enemies of low mass
  - High rate requires significant power and therefore some mass to manage the heat
  - Long detectors cannot be air cooled, and need some mass for structural stability.
- Significant commonality between heavy ions and ILC:
  - Need low mass, short detectors, low hit rate
- But achieving the lowest mass allowed by rate and size constraints is common to all, and this requires one thing
  - Better composite materials
- US has a leading role in this area. Opportunity to keep and expand

Example of new carbon foam

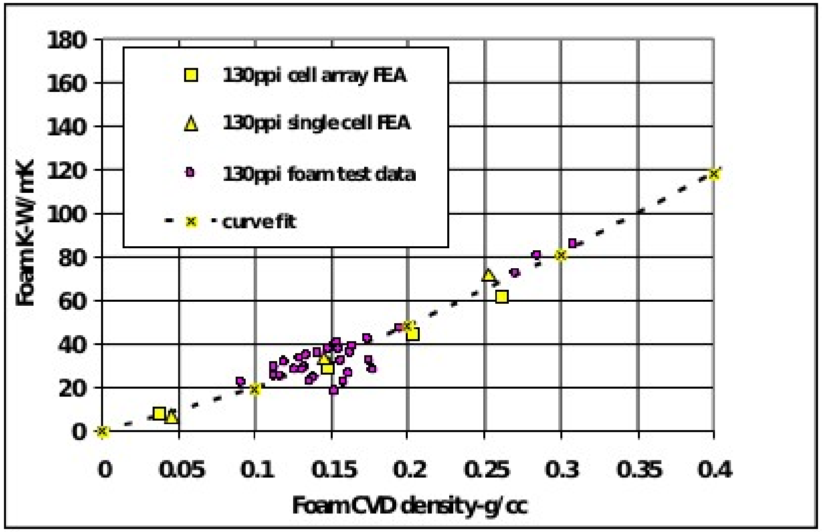
Development by Allcomp, Inc. with SBIR support



Micrograph showing
open cell structure
After treatment



Produced in blocks



Thermal conductivity vs. density

Low Power

- Absolutely critical for the lowest mass applications
- But techniques for power reduction are also of common interest
- Pulsed power proposed for ILC requires further development
  - Opportunity in combination with air cooling

New technologies

- Ron showed a number of new concepts being pursued
- I only talked about established technologies
- Is high risk R&D into new technologies needed?
  - Of course. Should always have some “free energy” to explore new concepts
- But regarding common initiatives
  - Can't predict which seeds will grow
  - Only makes sense to organize “large” R&D efforts around something that already has some roots.

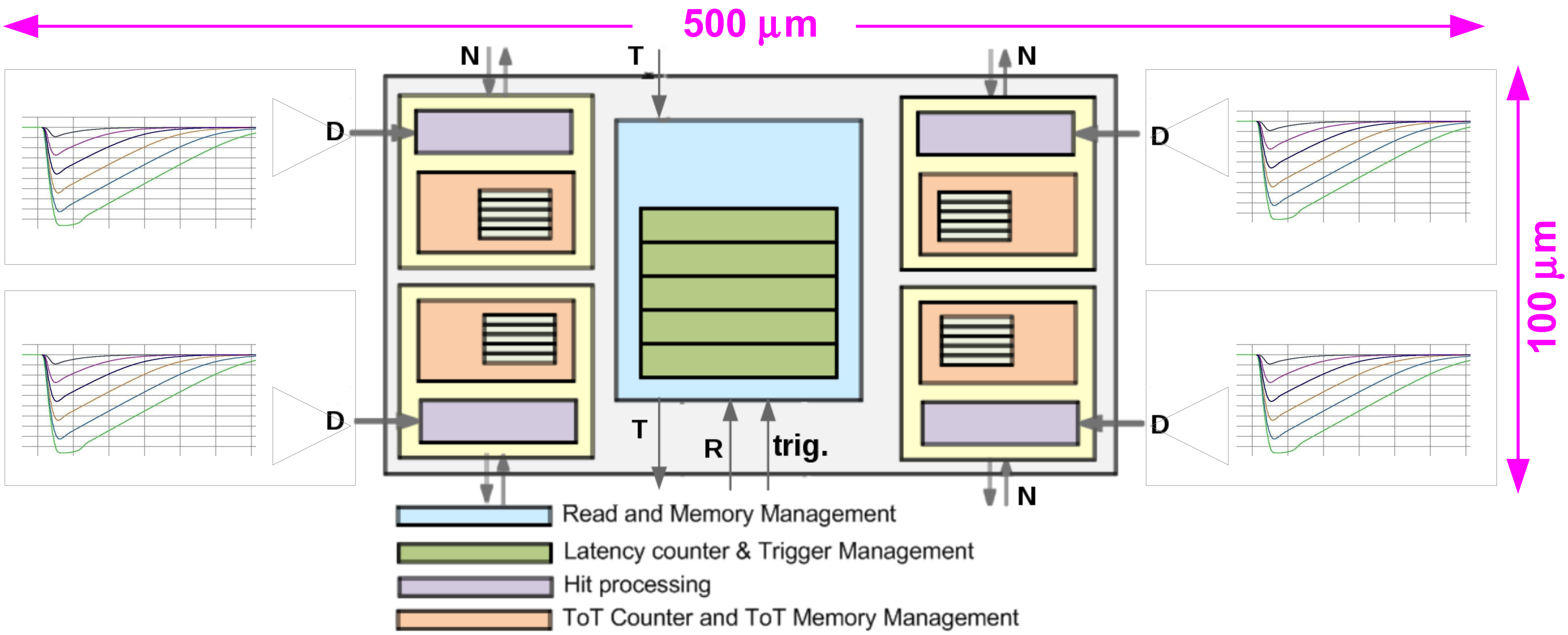
Conclusion

- Significant variation in pixel requirements for future experiments
- Nevertheless there is much commonality
- CMOS sensor development driven by different requirements is pursued by all
  - Relatively new for ATLAS/CMS
  - Significant opportunity
- Better composite materials needed by all to achieve the lowest mass consistent with rate and detector size
  - US leading role in this area presents significant opportunity
- Basic R&D into new concepts should always continue at some level

B A C K U P

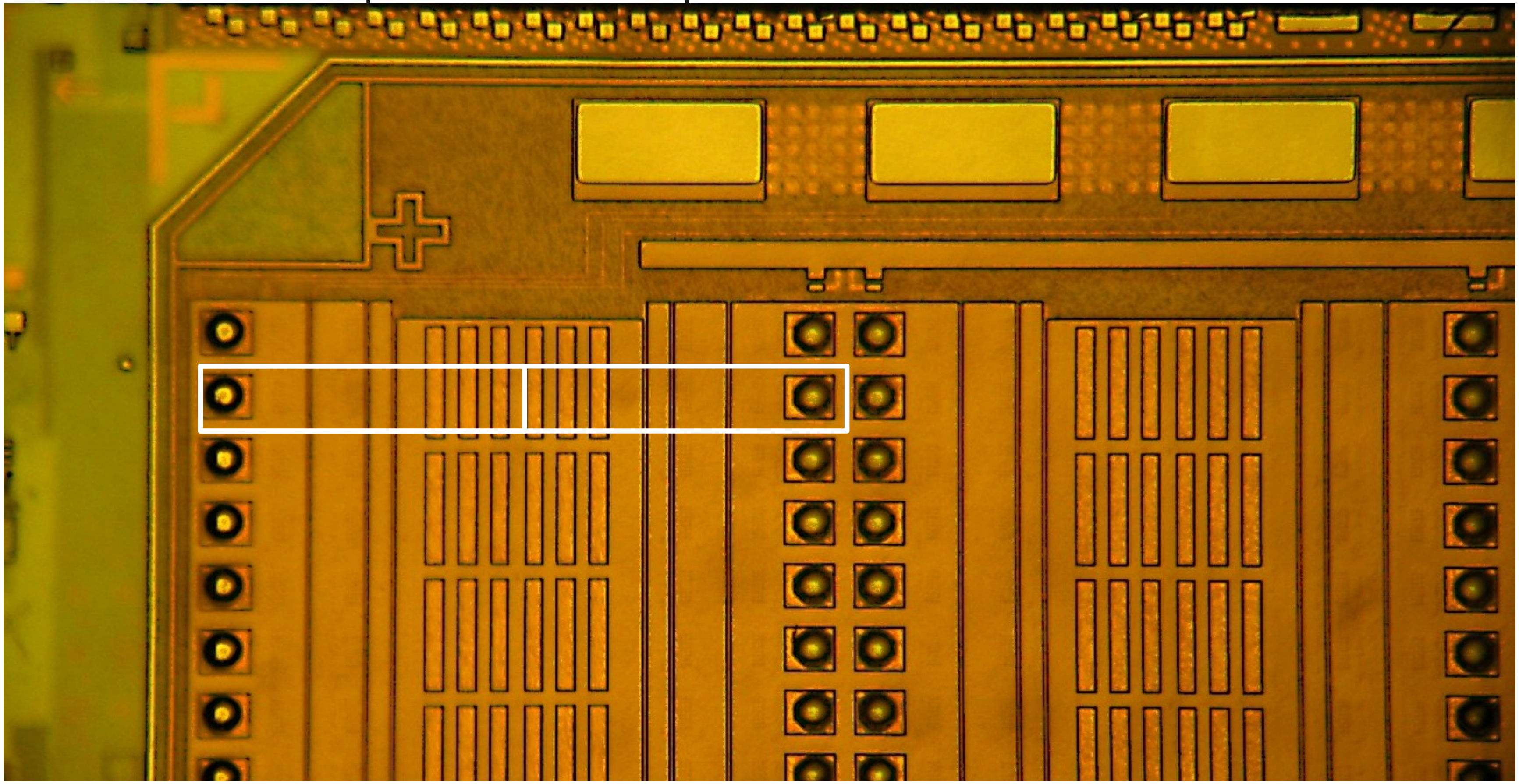
FE-I4 Digital Region

- **Digital block is shared with 4 inputs- each form an identical analog pixel.**
- **A simple digital processing "core"**



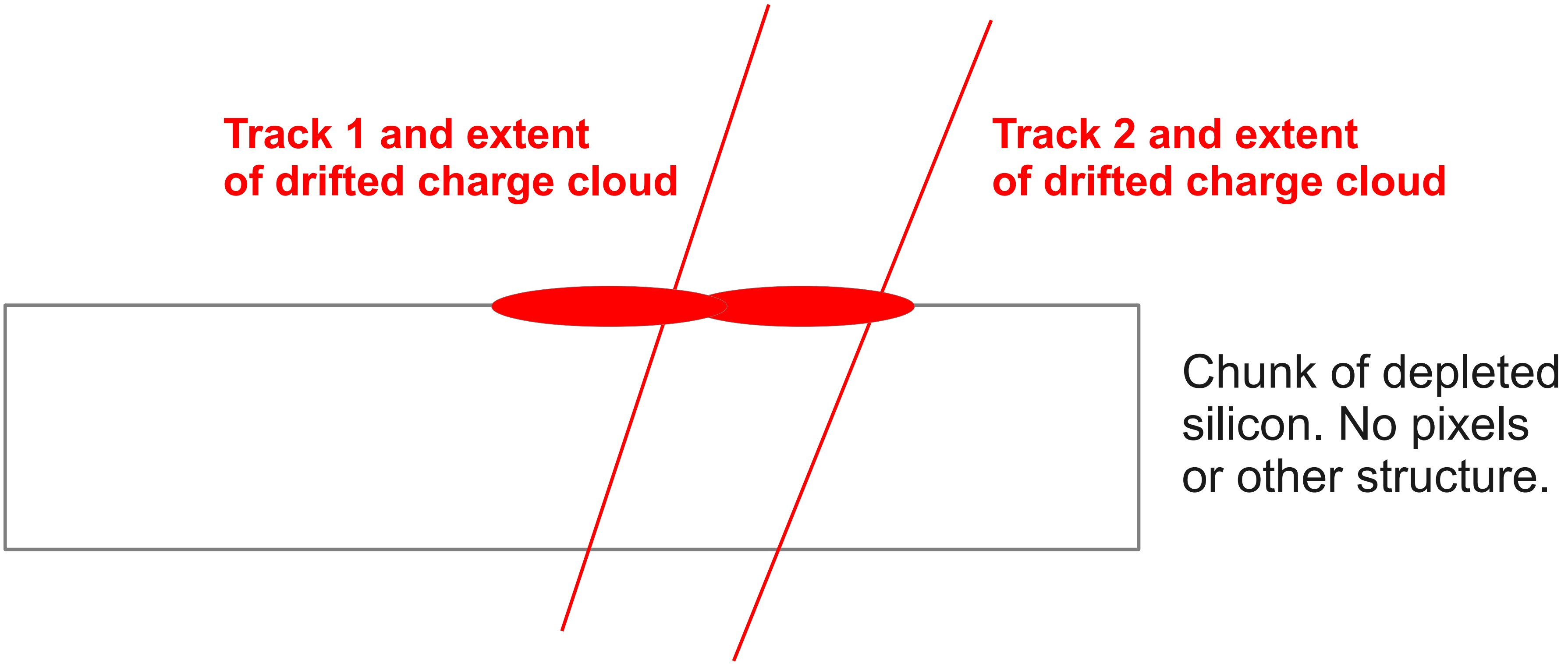
Bump bonding

Corner of FE-I4 chip with solder bumps



- **There is plenty of room to increase the number of bumps per unit area.**
- **Technology density = 400 bumps / mm^2**
- **FE-I4 used density = 80 bumps / mm^2**

Thinner silicon



Makes no difference how small one makes the pixels in this planar example. The charge clouds are merged- oversampling them will not separate them.