Feedback System Hardware/Software Progress and Future Plans

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Outline for Talk

- Updates on current work and next steps
  - Current hardware for SPS Feedback Demonstrator System
    - Features of the current system
    - Verification of system and noise measurements
  - Future hardware upgrades
    - Wider bandwidth kickers
    - Additional synchronization flexibility including feedback during energy ramp
    - Additional functionality to Feedback Demonstrator System
    - Upgrades to software (operation, user interface, analysis and feedback design)

System Diagram

- 4 GS/sec Feedback Control System with picosecond alignment

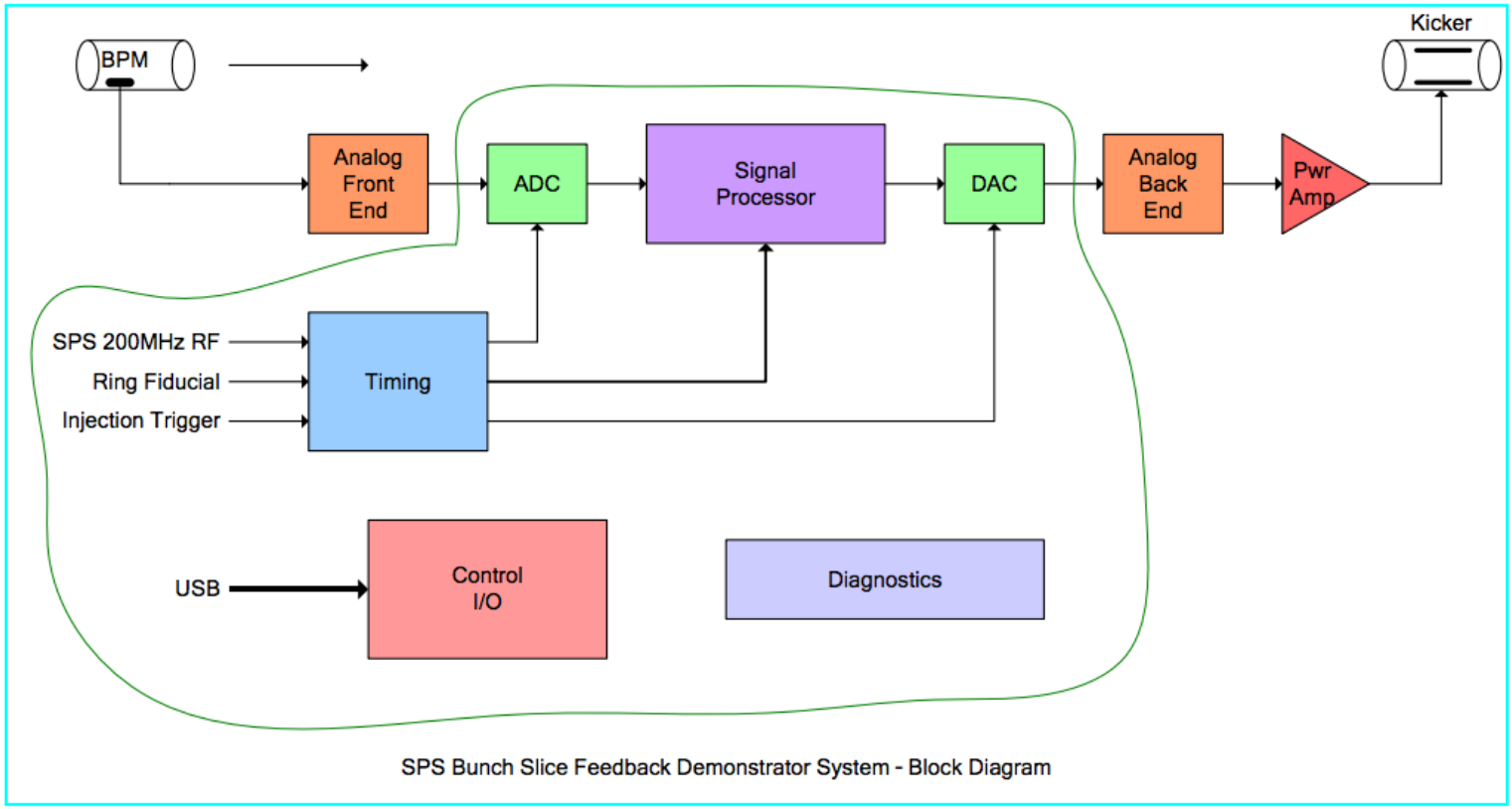
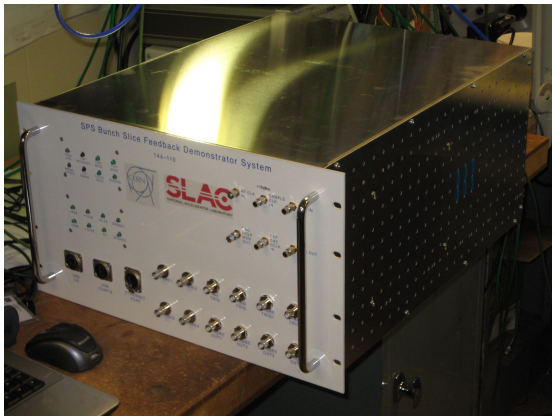
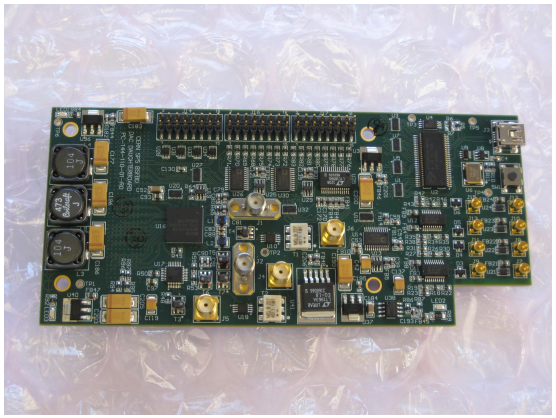


Figure 2: Block Diagram

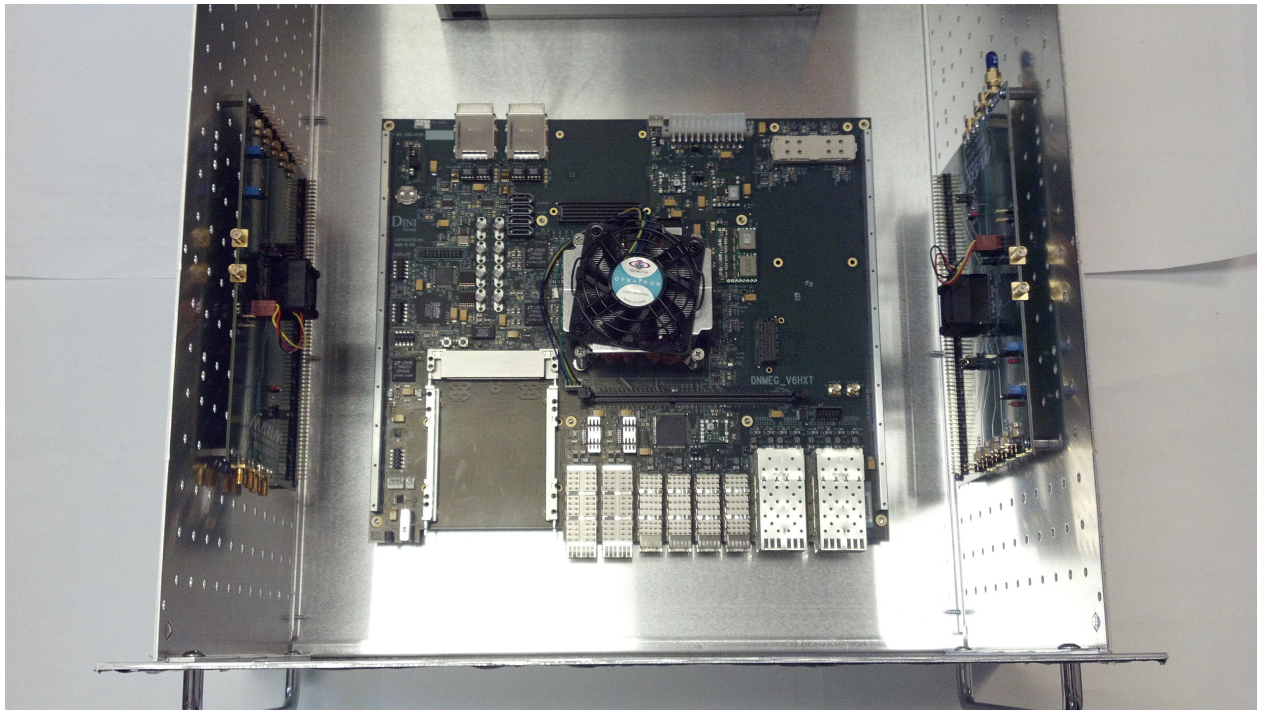
SPS Feedback Demonstrator System Pictures



Front Panel of System chassis.



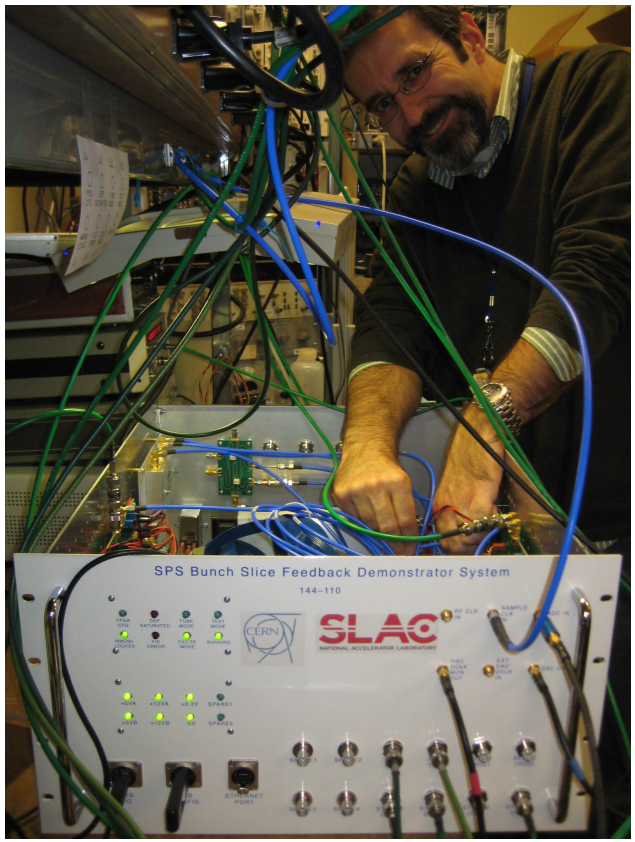
DAC daughterboard card.



Inside SPS Feedback System chassis without cables. FPGA and two ADCs are shown here.

SPS Feedback Demonstrator System Characterization

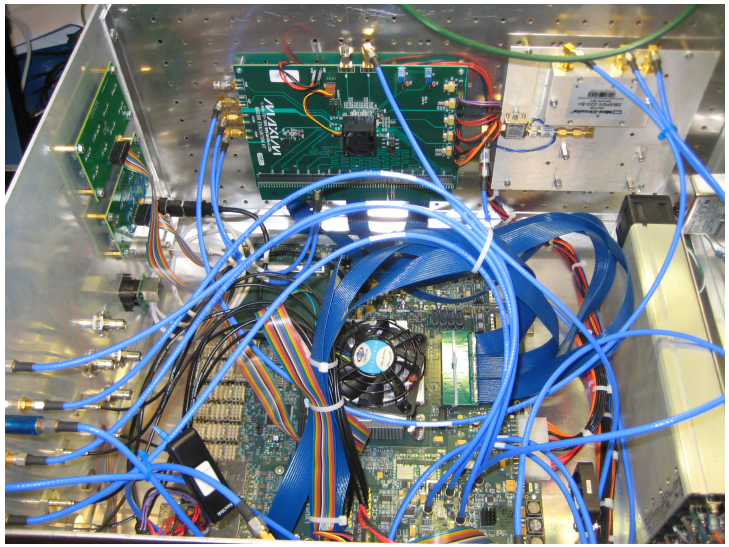
- System tested with SPS beam in Nov 2012 and Jan/Feb 2013
- Features:
  - Flexibility in configuration
  - Synchronized A/D and D/A sample bunch and output to kicker
  - 4 GS/sec. sampling rate (3.2 in current tests)
  - Able to control 1 bunch, with FPGA reconfigurable to expand to control of additional bunches
  - Snapshot memory captures bunch motion for up to 32k turns



J. Dusatko testing at SLAC.

SPS Feedback Demonstrator System Characterization

- Features continued:
  - 'Slices' controlled by 16 FIR filters, each with up to 16 taps
  - Can switch between 2 sets of filters in real-time
  - Initial control and measurement software written and tested
  - Can be synchronized with excitation system
  - Note: these studies use 200MHz stripline pickup as a kicker. Designing wideband kicker for further studies.



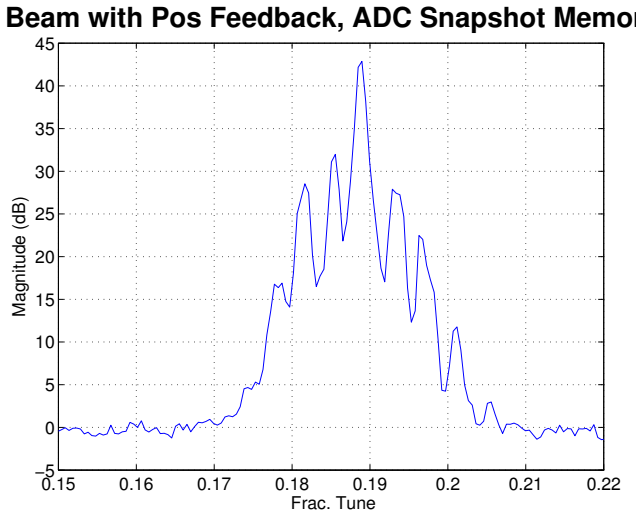
Inside SPS Feedback System chassis.

Current Hardware Updates Outline

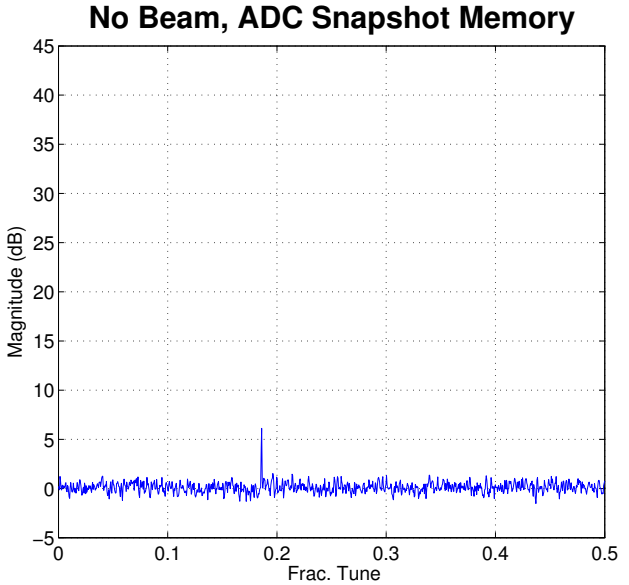
- Current hardware for SPS Feedback Demonstrator System
  - Tested and verified feedback system
    - Tested various filter configurations and ran feedback experimentation successfully
    - Nonlinear (two-tone) intermodulations tests run
    - Noise floor and dynamic range characterization
    - Developed methods of synchronizing system with the beam
  - Verification of equalizers
    - Frontend hardware equalizer
    - Backend equalizers for cabling and kicker

Hardware Verification Results: Noise Floor

- ADC dynamic range is as expected > 58 dB S/N.
- Noise without beam is low and flat across all frequencies.
- DC offset of beam means we currently use half the dynamic range for ADC input. Plans to remove DC offset in future.

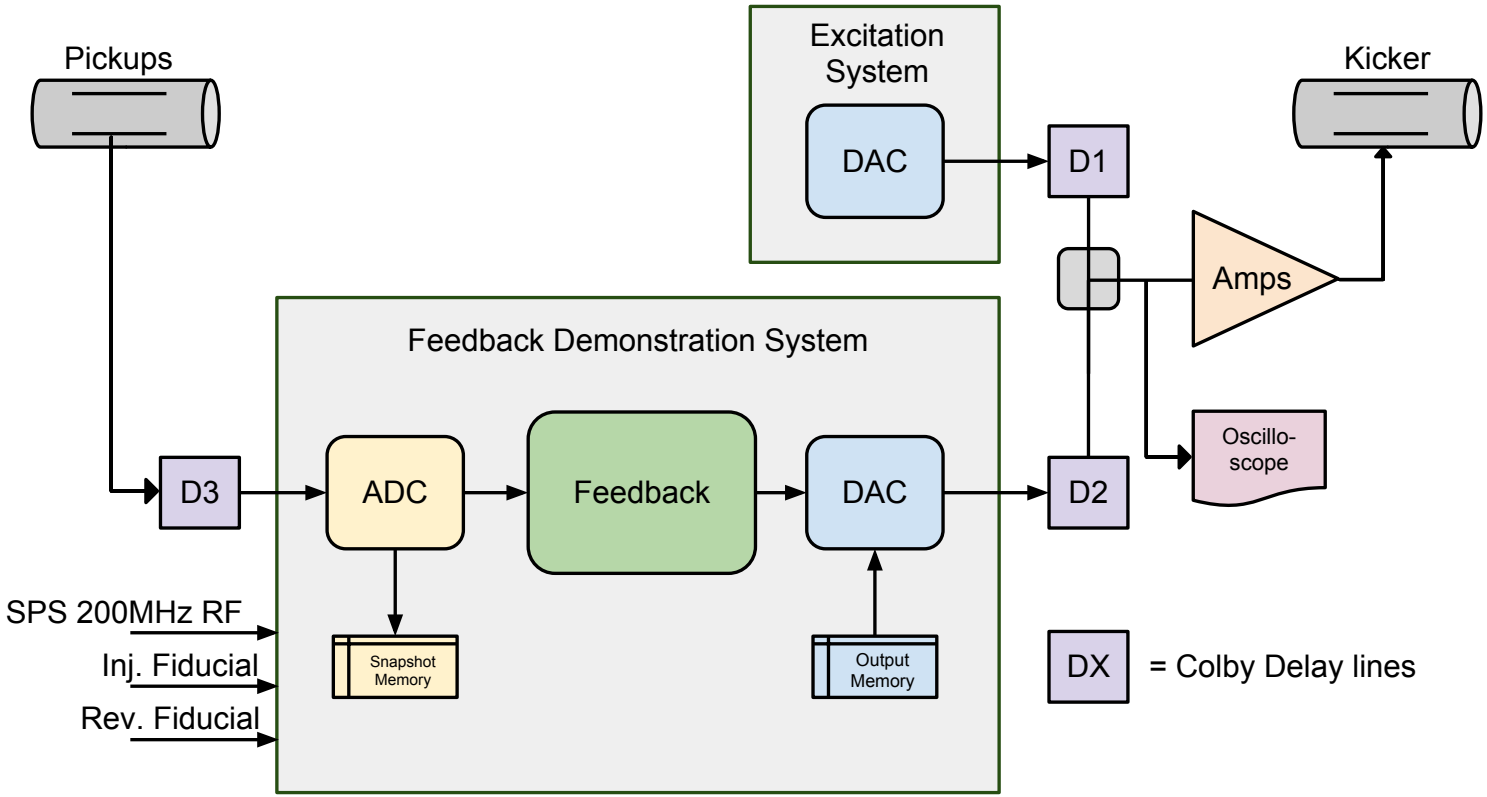


Averaged over 4k-12k turns, an example of large signal with many modes.



Averaged over same turns, signal without beam shows low noise.

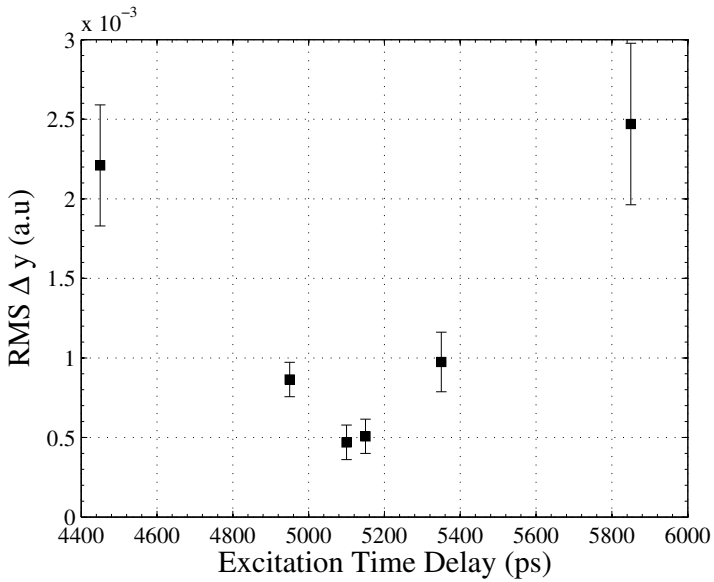
Timing Block Diagram



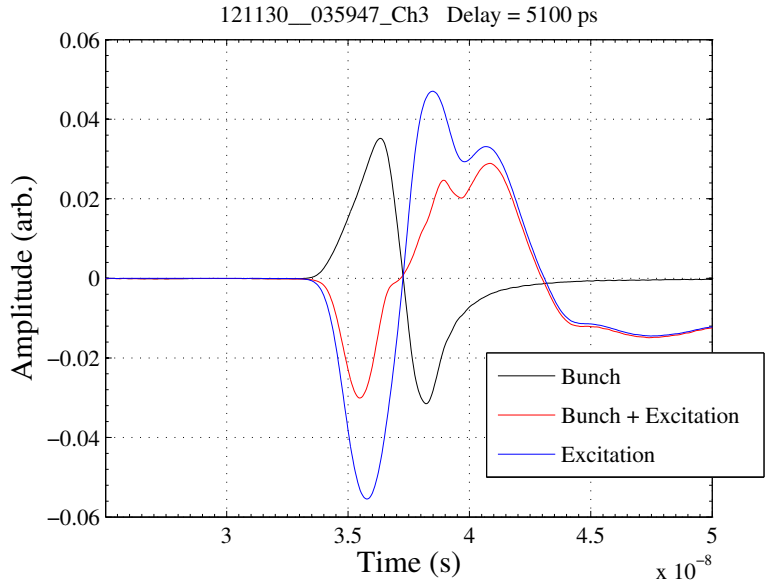
Simplified block diagram of the system for demonstrating timing procedure.

System Synchronization with Beam

- Backend timing alignment methods developed and refined



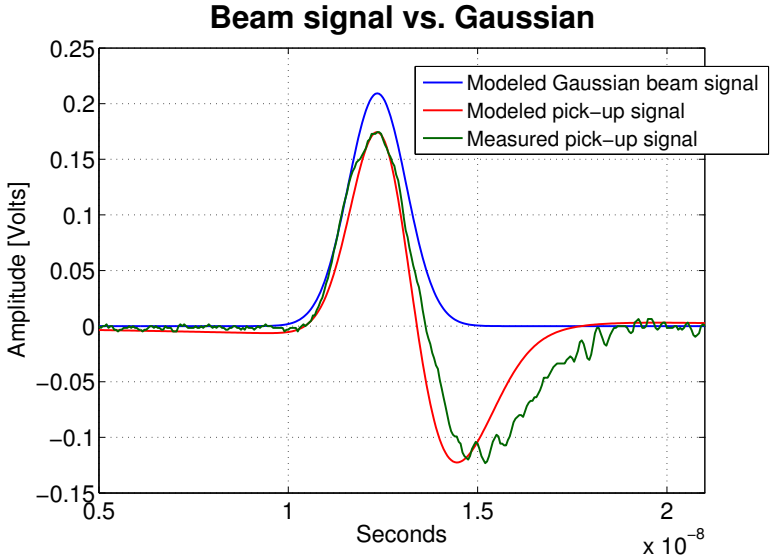
Method 1, pickup: excite with mode 1 and find minimum RMS motion at betatron tune. This method is very time consuming.



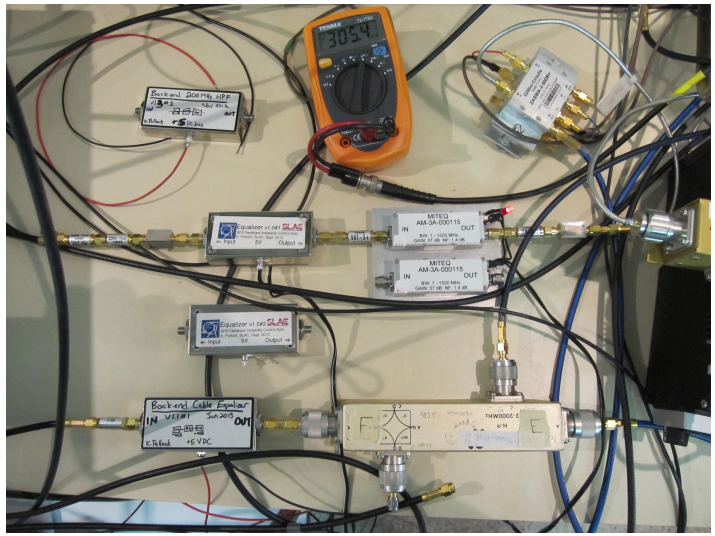
Method 2, kicker load: excite with mode 1 without amplitude modulation and adjust delay until inflection point coincides. A faster more practical method.

Hardware Equalizers

- The cabling and pick-up (and kicker) exhibit non-linear phase response.
- Hardware equalizers needed for fast response.
- Design method developed that includes parasitic components in optimization
- Front-end and back-end equalizers constructed and tested.



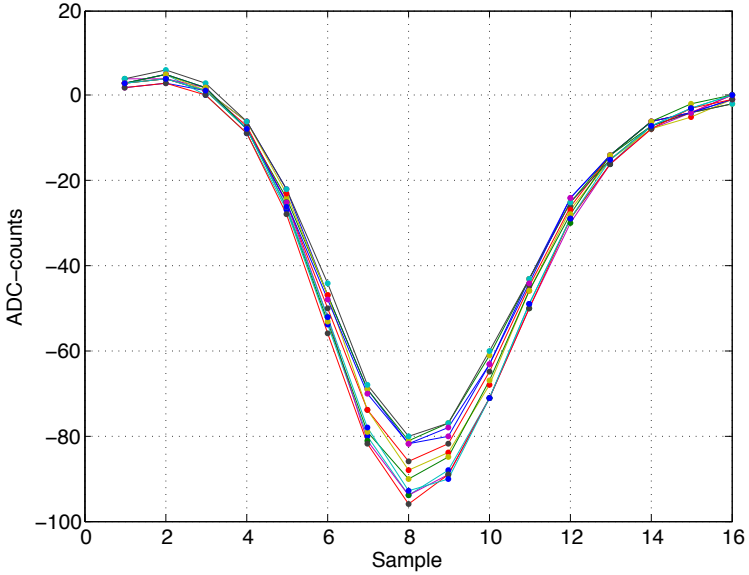
Signal with and without equalization.



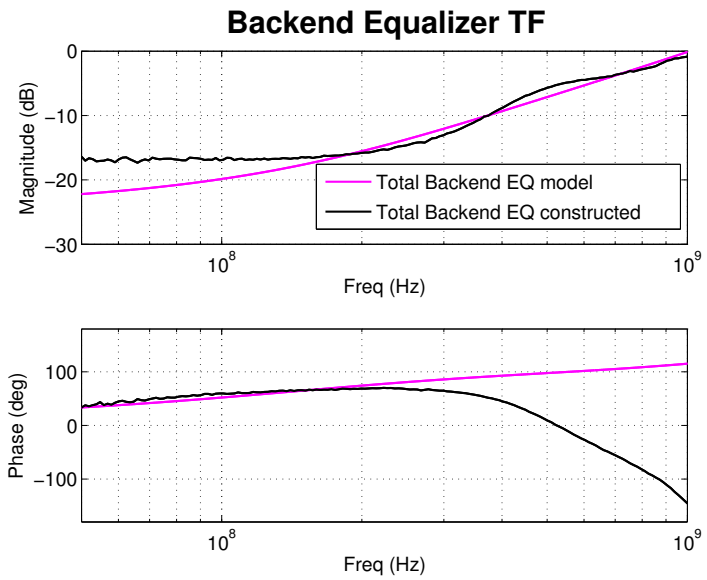
Equalizers shown here at CERN.

Hardware Equalizer Verified

- ADC snapshot with hardware front-end equalizer shows expected shape for bunch
- Cable equalizer for backend verified
- Kicker equalizer needs higher gain amplifiers, an we will re-evaluate need for backend equalizer with new kicker and amplifiers.



The bunch shape as measured by the ADC shows approx. Gaussian shape.



Transfer function for modeled and constructed backend equalizer.

Next Steps for Hardware Improvements

- Higher bandwidth kickers being designed by J. Cesaratto, the team at Frascati and the team at LBL
  - This is essential to demonstrate control of higher order instabilities as current stripline kickers only have 200MHz bandwidth.
  - Higher power amplifier testing in preparation for new kickers
- Greater flexibility of timing with energy ramping capability
- Additional improvements to demonstrator feedback control system

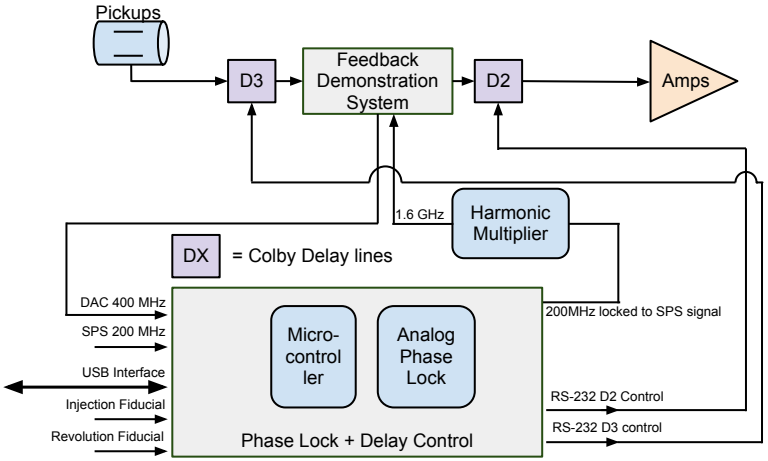
Testing New Amplifiers

- Testing various amplifiers in preparation for new kickers (S. Johnston)
- Specifications:
  - 100-200 Watts
  - 40MHz-1GHz bandwidth
  - Testing performance for higher order mode control.

S. Johnston testing amplifier power supply.

Phase Lock with Delay Line Control

- Building a general purpose phase lock that will tracking with energy ramp
- Additionally adding control of Colby delay for added flexibility and potential for automated timing



Block diagram of phase lock system components.

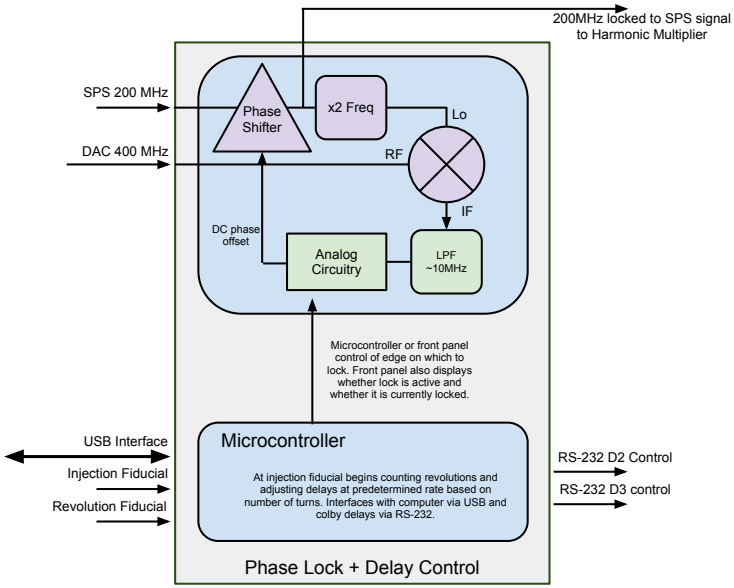


Diagram of phase lock procedure.

Upgrades to Feedback Demonstrator System

- Implement synchronization for full 4GS/sec sampling rate
- Additional software for control interface
- Additional software for data analysis
- Software for feedback/control specification and filter design
- Allow for individually configurable coefficients for each slice sample in the FIR
- Multi-bunch control up to one full batch or possibly more
- DC offset removal
- Extended snapshot memory

Thank You!

- Thank you to the many additional people involved in this project!
  - CERN: W. Hofle, U. Wehrle, H. Bartosik, G. Kotzian, K. Li, and R. Secondo
  - LBL: A. Ratti, S. De Santis, H. Qian, and Z. Paret
  - LNF: A. Drago, A. Gallo, D. Alesini, F. Marcellini, and M. Zobov
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  - KEK: M. Tobiyama